February 1985

Features

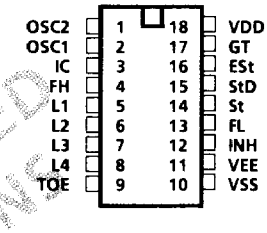
- Central Office quality detection
- Excellent voice talk-off
- Detect times down to 20ms
- Single supply 5V or 8 to 13V operation
- Latched three-state buffered outputs
- Detects all 16 DTMF combinations
- Uses inexpensive 3.58 MHz crystal
- Low power CMOS circuitry
- Adjustable acquisition & release times

Applications

In DTMF Receivers For

- End to end signalling
- Control systems
- PABX
- Central Office
- Mobile Radio
- Key systems
- Tone to pulse converters

Pin Connections



Ordering Information

MT8860XC	18 Pin Ceramic DIP
MT8860XE	18 Pin Plastic DIP

−40 °C to +85 °C

Description

The Mitel MT8860 detects and decodes all 16 DTMF tone pairs.The device accepts the high group and low group squarewave signals from a DTMF FILTER (Mitel MT8865) and provides a three-state buffered 4 Bit binary output. The clock signals are derived from an on-chip oscillator requiring only a single resistor and low cost TV crystal as external components. The MT8860 is implemented in CMOS technology and incorporates an on chip regulator, providing low power operation and power supply flexibility.

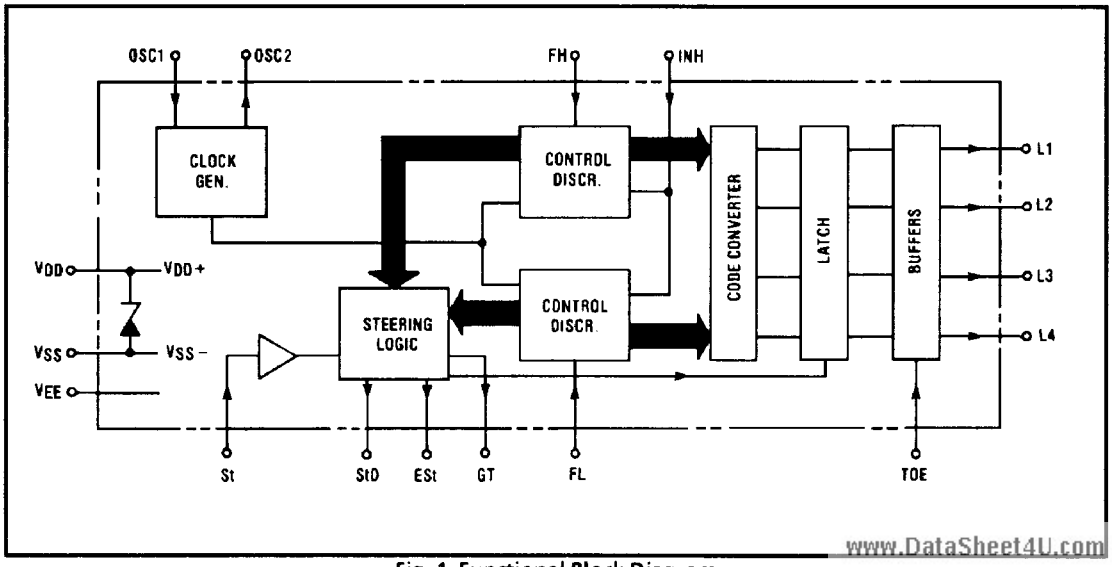


Fig. 1 Functional Block Diagram

Absolute Maximum Ratings*

	Parameter		Symbol	Min	Max	Units
1	V_{DD} - V_{EE}				15	V
2	V_{DD} - V_{SS} (Low Impedance Supply)				5.5	V
3	Voltage on any pin except OS1, OSC2			$V_{EE}-0.3$	$V_{DD}+0.3$	V
4	Voltage on OSC1, OSC2			$V_{SS}-0.3$	$V_{DD}+0.3$	V
5	Max. Current at any pin (except V_{DD} & V_{EE})		I_I		10	mA
6	Storage Temperature	C Package E Package	T_{STG} T_{STG}	−65 −65	+150 +125	°C °C
7	Power Dissipation	C Package① E Package②	P_D P_D		1000 450	mW mW

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
①Derate above 75 °C at 16 mW / °C. All leads soldered to board.
②Derate above 25 °C at 6.3 mW / °C. All leads soldered to board.

Recommended Operating Conditions - All voltages referenced to V_{EE} unless otherwise stated

		Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions
1		DC Power Supply Voltage (V_{DD}-V_{EE})	V_{DD} V_{DD}	4.75 8	5	5.25 13	V V	Connections, Fig. 5a Connections, Fig. 5b
2		Operating Temperature	T_O	−45		+85	°C	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - All voltages referenced to V_{EE}, T_A = 25°C f_c = 3.579545 MHz unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	SUPPLY	Operating Supply Voltage (V_{DD} - V_{EE})	V_{DD} V_{DD}	4.75 8	5	5.25 13	V V	Connections Fig. 5a Connections Fig. 5b
2		Internal Logic Ground Voltage (V_{DD} - V_{SS})	V_{DDSS} V_{DDSS}	4.75 6.0	6.5	5.25 7.5	V V	Connections Fig. 5a I_{dd} = 7mA
3		Operating Supply Current	I_{DD} I_{DD}		1.3 2.5	4 5	mA mA	5V 12V V_{DD} - V_{SS} = 5.5V
4		Internal Logic Ground Pin Current	I_{SS}		5.5	6.7	mA	12V R_{SSEE} = 900Ω
5		Operating Power Consumption	P_O P_O		6.5 66		mW mW	5V 12V
6	INPUTS	High Level Input Voltage (All Inputs Except OSC1)	V_{IH} V_{IH}	3.5 8.5			V V	5V 12V
7		Low Level Input Voltage (All Inputs Except OSC1)	V_{IL} V_{IL}			1.5 3.5	V V	5V 12V
8		High Level Input Voltage OSC1	V_{IHO} V_{IHO}	3.5 10.5			V V	5V 12V
9		Low Level Input Voltage OSC1	V_{ILO} V_{ILO}			1.5 1.5	V V	5V Ref V_{SS} 12V Ref V_{SS}
10		Steering Input Threshold Voltage	V_{TSt} V_{TSt}	2.04 5.4	2.27 6.0	2.5 6.6	V V	5V 12V
11		Pull Down Sink Current (INH)	I_{SI} I_{SI}	10 10	25 190	75 400	µA µA	5V 12V
12		Pull Up Source Current (TOE)	I_{SO}	2	7	45	µA	5V + 12V
13		Input High Leakage Current	I_{IH}		0.1	1.5	µA	5V or 12V
14		Input Low Leakage Current	I_{LH}		0.1	1.5	µA	5V or 12V

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics (cont'd)

All voltages referenced to V_{EE}, $T_A = 25°C$ $f_c = 3.579545$ MHz unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
15	OUTPUTS	High Level Output Voltage (All Outputs Except OSC2)	V_{OH} V_{OH}	4.9 11.9			V V	5V 12V
16		Low Level Output Voltage (All Outputs Except OSC2)	V_{OL} V_{OL}			0.1 0.1	V V	5V 12V
17		High Level Output Voltage OSC2	V_{OHO}	4.9 11.9			V V	5V 12V
18		Low Level Output Voltage OSC2	V_{OL} V_{OL}			0.1 0.1	V V	5V Ref V_{SS} 12V Ref V_{SS}
19		Output Drive Current P Channel Source (All Outputs Except OSC2)	I_{OH} I_{OH}	0.4 0.5	0.6 0.8		mA mA	5V V_{OH} = 4.6V 12V V_{OH} = 11.5V
20		Output Drive Current N Channel Sink (All Outputs Except OSC2)	I_{OL} I_{OL}	0.8 1.0	1.2 1.6		mA mA	5V V_{OL} = 0.4V 12V V_{OL} = 0.5V
21		Output Drive Current - OSC2 P Channel Source	I_{OH} I_{OH}	90 90	120 120		µA µA	5V V_{OH} = 4.6V 12V V_{OH} = 11.5V
22		Output Drive Current - OSC2 N Channel Sink	I_{OL} I_{OL}	100 100	160 160		µA µA	5V V_{OL} = 0.4V 12V V_{OL} = 0.5V
23		Tristate Output Current (High Impedance State) L1-L4 = H L1-L4 = L L1-L4 = H L1-L4 = L	I_{OZ} I_{OZ} I_{OZ} I_{OZ}		0.035 0.1 0.1 0.3	1.5 1.5 1.5 1.5	µA µA µA µA	5V Appl V_{OL} = 0V 5V Appl V_{OH} = 5V 12V Appl V_{OL} = 0V 12V Appl V_{OH} = 12V

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Test Conditions: 5V: $V_{DD} - V_{EE} = 5V$ $V_{SS} = V_{EE}$ Connection as Fig. 5a, 12V: $V_{DD} - V_{EE} = 12V$ $R_{SSEE} = 900\Omega$ Connection as Fig. 5b

For Input current parameters only $V_{IH} = V_{IHO} = V_{DD}$, $V_{IL} = V_{EE}$, $V_{ILO} = V_{SS}$

AC Electrical Characteristics

$V_{DD} = 5V$, $T_A = 25°C$ $f_c = 3.579545$ MHz unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	DETECTOR	Tone Freq. Deviation Accept	Δf_A			±2.5	%Nom.	
2		Tone Freq. Deviation Reject	Δf_R	±3.5			%Nom.	
3		Tone Present Detection Time (MT8860X)	t_{DP}	6		10	ms	
4		Tone Absent Detection Time (MT8860X)	t_{DA}	0.6		6	ms	
5		Guard Time (P or A)	t_{GT}	Adjustable Functions of t_{GT} - See Figs. 2,6,7.				
6		Time to Receive = (t_{DP} + t_{GTP})	t_{REC}					
7		Invalid Tone Duration (f_n of t_{REC})	t_{REC}					
8		Interdigit Pause = (t_{DA} + t_{GTA})	t_{ID}					
9		Acceptable Dropout (f_n of t_{ID})	t_{DO}					
10	I/P	FL FH Input Transition Time	t_T			1.0	µs	10% - 90% V_{DD}
11		Capacitance Any Input	C		5	7.5	pF	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics cont'd - V_{DD} = 5V, T_A = 25°C f_c = 3.579545 MHz unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
12	OUTPUTS	Propagation Delay St to L_1-L_4	t_{PL}		8	11	µs	V_{DD} 5V or 12V
13		Propagation Delay St to StD	t_{PStD}		12	14	µs	V_{DD} 5V or 12V
14		Sync. Delay L_1-L_4 to StD	t_{LStD}		3.43		µs	V_{DD} 5V or 12V
15		Propagation Delay TOE to L1-L4 - Enable	t_{PTE} t_{PTE}		300 200		ns ns	V_{DD} 5V V_{DD} 12V
16		Propagation Delay TOE to L1-L4 - Disable	t_{PTD} t_{PTD}		300 200		ns ns	V_{DD} 5V V_{DD} 12V
17	CLOCK	Crystal/Clock Frequency	f_c	3.5759	3.5795	3.581	MHz	OSC1 OSC2
18		Clock Input (OSC 1) Rise Time	t_{LHCl}			110	ns	10% - 90%
		Fall Time	t_{HLCl}			110	ns	V_{DD}-V_{SS}
		Duty Cycle	DC_{Cl}	40	50	60	%	Externally Applied Clock
19		Clock Output (OSC 2) Capacitive Load	C_{LO}			30	pF	

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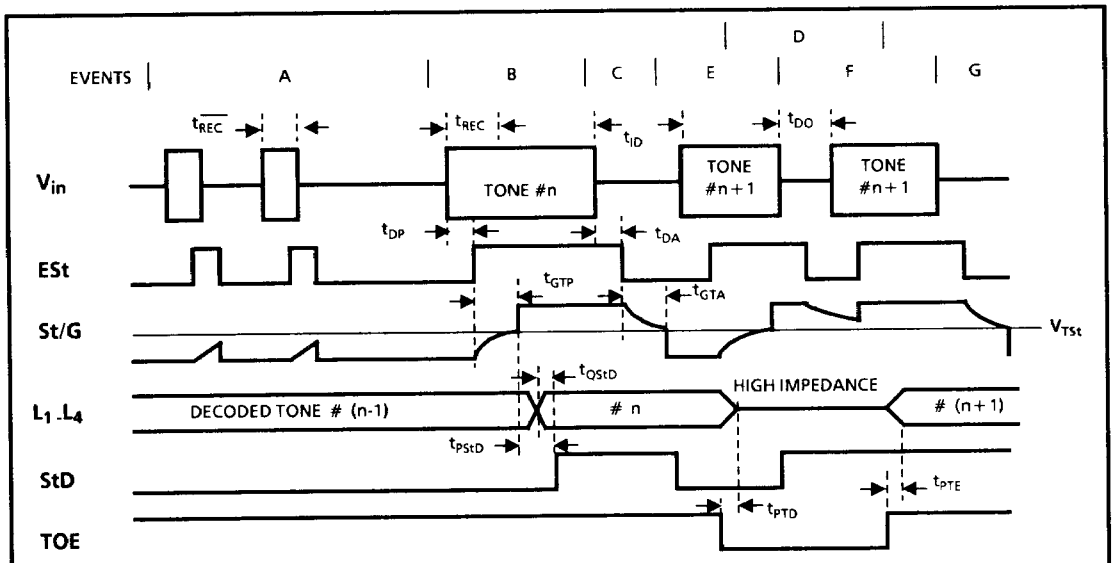


EXPLANATION OF EVENTS

A) TONE BURSTS DETECTED, TONE DURATION INVALID, OUTPUTS NOT UPDATED.

B) TONE #n DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS.

C) END OF TONE #n DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE.

D) OUTPUTS SWITCHED TO HIGH IMPEDANCE STATE.

E) TONE #n+1 DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS (CURRENTLY HIGH IMPEDANCE).

F) ACCEPTABLE DROPOUT OF TONE #n+1, TONE ABSENT DURATION INVALID, OUTPUTS REMAIN LATCHED.

G) END OF TONE #n+1 DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE.

Figure 2- Timing Diagram

Original Tone Character		TOE	L4	L3	L2	L1
	X	L	Z	Z	Z	Z
DR	1	H	L	L	L	H
	2	H	L	L	H	L
	3	H	L	L	H	H
	4	H	L	H	L	L
	5	H	L	H	L	H
	6	H	L	H	H	L
	7	H	L	H	H	H
	8	H	H	L	L	L
	9	H	H	L	L	H
	0	H	H	L	H	L
D	*	H	H	L	H	H
	#	H	H	H	L	L
	A	H	H	H	L	H
	B	H	H	H	H	L
	C	H	H	H	H	H
	D	H	L	L	L	L

Fig. 3a) Output Coding

Detected Character	INH	ESt
None	0	L
X	L	H
DR	H	H
D	H	L

Fig. 3b) Inhibit Function

ESt	St	GT	StD*
L	L	L	L
H	L	Z	L
L	H	Z	H
H	H	H	H

Fig. 3c) Steering
*Delayed wrt St.

For the purpose of these Tables consider:
$V_{St} < V_{TSt}$ Logic LOW (L)
$V_{St} > V_{TSt}$ Logic HIGH (H)

H = LOGIC HIGH L = LOGIC LOW
0 = "DON'T CARE" LOGIC HIGH OR LOW
Z = HIGH IMPEDANCE X = ANY CHARACTER

Fig. 3 - Coding Tables

Pin Description

Pin #	Name	Description
1	OSC2	**Clock Output.**
2	OSC1	**Clock Input.** 3.579545MHz crystal with parallel 5M resistor connected between this pin and OSC2 completes the internal oscillator, running between V_{DD} and V_{SS}.
3	IC	**Internal Connection.** For testing only. Must be left open circuit.
4	FH	**High Frequency Group Input.** Accepts single rectangular wave High group tone from DTMF filter.
5,6, 7,8	L1,L2, L3, L4	**Data Outputs.** Three-state buffered. Provides 4 Bit binary word corresponding to the tone pair decoded, when enabled by TOE. See Fig. 3 for state table.
9	TOE	**Three-state Output Enable Input.** Logic high on this input enables outputs L1-L4. Internal pull-up.
10	V_{SS}	**Internal Logic Ground.** For $V_{DD} - V_{EE} = 5V$ V_{SS} connected to V_{EE}. For $V_{DD} - V_{EE} > 8V$, V_{SS} connected via resistor to V_{EE} see Fig. 5.
11	V_{EE}	**Negative Power Supply.** External logic ground.
12	INH	**Inhibit Input.** Logic high inhibits detection of tones representing characters #, *, A, B, C, D. Internal pull-down.
13	FL	**Low Frequency Group Input.** Accepts single rectangular wave low group tone from DTMF filter.
14	St	**Steering Input.** A voltage greater than V_{TSt} on this input causes the device to accept validity of the detected tone pair and latch the corresponding codeword at the outputs. Voltage < V_{TSt} on this pin frees the device to accept a new tone pair, see Fig. 3c and Functional Description.
15	StD	**Delayed Steering Output.** Flags when a valid tone pair has been received. Presents logic high when output latch updated. When St voltage exceeds V_{TSt}. Returns to logic low when St voltage falls below V_{TSt}.
16	ESt	**Early Steering Output.** Presents a logic high immediately the digital algorithm detects a recognizable tone pair. Any momentary loss of the incoming tone or excessive distortion of the tone will cause ESt to return to a logic low .
17	GT	**Guard Time Output.** Three-state output. Normally connected to St, is used in the steering algorithm and is a function of St and ESt (See Fig. 3c).
18	V_{DD}	**Positive Power Supply.**

Functional Description

The Mitel MT8860 is a CMOS Digital DTMF Detector and Decoder. Used in conjunction with a suitable DTMF filter (Mitel MT8865) it can detect and decode all 16 standard DTMF tone pairs, accurately discriminating between adjacent frequencies in both high and low groups in the presence of noise and normal voice signals.

To form a complete DTMF receiver the MT8860 must be preceded by a DTMF filter, the function of which is to separate the high group and low group components of the composite dual tone signal and limit the resulting pair of sine wave signals to produce rectangular wave signals having the same frequencies as the individual components of the composite DTMF input. The High Group and Low Group rectangular waves are applied to the MT8860's FH and FL inputs respectively. Mitel's MT8865 DTMF Filter provides these functions.

Within the MT8860 the FL and FH signals are operated on by a complex averaging algorithm. This is implemented using digital counting techniques (Control/Discriminators Fig. 1) to determine the frequencies of the incoming tones and verify that they correspond to standard DTMF frequencies. When both High Group and Low Group signals have been simultaneously detected a flag ESt (Logic High) is generated. ESt is generated (cancelled) rapidly on detecting the presence (absence) of a DTMF tone pair (see Fig. 2) and is used to perform a final validity check.

The final validity check requires the input DTMF signal to be present uninterrupted by drop out or excessive distortion (which would result in ESt being cancelled) for a minimum time (t_{REC}) before being considered valid. This contributes greatly to the talk-off performance of the system. The check also imposes a minimum period of "tone absent" before a valid received tone is recognized as having ended. This allows short periods of drop out (t_{DO}) or excessive noise to occur during a received tone, without it being misinterpreted as two successive characters by the steering circuit (ESt, St, GT). A capacitor C (Fig. 7a) is charged via resistor R from ESt when a DTMF tone pair is detected. After a period t_{GTP} V_c exceeds the St input threshold voltage V_{TSt} setting an internal flag indicating the detected signal is valid. Functioning of the check algorithm is completed by the three state output GT which is normally connected to St and operates under the control of ESt and St. Its mode of operation is shown by the steering state table (Fig. 3c) and timing diagram (Fig. 2).

Internally the presence of the ESt flag allows the control/discriminator to identify the detected tones to the code converter which in turn presents a 4 bit binary code word, corresponding to the original transmitted character, to the output latch. The appearance of the internal St flag clocks the latch, presenting the output code at the tristate outputs L_1 to L_4. The St internal flag is delayed (by t_{PStD}) and appears at the StD output to provide a strobe output function indicating that a new character has been received and the output updated. StD will return to a logic low after the St flag has been reset by V_c (Fig. 7a) falling below V_{TSt}.

Increasing the "time to receive" t_{REC} tends to further improve "talk-off" performance (discrimination against voice simulation of a DTMF tone pair) but degrades the acceptable signal to noise ratio for the incoming signal. Increasing interdigit pause t_{ID} further reduces the probability of receiving the same character twice and improves acceptable signal-to-noise ratio but imposes a longer interdigit pause. Reducing t_{REC} or t_{ID} has the opposite effect respectively. The values of t_{REC} and t_{ID} can be tailored by adjusting t_{GTP} and t_{GTA} as shown in Fig. 7.

When L_1 - L_4 are connected to a data bus TOE may be controlled by external circuitry or connected directly to StD automatically enabling the outputs whenever a tone is received. In either case StD may be used to flag external circuitry indicating a character has been received.

The MT8860 may be operated from either a 5 volt or 8 to 13 volt supply by use of the internal zener reference. The relevant connection diagrams are shown in Fig. 5.

When using the MT8860 with the MT8865 DTMF Filter it is only necessary to use the MT8865 crystal oscillator (see Fig. 6). When using the higher supply voltage range the 8865 OSC2 output should be capacitively coupled to the 8860 OSC1 input as shown in Fig. 6.

Where it is desirable to receive only the DTMF digits taking INH to a logic high inhibits detection of the # * ABCD DTMF characters. This also further improves "talk-off" performance due to the reduced number of detectable tones.

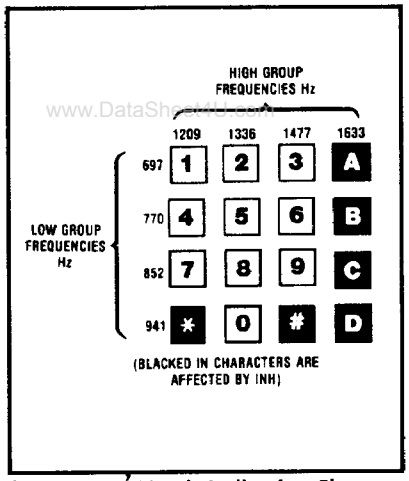


Fig. 4 - DTMF Matrix Indicating Character -Tone Pair Correspondence

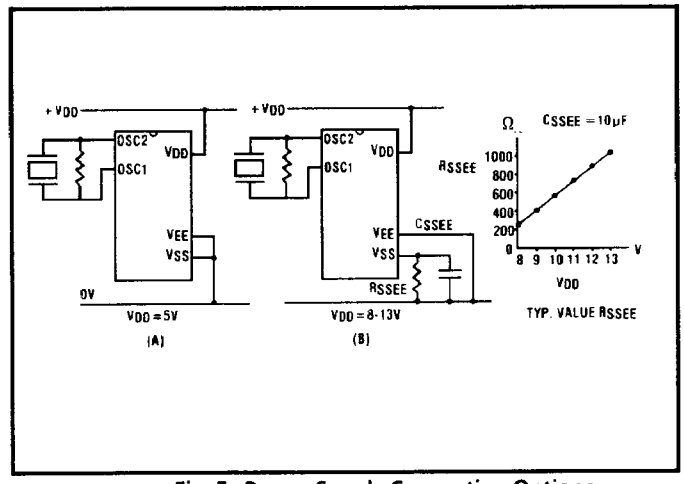


Fig. 5 - Power Supply Connection Options

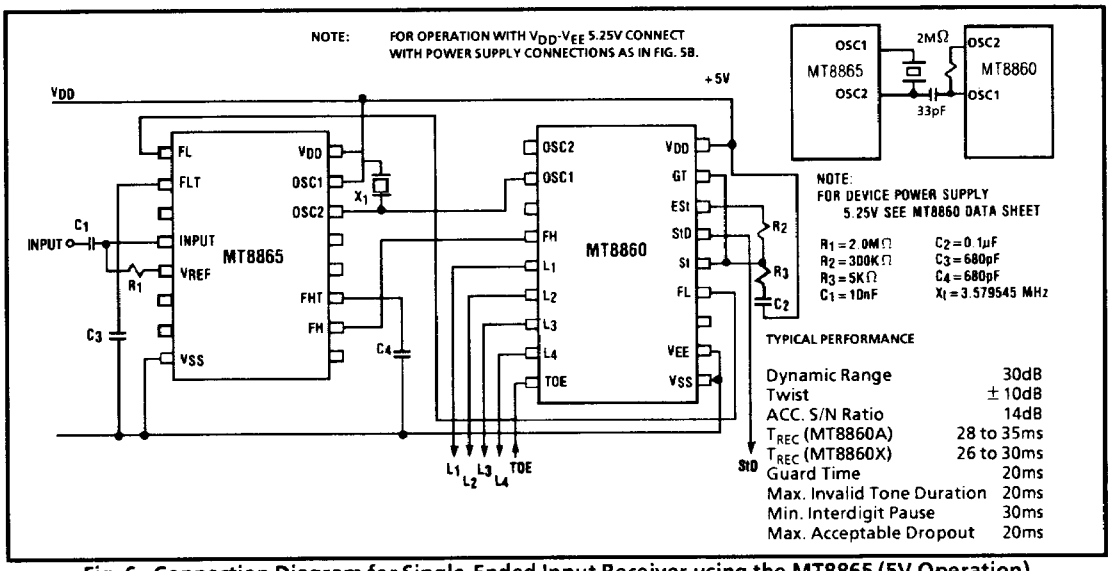


Fig. 6 - Connection Diagram for Single-Ended Input Receiver using the MT8865 (5V Operation)

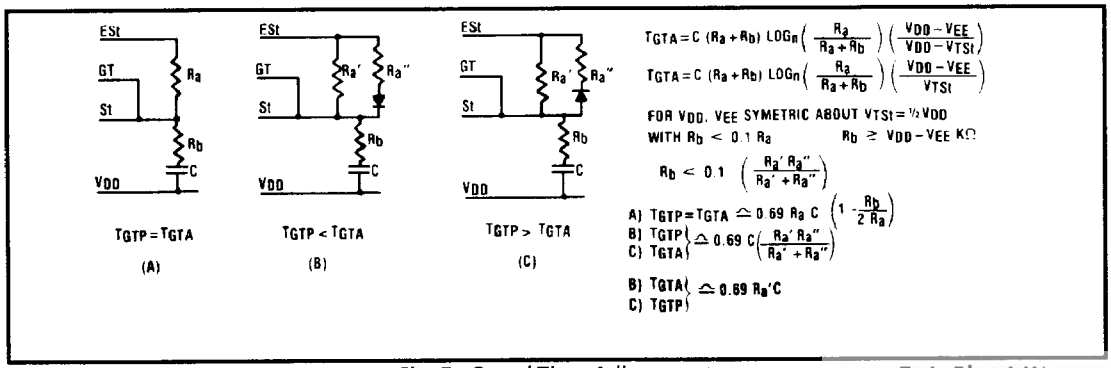
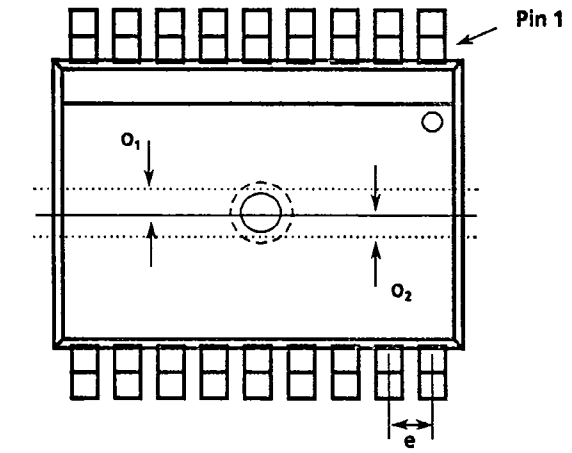
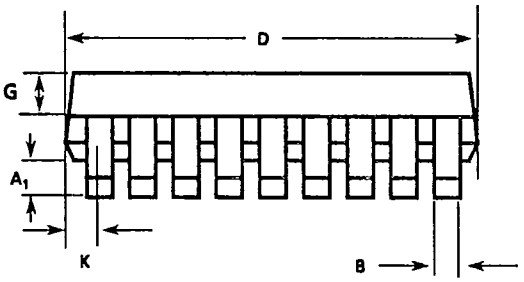
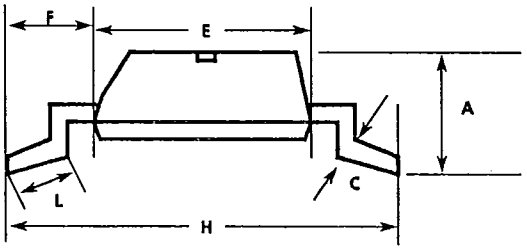


Fig. 7 - Guard Time Adjustment

PACKAGING OUTLINES





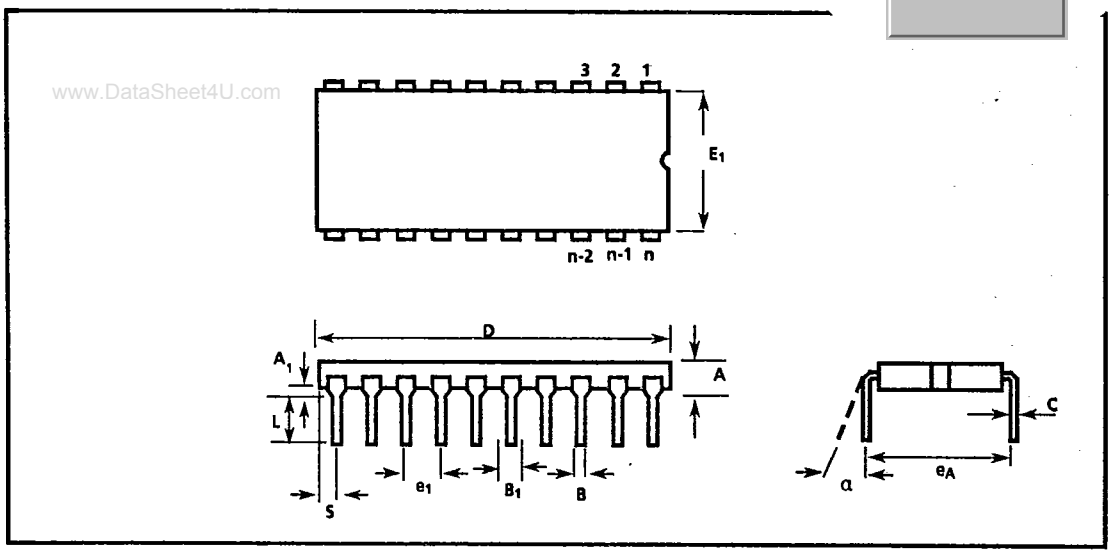


DIM	18-Pin SOIC		20-Pin SOIC	
	Min	Max	Min	Max
A	0.093 (2.35)	0.104 (2.65)	0.093 (2.35)	0.104 (2.65)
A_1	0.004 (0.10)	0.012 (0.30)	0.004 (0.10)	0.012 (0.30)
B	0.014 (0.351)	0.019 (0.488)	0.014 (0.351)	0.019 (0.488)
C	0.009 (0.231)	0.013 (0.318)	0.009 (0.231)	0.013 (0.318)
D	0.447 (11.35)	0.469 (11.90)	0.496 (12.60)	0.518 (13.00)
E	0.291 (7.40)	0.305 (7.75)	0.291 (7.40)	0.305 (7.75)
e	0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)	
F	0.044 (1.125)	0.064 (1.625)	0.044 (1.125)	0.064 (1.625)
G	0.040 (1.016)	0.050 (1.270)	0.040 (1.016)	0.050 (1.270)
H	0.394 (10.00)	0.419 (10.65)	0.394 (10.00)	0.419 (10.65)
K	0.035 (0.889)	0.045 (1.143)	0.035 (0.889)	0.045 (1.143)
L	0.016 (0.40)	0.050 (1.27)	0.016 (0.40)	0.050 (1.27)
O_1	-	0.005 (0.13)	-	0.005 (0.13)
O_2	-	0.005 (0.13)	-	0.005 (0.13)

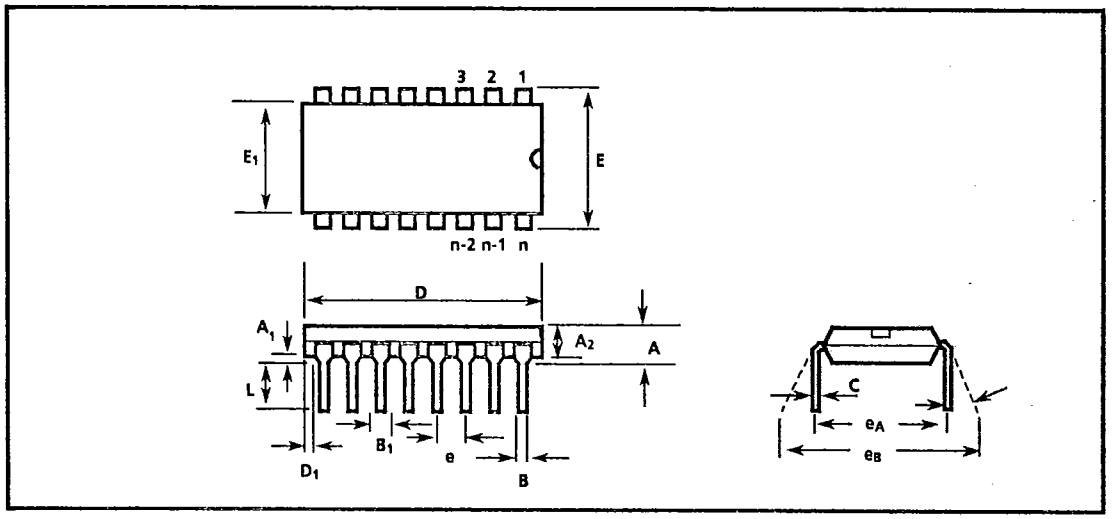
NOTE: ( ) millimeters

NOTES:
1) A & B Maximum dimensions include allowable mold flash.
2) O_1 & O_2 are SYMMETRY dimensions.

Lead SOIC Package (S Suffix)



Ceramic Dual-In-Line Packages (CDIP) - C Suffix



Plastic Dual-In-Line Packages (PDIP) - E Suffix

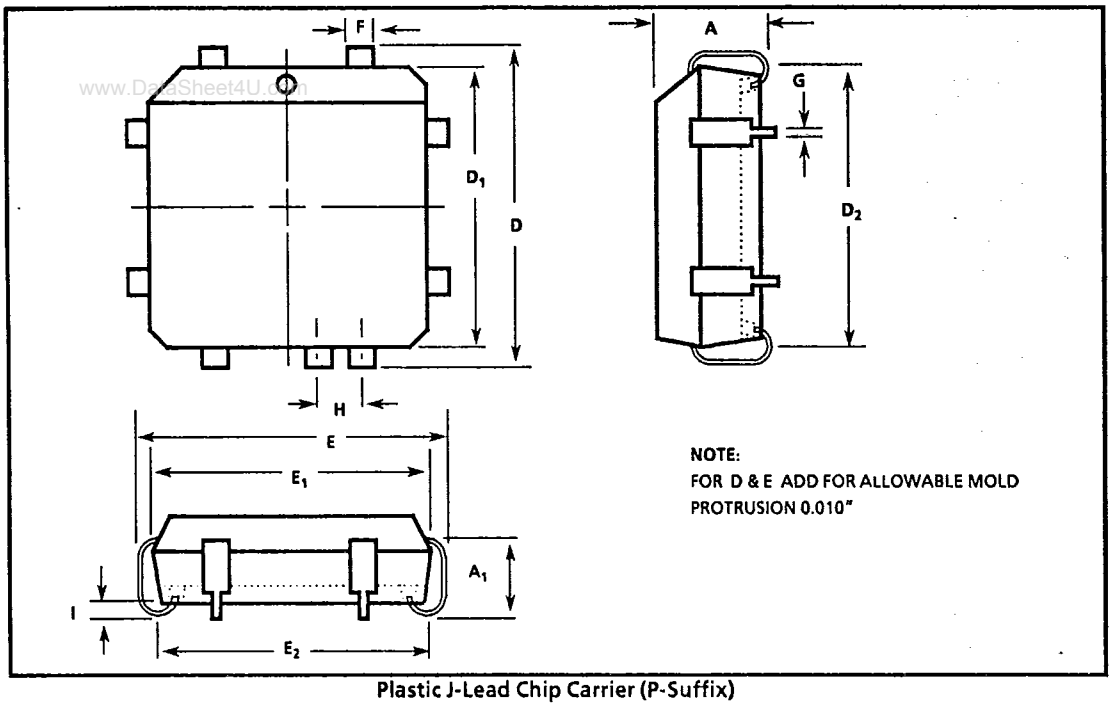
Package Outlines

DIM	8-Pin				16-Pin				18-Pin				20-Pin			
	Plastic		Ceramic		Plastic		Ceramic		Plastic		Ceramic		Plastic		Ceramic	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A		0.210 (5.33)	0.105 (2.67)	0.200 (5.08)		0.210 (5.33)	0.105 (2.67)	0.200 (5.08)		0.210 (5.33)	0.105 (2.67)	0.200 (5.08)		0.210 (5.33)	0.105 (2.67)	0.200 (5.08)
A_1			0.025 (0.64)	0.055 (1.39)			0.025 (0.64)	0.055 (1.39)			0.025 (0.64)	0.055 (1.39)			0.025 (0.64)	0.055 (1.39)
A_2	0.115 (2.93)	0.195 (4.95)			0.115 (2.93)	0.195 (4.95)			0.115 (2.93)	0.195 (4.95)			0.115 (2.93)	0.195 (4.95)		
B	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.021 (0.533)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.021 (0.533)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.021 (0.533)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.021 (0.533)
B_1	0.045 (1.15)	0.070 (1.77)	0.035 (0.89)	0.060 (1.52)	0.045 (1.15)	0.070 (1.77)	0.035 (0.89)	0.060 (1.52)	0.045 (1.15)	0.070 (1.77)	0.035 (0.89)	0.060 (1.52)	0.045 (1.15)	0.070 (1.77)	0.035 (0.89)	0.060 (1.52)
C	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)
D	0.348 (8.84)	0.430 (10.92)	0.380 (9.7)	0.550 (13.9)	0.745 (18.93)	0.840 (21.33)		0.784 (19.9)	0.845 (21.47)	0.925 (23.49)	0.880 (22.36)	0.930 (23.62)	0.925 (23.49)	1.060 (26.9)		0.996 (25.3)
D_1	0.005 (0.13)				0.005 (0.13)				0.005 (0.13)				0.005 (0.13)			
E	0.290 (7.37)	0.330 (8.38)			0.290 (7.37)	0.330 (8.38)			0.290 (7.37)	0.330 (8.38)			0.290 (7.37)	0.330 (8.38)		
E_1	0.240 (6.10)	0.280 (7.11)	0.280 (7.12)	0.310 (7.87)	0.240 (6.10)	0.280 (7.11)	0.280 (7.12)	0.310 (7.87)	0.240 (6.10)	0.280 (7.11)	0.280 (7.12)	0.310 (7.87)	0.240 (6.10)	0.280 (7.11)	0.280 (7.12)	0.310 (7.87)
e	0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)			
e_1			0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)	
e_A	0.300 BSC (7.62 BSC)		0.300 BSC (7.62 BSC)		0.300 BSC (7.62 BSC)		0.300 BSC (7.62 BSC)		0.300 BSC (7.62 BSC)		0.300 BSC (2.54 BSC)		0.300 BSC (7.62 BSC)		0.300 BSC (7,62 BSC)	
e_B		0.430 (10.92)				0.430 (10.92)				0.430 (10.92)				0.430 (10.92)		
L	0.115 (2.93)	0.160 (4.06)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.160 (4.06)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.160 (4.06)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.160 (4.06)	0.125 (3.18)	0.175 (4.44)
S				0.120 (3.04)				0.120 (3.04)				0.120 (3.04)				0.120 (3.04)
α			0°	15°			0°	15°			0°	15°			0°	15°

NOTE: ( ) Millimeters

DIM	22-Pin				24-Pin				28-Pin				40-Pin			
	Plastic		Ceramic		Plastic		Ceramic		Plastic		Ceramic		Plastic		Ceramic	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A		0.210 (5.33)	0.090 (2.29)	0.225 (5.71)		0.250 (6.35)	0.085 (2.2)	0.190 (4.8)		0.250 (6.35)	0.085 (2.2)	0.190 (4.8)		0.250 (6.35)	0.085 (2.2)	0.190 (4.8)
A_1			0.025 (0.64)	0.055 (1.39)			0.020 (0.51)	0.070 (1.77)			0.020 (0.51)	0.070 (1.77)			0.020 (0.51)	0.070 (1.77)
A_2	0.125 (3.18)	0.195 (4.95)			0.125 (3.18)	0.195 (4.95)			0.125 (3.18)	0.195 (4.95)			0.125 (3.18)	0.195 (4.95)		
B	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.023 (0.584)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.023 (0.584)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.023 (0.584)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.023 (0.584)
B_1	0.045 (1.15)	0.070 (1.77)	0.028 (0.71)	0.060 (1.52)	0.030 (0.77)	0.070 (1.77)	0.028 (0.71)	0.060 (1.52)	0.030 (0.77)	0.070 (1.77)	0.028 (0.71)	0.060 (1.52)	0.030 (0.77)	0.070 (1.77)	0.028 (0.71)	0.060 (1.52)
C	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)
D	1.050 (26.67)	1.120 (28.44)	1.040 (26.42)	1.260 (32.0)	1.150 (29.3)	1.290 (32.7)	1.180 (29.88)	1.291 (32.80)	1.380 (35.1)	1.565 (39.7)	1.380 (35.06)	1.520 (38.61)	1.980 (50.3)	2.095 (53.2)	1.980 (50.30)	2.110 (53.60)
D_1	0.005 (0.13)				0.005 (0.13)				0.005 (0.13)				0.005 (0.13)			
E	0.390 (9.91)	0.430 (10.92)			0.600 (15.24)	0.670 (17.02)			0.600 (15.24)	0.670 (17.02)			0.600 (15.24)	0.670 (17.02)		
E_1	0.330 (8.39)	0.380 (9.65)	0.350 (8.89)	0.410 (10.41)	0.485 (12.32)	0.580 (14.73)	0.516 (13.11)	0.610 (15.49)	0.485 (12.32)	0.580 (14.73)	0.480 (12.19)	0.610 (15.49)	0.485 (12.32)	0.580 (14.73)	0.480 (12.19)	0.618 (15.70)
e	0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)			
e_1			0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)	
e_A	0.400 BSC (10.16 BSC)		0.400 BSC (10 .16 BSC)		0.600 BSC (15.24 BSC)		0.600 BSC (15.24 BSC)		0.600 BSC (15.24 BSC)		0.600 BSC (15.24 BSC)		0.600 BSC (15.24 BSC)		0.600 BSC (15.24 BSC)	
e_B		0.500 (12.70)				0.700 (17.78)				0.700 (17.78)				0.700 (17.78)		
L	0.115 (2.93)	0.160 (4.06)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.200 (5.08)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.200 (5.08)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.200 (5.08)	0.125 (3.18)	0.175 (4.44)
S				0.120 (3.04)				0.100 (2.54)				0.800 (2.05)				0.800 (2.05)
α			0°	15°			0°	15°			0°	15°			0°	15°

NOTE: ( ) Millimeters



Plastic J-Lead Chip Carrier (P-Suffix)

DIM	20-Pin PLCC		28-Pin PLCC		44-Pin PLCC		68-Pin PLCC		84-Pin PLCC	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	0.165 (4.20)	0.180 (4.57)	0.165 (4.20)	0.180 (4.57)	0.165 (4.20)	0.180 (4.57)	0.165 (4.20)	0.200 (5.08)	0.165 (4.20)	0.200 (5.08)
A_1	0.090 (2.29)	0.120 (3.04)	0.090 (2.29)	0.120 (3.04)	0.090 (2.29)	0.120 (3.04)	0.090 (2.29)	0.130 (3.30)	0.090 (2.29)	0.130 (3.30)
B			0.020 TP (0.511 TP)							
B_1										
B_2										
D/E	0.385 (9.78)	0.395 (10.03)	0.485 (12.32)	0.495 (12.57)	0.685 (17.40)	0.695 (17.65)	0.985 (25.02)	0.995 (25.27)	0.185 (30.10)	1.195 (30.35)
D_1/E_1	0.350 (8.890)	0.356 (9.042)	0.450 (11.430)	0.456 (11.582)	0.650 (16.510)	0.656 (16.662)	0.950 (24.130)	0.958 (24.333)	1.150 (29.210)	1.158 (29.413)
D_2/E_2	0.290 (7.37)	0.330 (8.38)	0.390 (9.91)	0.430 (10.92)	0.590 (14.99)	0.630 (16.00)	0.890 (22.61)	0.930 (23.62)	1.090 (27.69)	1.130 (28.70)
D_4/E_4										
e			0.050 BSC (1.27 BSC)							
F	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)
G	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)
H	0.050 BSC (1.27 BSC)				0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)	
h			0.040 BSC (1.02 BSC)							
h_1										
I	0.020 (0.51)		0.020 (0.51)		0.020 (0.51)		0.020 (0.51)		0.020 (0.51)	
L										
L_1										
R_1										

NOTE: ( ) Millimeters