ISSUE 1 May 1995

Features

- DS3 payload access in either bit-serial or nibble-parallel mode
- C-bit parity or M13 operating mode
- Separate interface for C-bits
- Detect and generate DS3 AIS, and idle signals
- Transmit reference generator for serial operation
- Transmit and receive FEAC channel under software control
- Transmit single errors: framing, FEBE, C-bit parity, and P-bit parity
- FEBE, C-bit and P-bit performance counters
- Transmit-to-Receive and Receive-to-Transmit loopbacks

Applications

- Subrate multiplexing
- Wideband data or video transport
- DS3 monitor and test
- Channel extenders

Ordering Information

MT90733AP 68 Pin PLCC

-40° to 85°C

Description

The MT90733 DS3 Framer (DS3F) is designed for mapping broadband payloads into the DS3 frame format, which meets ANSI's T1.107-1988 and supplement T1.107a-1990.

Although the C-bit parity format is recommended, the DS3F can also operate in the M13 mode. In the C-bit parity format, the DS3F provides a separate interface for selected C-bits. The DS3F also provides software access for transmitting and receiving the FEAC channel, and generates and detects DS3 AIS, DS3 idle, P-bit parity and C-bit parity. In addition, performance counters are provided, as well as the ability to generate single framing, FEBE, C-bit parity and P-bit parity errors. The payload interface is selectable through software as either a bit-serial or nibble-parallel format.

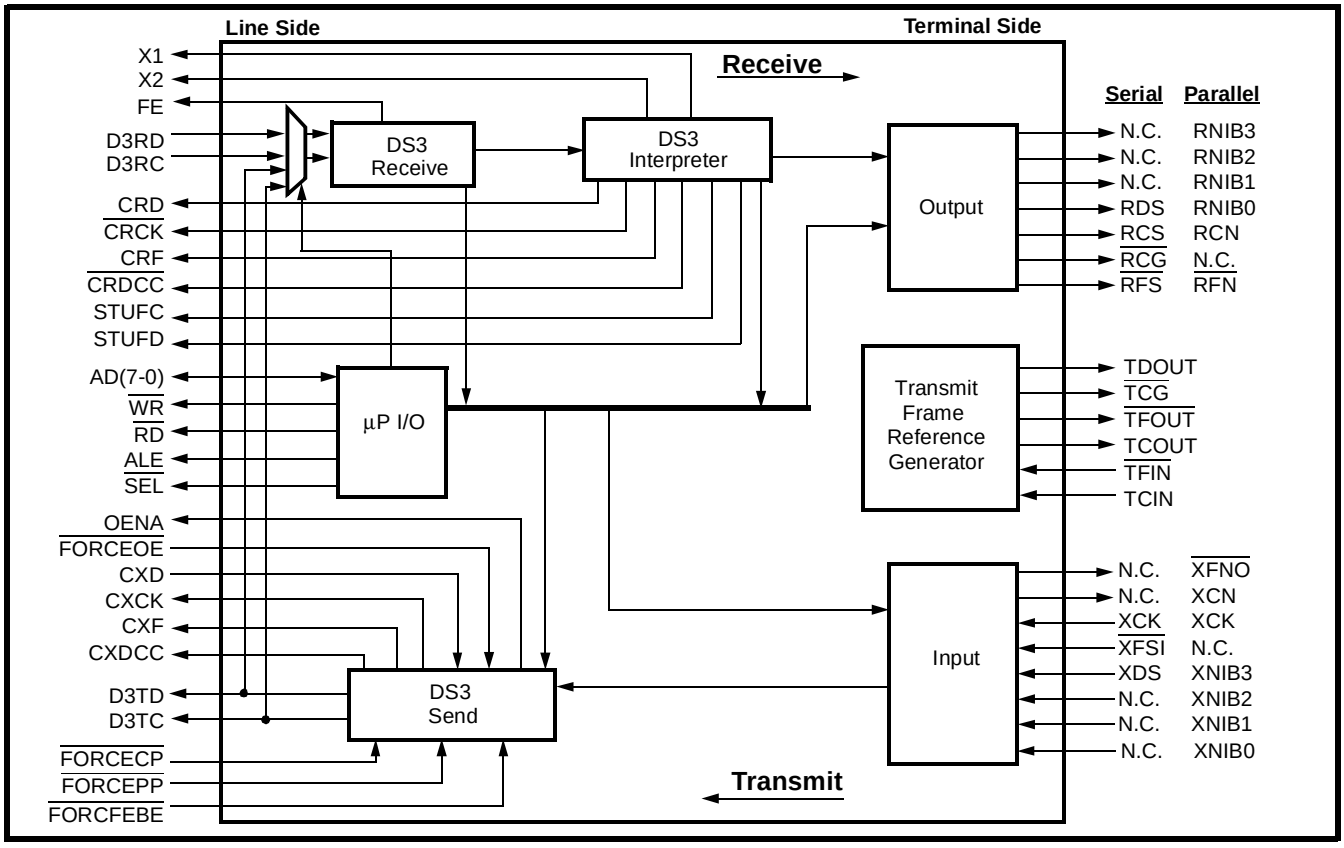

Figure 1 - Functional Block Diagram

U.S. Patent Number 5040170

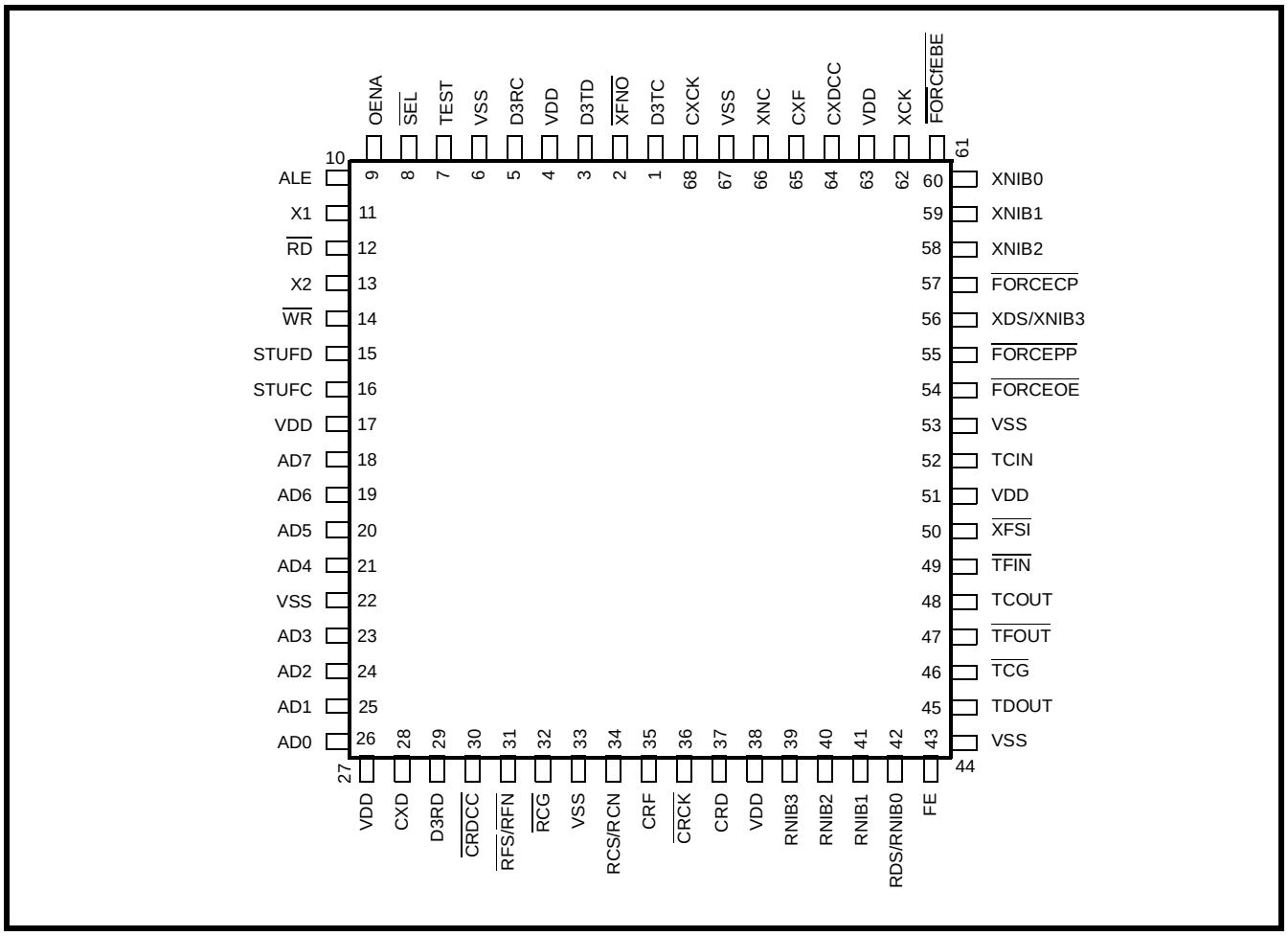

Figure 2 - Pin Connections

Pin Description

Power Supply & Ground

Pin #	Name	I/O/P	Description
4, 17, 27 38, 51, 63	VDD	P	**Power Supply Input.** +5v± 5%.
6, 22, 33 44, 53, 67	VSS	P	**Ground**.

Note: I = Input; O = Output; P = Power

DS3 Receive Line Side Interface

Pin #	Name	I/O/P	Description
5	D3RC	I	**DS3 Receive Clock.** A 44.736 MHz clock used for clocking in receive data, and as the time base for the DS3F receiver.
29	D3RD	I	**DS3 Receive Data.** DS3 line side serial receive data.

Note: I = Input; O = Output; P = Power

DS3 Transmit Line Side Interface

Pin #	Name	I/O/P	Description
1	D3TC	O	**DS3 Transmit Clock.** A 44.736 MHz clock that is derived from the transmit clock (XCK) signal and is used for clocking out the line side DS3 data signal.
3	D3TD	O	**DS3 Transmit Data.** DS3 line side serial transmit data.

Note: I = Input; O = Output; P = Power

Receive Terminal Side Interface

Pin #	Name	I/O/P	Description
31	$\overline{\text{RFS}}$/$\overline{\text{RFN}}$	O	**Receive Framing Pulse for Serial/Nibble Interface.** The framing pulse is synchronous with the first bit 1 in the DS3 frame or nibble 1175.
32	$\overline{\text{RCG}}$	O	**Receive Clock Gap Signal.** The active low gap signal is synchronous with each overhead bit in the serial DS3 frame (first bit in the 85-bit group).
34	RCS/RCN	O	**Receive Clock for Serial/Nibble Interface.** Clock used for clocking out the terminal side receive serial and nibble data.
39 40 41 42	RNIB3 RNIB2 RNIB1 RDS/RNIB0	O	**Receive Nibble/Serial Interface.** Nibble data is clocked out on positive transitions of the nibble clock (RCN). Serial data is clocked out on negative transitions of the receive clock (RCS).

Note: I = Input; O = Output; P = Power

Transmit Terminal Side Interface

Pin #	Name	I/O/P	Description
2	$\overline{\text{XFNO}}$	O	**Transmit Framing Pulse for Nibble Interface.** An active low, one nibble clock cycle wide (XCN) pulse that occurs during the second nibble time.
50	$\overline{\text{XFSI}}$	I	**Transmit Framing Pulse for Serial Interface:** A framing pulse input that must be synchronous with bit 1 in the transmit serial data DS3 frame.
56 58 59 60	XDS/XNIB3 XNIB2 XNIB1 XNIB0	I	**Transmit Nibble/Serial Interface.** Nibble data is clocked in on positive transitions of the nibble clock (XCN). Serial data is clocked into the DS3F on positive transitions of the transmit clock (XCK).
62	XCK	I	**Transmit Clock.** A 44.736 Mbit/s clock input with a stability of ±20 ppm and a duty cycle of 50 ±10%. XCK provides the time base for the transmitter in the DS3F.
66	XCN	O	**Transmit Clock for Nibble Interface.** Output clock signal derived from the transmit clock (XCK).

Note: I = Input; O = Output; P = Power

Transmit Reference Generator Interface

Pin #	Name	I/O/P	Description
45	TDOUT	O	**Transmit Reference Generator Data Output.** A DS3 frame is provided on this signal lead with only the appropriate M and F bits. All other bits in the frame are held active low.
46	$\overline{\text{TCG}}$	O	**Transmit Reference Generator Clock Gap Signal.** An active low, one clock cycle wide (TCOUT) output signal that is synchronous with bit 1 in each 85-bit group (56 overhead bits) in the DS3 frame.
47	$\overline{\text{TFOUT}}$	O	**Transmit Reference Generator Framing Pulse.** An active low, one clock cycle wide (TCOUT) output pulse that is synchronous with bit 1 in the DS3 frame.
48	TCOUT	O	**Transmit Reference Generator Clock Out.** Clock signal that is derived from the transmit reference generator clock input (TCIN).
52	TCIN	I	**Transmit Reference Generator Clock In.** A 44.736 Mbit/s clock with a stability of ±20 ppm and a duty cycle of 50 ±10%.

Note: I = Input; O = Output; P = Power

Receive C-Bit Interface

Pin #	Name	I/O/P	Description
30	$\overline{\text{CRDCC}}$	O	**C-Bit Receive Data Link Clock.** A gapped clock provided for clocking in the three data link bits (C13, C14, and C15) into external circuitry from the serial data (CRD).
35	CRF	O	**C-Bit Receive Framing Pulse.** Provides a time base reference for clocking in the C-bits in a DS3 frame.
36	$\overline{\text{CRCK}}$	O	**C-Bit Receive Clock.** A gapped clock which clocks C-bit data out of the DS3F on positive transitions.
37	CRD	O	**C-Bit Receive Data.** Serial interface for receiving the selected C-bits in the C-bit parity mode.

Note: I = Input; O = Output; P = Power

Transmit C-Bit Interface

Pin #	Name	I/O/P	Description
28	CXD	I	**C-Bit Transmit Data.** Serial interface for transmitting the selected C-bits in the C-bit parity mode.
64	CXDCC	O	**C-Bit Transmit Data Link Clock.** A gapped clock provided for clocking the three data link bits (C13, C14, and C15).
65	CXF	O	**C-Bit Transmit Framing Pulse.** Identifies the location of the first C-bit in the DS3 frame.
68	CXCK	O	**C-Bit Transmit Clock.** A gapped clock which clocks the external C-bit serial data into the DS3F on positive transitions.

Note: I = Input; O = Output; P = Power

Other Signals

Pin #	Name	I/O/P	Description
7	TEST	I	**Test Pin:** Leave open.
9	OENA	O	**Overhead Enable.** An active high signal that enables an overhead error to be introduced into the overhead bit in the next 85th group by placing a low on the FORCEOE lead.
11	X1	O	**DS3 Received X-Bit 1.** An output indication of the state of the first X-bit received in the DS3 frame.
13	X2	O	**DS3 Received X-Bit 2.** An output indication of the state of the second X-bit received in the DS3 frame (bit 680).
15	STUFD	O	**Stuff Data Status.** This output signal provides an indication of the state of the stuff opportunity bit from the received DS3F frame.
16	STUFC	O	**Stuff Clock.** Provided for clocking out the stuff opportunity bit state.
43	FE	O	**Framing Error Indication.** An active high signal is generated when a framing error is detected while in frame alignment. The framing error indication is held active low when a DS3 out of frame alarm occurs.
49	$\overline{\text{TFIN}}$	I	**Optional Framing Input Pulse.** Not required for normal operation.
54	$\overline{\text{FORCEOE}}$	I	**Force DS3 Overhead Bit Error.** An active low input signal used in conjunction with the overhead enable signal (OENA) for introducing an overhead bit error in the next transmitted 85-bit group.
55	$\overline{\text{FORCEPP}}$	I	**Force P-Bit Parity Error.** An active low input signal generates and transmits a P-bit error by inverting both P-bits.
57	$\overline{\text{FORCECP}}$	I	**Force C-Bit Parity Error.** An active low input signal generates and transmits a C-bit parity error when operating in the C-bit parity mode.
61	$\overline{\text{FORCFEBE}}$	I	**Force FEBE Error.** An active low input signal generates and transmits a far end block error (FEBE) when operating in the C-bit parity mode.

Note: I = Input; O = Output; P = Power

Microprocesssor Interface

Pin #	Name	I/O/P	Description
8	$\overline{\text{SEL}}$	I	**Microprocessor Select.** A low enables the processor to access the DS3F memory map for control, status and alarm information.
10	ALE	I	**Address Latch Enable.** An active high input signal is used by the processor to hold an address stable during a read/write bus cycle on the falling edge.
12	$\overline{\text{RD}}$	I	**Read.** An active low input signal generated by the processor for reading the registers which reside in the DS3F memory map.
14	$\overline{\text{WR}}$	I	**Write.** An active low input signal generated by the processor for writing to the registers which reside in the memory map.
18-21 23-26	AD(7-4) AD(3-0))	I/O	**Address/Data Bus.** These leads constitute the time multiplexed address and data bus for accessing the registers which reside in the DS3F memory map.

Note: I = Input; O = Output; P = Power

Functional Description

The MT90733 (DS3F) is designed for DS3 framer applications in which broadband payloads are mapped into the DS3 frame format. Although the C-bit parity format is recommended, the DS3F can also operate in the M13 mode. In the C-bit parity format, the DS3F provides a separate interface for selected C-bits. The DS3F can transmit and receive the FEAC channel, generate and detect DS3 AIS, DS3 idle, P-bit parity and C-bit parity. In addition, performance counters are provided, as well as the ability to generate single framing, FEBE, C-bit parity and P-bit parity errors. The payload interface is selectable through software as either a bit serial or nibble-parallel format. Figure 1 shows the block diagram for the MT90737 (DS3F).

The DS3F receives a DS3 data signal (D3RD) and a clock signal (D3RC) from a line interface device. The DS3 receive block performs DS3 frame alignment, monitors the signal and the input clock for loss of signal (LOS), out of frame (OOF), and loss of clock (LOC). A framing error (FE) output is provided to indicate when any of the 28 framing bits in the DS3 signal are in error.

The DS3 Interpreter Block performs P-bit and C-bit parity detection and error counting, receive AIS and idle pattern detection, far end block error (FEBE) detection and error counting, far end alarm and control (FEAC) code word detection, C-bit reception, and X-bit reception. Serial interfaces are provided for the received X-bits and for 14 of the 21 C-bits. The clock signal (CRCK) is gapped and is available only for clocking out C-bits C2, C3 through C6, and C13 through C21. The data communication link clock (CRDCC) is present only for C-bits C13, C14, and C15, which are assigned as a data communication channel. An interface that indicates the state of the stuff opportunity bit (STUFD) during each of the seven DS3 subframes and a clock signal (STUFC) is also provided.

The Output Block provides a bit-serial or a nibble-parallel interface. The interface is selected by writing a control bit in the memory map, and is common to the DS3F receive and transmit circuitry.

In the transmit direction, the Input Block provides either a serial or parallel interface. The DS3 Send Block performs P-bit and C-bit parity generation, AIS and idle pattern generation, far end alarm and control (FEAC) transmission, X-bit insertion, and C-bit insertion. The C-bits may be generated internally (such as C-bit parity), written by the microprocessor (such as the FEAC channel), or provided from the external C-bit interface.

DS3 loopback is controlled by setting a bit in the memory map. The entire device is used when loopback is in affect, but the line side input data and clock are blocked (by the gate preceding the DS3 Framer Block shown in Figure 1).

The capability to generate and transmit single overhead bit errors is also provided. External interfaces are provided for transmitting a far end block error (FORCFEBE), a P-bit parity error (FORCEPP), a C-bit parity error (FORCECP) and an overhead bit error (FORCEOE). The FORCEOE signal is used in conjunction with the enable signal (OENA) for introducing an overhead bit error in the next 85-bit segment of the DS3 frame.

The Transmit Frame Reference Generator Block provides reference timing for bit-serial operation. This block accepts an external 44.736 MHz clock signal (TCIN) and derives a clock signal (TCOUT), a framing pulse (TFOUT), a clock gap signal (TCG) and a data signal (TDOUT). The TDOUT signal consists of framing bits and zeros elsewhere.

The microprocessor bus interface consists of eight bidirectional data and address leads (AD7-AD0), along with other microprocessor control leads. The microprocessor bus is used to write control information and to read status information and alarms.

Typical Applications

Figure 3 shows an application of the MT90733 in wideband data transmission at 44.736Mb/s. The Line Interface Unit (LIU) interfaces to the line on one side and to the MT90733 on the other. The MT90733, with the nibble-parallel interface on the terminal side, can provide the payload data without the overhead information. Similarly, the overhead data can be loaded from the terminal side and mapped into DS3 format by the MT90733. The C-bits may be inserted internally, written by the microprocessor, or generated by the external C-bit interface.

Figure 4 shows a video application where the MT90733 is used for the reception of TV signals and commands transmission. Simple compression techniques allow the TV signal to be transmitted and received in DS3 bandwidth. The bandwidth required for the command channel in the other direction is very low.

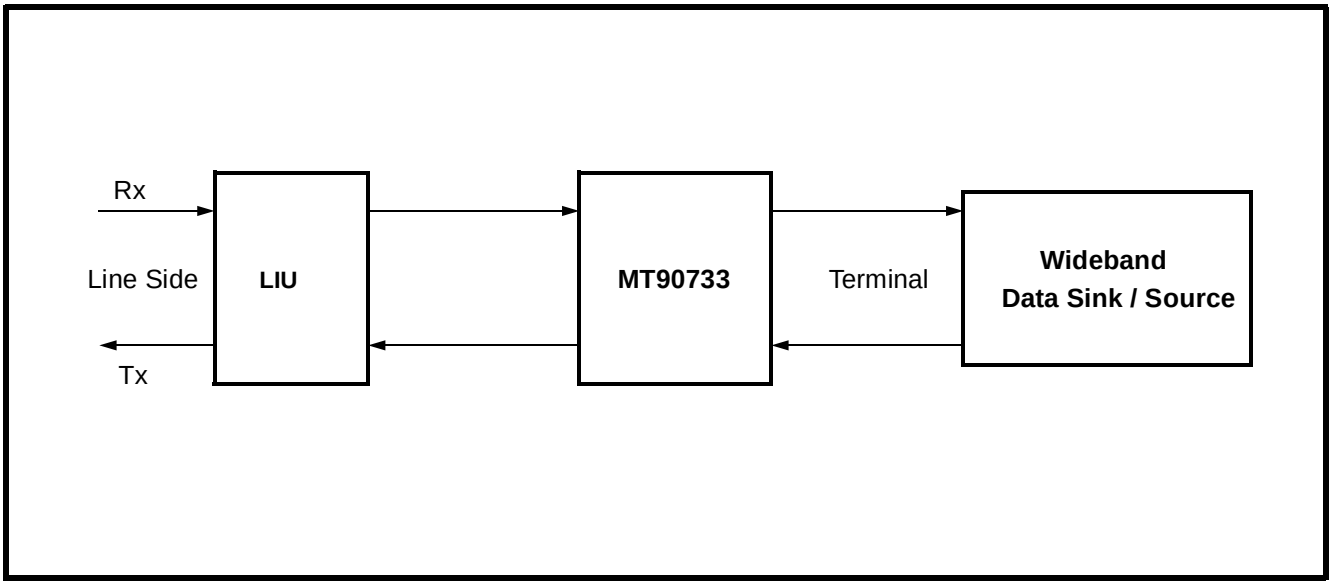

Figure 3. Wideband Data Transport Using MT90733

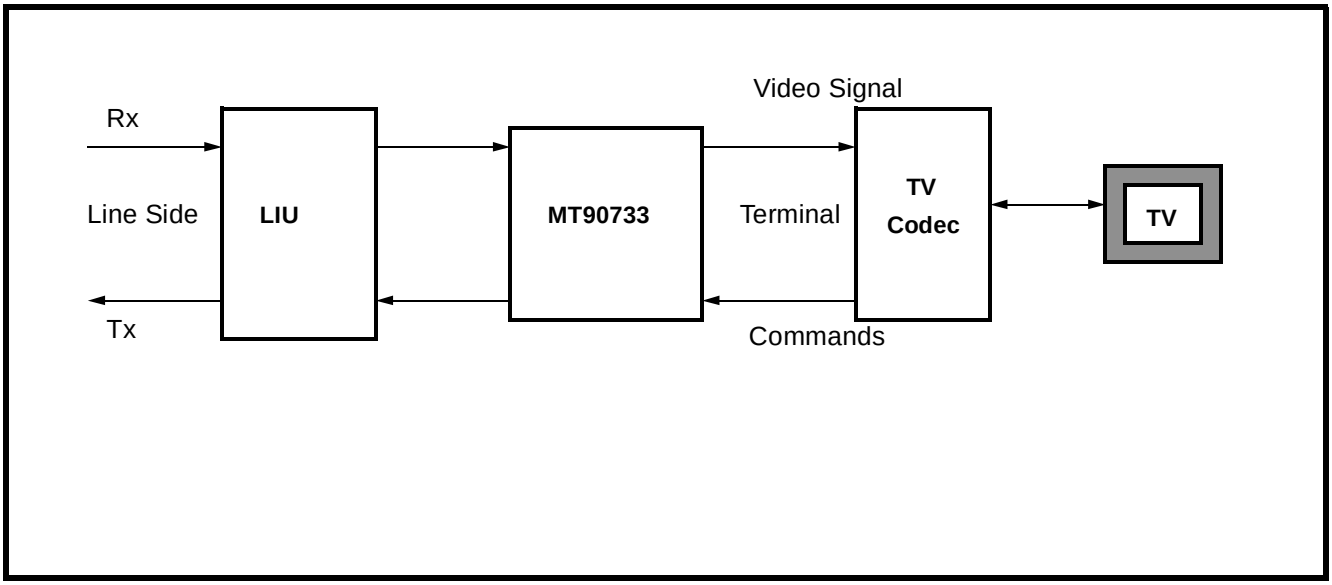

Figure 4. Video Application Using MT90733

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