MITEL
SEMICONDUCTOR

MT9042C

Multitrunk System Synchronizer

Advance Information

DS5144 ISSUE 2 September 1999

Features

- Meets jitter requirements for: AT&T TR62411 Stratum 3, 4 and Stratum 4 Enhanced for DS1 interfaces; and for ETSI ETS 300 011, TBR 4, TBR 12 and TBR 13 for E1 interfaces
- Provides C1.5, $\overline{\text{C3}}$, C2, $\overline{\text{C4}}$, C8 and $\overline{\text{C16}}$ output clock signals
- Provides 8kHz ST-BUS framing signals
- Selectable 1.544MHz, 2.048MHz or 8kHz input reference signals
- Accepts reference inputs from two independent sources
- Provides bit error free reference switching - meets phase slope and MTIE requirements
- Operates in either Normal, Holdover and Freerun modes

Applications

- Synchronization and timing control for multitrunk T1 and E1 systems
- ST-BUS clock and frame pulse sources
- Primary Trunk Rate Converters

Ordering Information	
MT9042CP	28 Pin PLCC
-40°C to +85°C	

Description

The MT9042C Multitrunk System Synchronizer contains a digital phase-locked loop (DPLL), which provides timing and synchronization signals for multitrunk T1 and E1 primary rate transmission links.

The MT9042C generates ST-BUS clock and framing signals that are phase locked to either a 2.048MHz, 1.544MHz, or 8kHz input reference.

The MT9042C is compliant with AT&T TR62411 Stratum 3, 4 and 4 Enhanced, and ETSI ETS 300 011. It will meet the jitter tolerance, jitter transfer, intrinsic jitter, frequency accuracy, holdover accuracy, capture range, phase slope and MTIE requirements for these specifications.

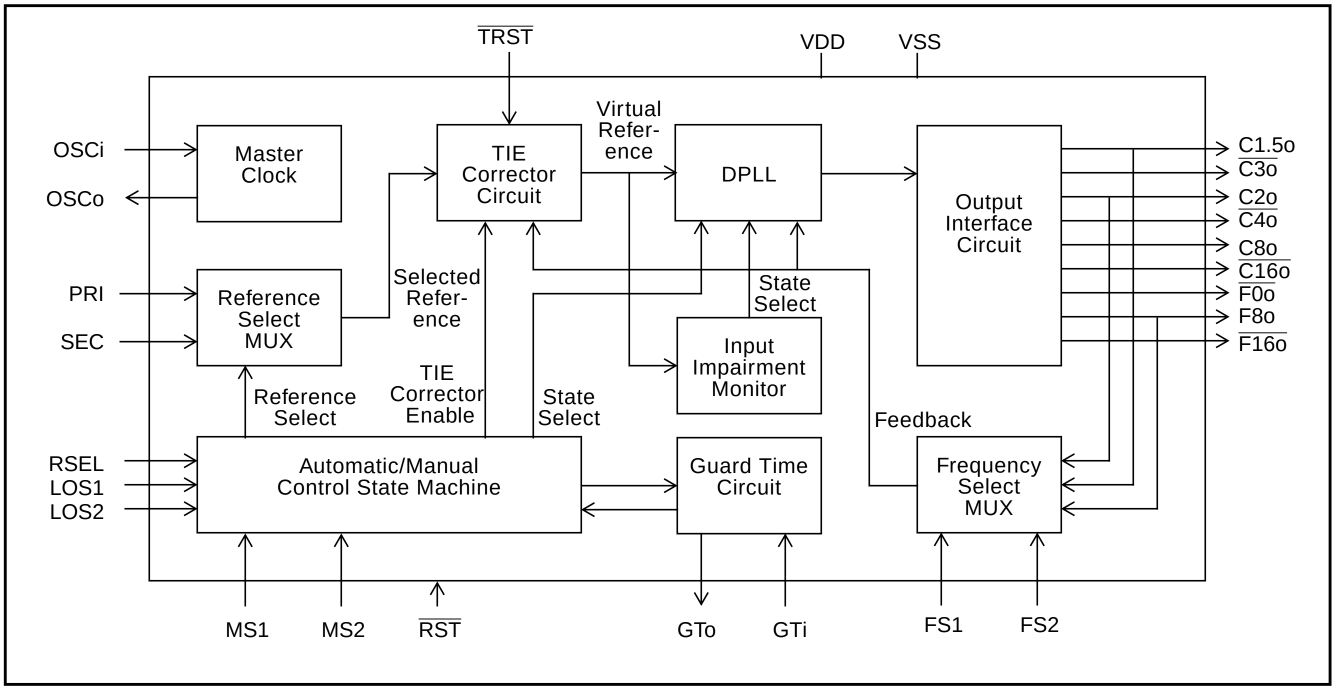


Figure 1 - Functional Block Diagram

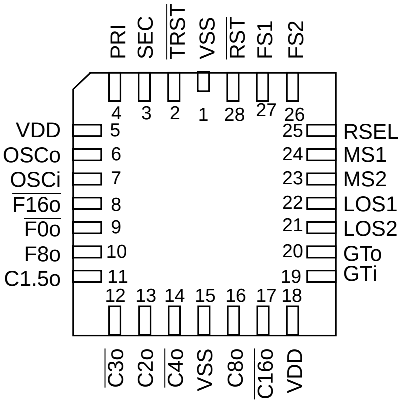


Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description (see notes 1 to 5)
1,15	V_{SS}	**Ground.** 0 Volts.
2	$\overline{\mathrm{TRST}}$	**TIE Circuit Reset (TTL Input).** A logic low at this input resets the Time Interval Error (TIE) correction circuit resulting in a re-alignment of input phase with output phase as shown in Figure 19. The $\overline{\mathrm{TRST}}$ pin should be held low for a minimum of 300ns.
3	SEC	**Secondary Reference (TTL Input).** This is one of two (PRI & SEC) input reference sources (falling edge) used for synchronization. One of three possible frequencies (8kHz, 1.544MHzMHz, or 2.048MHz) may be used. The selection of the input reference is based upon the MS1, MS2, LOS1, LOS2, RSEL, and GTi control inputs (Automatic or Manual).
4	PRI	**Primary Reference (TTL Input).** See pin description for SEC.
5,18	V_{DD}	**Positive Supply Voltage.** $+5V_{DC}$ nominal.
6	OSCo	**Oscillator Master Clock (CMOS Output).** For crystal operation, a 20MHz crystal is connected from this pin to OSCi, see Figure 10. For clock oscillator operation, this pin is left unconnected, see Figure 9.
7	OSCi	**Oscillator Master Clock (CMOS Input).** For crystal operation, a 20MHz crystal is connected from this pin to OSCo, see Figure 10. For clock oscillator operation, this pin is connected to a clock source, see Figure 9.
8	$\overline{\mathrm{F16o}}$	**Frame Pulse ST-BUS 16.384Mb/s (CMOS Output).** This is an 8kHz 61ns active low framing pulse, which marks the beginning of an ST-BUS frame. This is typically used for ST-BUS operation at 16.384Mb/s. See Figure 20.
9	$\overline{\mathrm{F0o}}$	**Frame Pulse ST-BUS 2.048Mb/s (CMOS Output).** This is an 8kHz 244ns active low framing pulse, which marks the beginning of an ST-BUS frame. This is typically used for ST-BUS operation at 2.048Mb/s and 4.096Mb/s. See Figure 20.
10	F8o	**Frame Pulse ST-BUS 8.192Mb/s (CMOS Output).** This is an 8kHz 122ns active high framing pulse, which marks the beginning of an ST-BUS frame. This is used for ST-BUS operation at 8.192Mb/s. See Figure 20.
11	C1.5o	**Clock 1.544MHz (CMOS Output).** This output is used in T1 applications.
12	$\overline{\mathrm{C3o}}$	**Clock 3.088MHz (CMOS Output).** This output is used in T1 applications.
13	C2o	**Clock 2.048MHz (CMOS Output).** This output is used for ST-BUS operation at 2.048Mb/s.
14	$\overline{\mathrm{C4o}}$	**Clock 4.096MHz (CMOS Output).** This output is used for ST-BUS operation at 2.048Mb/s and 4.096Mb/s.

Pin Description

Pin #	Name	Description (see notes 1 to 5)
16	$\overline{\text{C8o}}$	**Clock 8.192MHz (CMOS Output).** This output is used for ST-BUS operation at 8.192Mb/s.
17	$\overline{\text{C16o}}$	**Clock 16.384MHz (CMOS Output).** This output is used for ST-BUS operation at 16.384Mb/s.
19	GTi	**Guard Time (Schmitt Input).** This input is used by the MT9042B state machine in both Manual and Automatic modes. The signal at this pin affects the state changes between Primary Holdover Mode and Primary Normal Mode, and Primary Holdover Mode and Secondary Normal Mode. The logic level at this input is gated in by the rising edge of F8o. See Tables 4 and 5.
20	GTo	**Guard Time (CMOS Output).** The LOS1 input is gated by the rising edge of F8o, buffered and output on GTo. This pin is typically used to drive the GTi input through an RC circuit.
21	LOS2	**Secondary Reference Loss (TTL Input).** This input is normally connected to the loss of signal (LOS) output signal of a Line Interface Unit (LIU). When high, the SEC reference signal is lost or invalid. LOS2, along with the LOS1 and GTi inputs control the MT9042B state machine when operating in Automatic Control. The logic level at this input is gated in by the rising edge of F8o.
22	LOS1	**Primary Reference Loss (TTL Input).** Typically, external equipment applies a logic high to this input when the PRI reference signal is lost or invalid. The logic level at this input is gated in by the rising edge of F8o. See LOS2 description.
23	MS2	**Mode/Control Select 2 (TTL Input).** This input, in conjunction with MS1, determines the device's mode (Automatic or Manual) and state (Normal, Holdover or Freerun) of operation. The logic level at this input is gated in by the rising edge of F8o. See Table 3.
24	MS1	**Mode/Control Select 1 (TTL Input).** The logic level at this input is gated in by the rising edge of F8o. See pin description for MS1.
25	RSEL	**Reference Source Select (TTL Input).** In Manual Control, a logic low selects the PRI (primary) reference source as the input reference signal and a logic high selects the SEC (secondary) input. In Automatic Control, this pin must be at logic low. The logic level at this input is gated in by the rising edge of F8o. See Table 2.
26	FS2	**Frequency Select 2 (TTL Input).** This input, in conjunction with FS1, selects which of three possible frequencies (8kHz, 1.544MHz, or 2.048MHz) may be input to the PRI and SEC inputs. See Table 1.
27	FS1	**Frequency Select 1 (TTL Input).** See pin description for FS2.
28	$\overline{\text{RST}}$	**Reset (Schmitt Input).** A logic low at this input resets the MT9042B. To ensure proper operation, the device must be reset after changes to the method of control, reference signal frequency changes and power-up. The $\overline{\text{RST}}$ pin should be held low for a minimum of 300ns. While the $\overline{\text{RST}}$ pin is low, all frame and clock outputs are at logic high. Following a reset, the input reference source and output clocks and frame pulses are phase aligned as shown in Figure 19.

Notes:
1. All inputs are CMOS with either TTL compatible logic levels, CMOS compatible logic levels or Schmitt trigger compatible logic levels as indicated in the Pin Description.
2. All outputs are CMOS with CMOS compatible logic levels.
3. See DC Electrical Characteristics for static logic threshold values.
4. See AC Electrical Characteristics - Timing Parameter Measurement Voltage Levels for dynamic logic threshold values.
5. Unless otherwise stated, all unused inputs should be connected to logic high or logic low and all unused outputs should be left open circuit.

Functional Description

The MT9042C is a Multitrunk System Synchronizer, providing timing (clock) and synchronization (frame) signals to interface circuits for T1 and E1 Primary Rate Digital Transmission links.

Figure 1 is a functional block diagram which is described in the following sections.

Reference Select MUX Circuit

The MT9042C accepts two simultaneous reference input signals and operates on their falling edges. Either the primary reference (PRI) signal or the secondary reference (SEC) signal can be selected as input to the TIE Corrector Circuit. The selection is based on the Control, Mode and Reference Selection of the device. See Tables 1, 4 and 5.

Frequency Select MUX Circuit

The MT9042C operates with one of three possible input reference frequencies (8kHz, 1.544MHz or 2.048MHz). The frequency select inputs (FS1 and FS2) determine which of the three frequencies may be used at the reference inputs (PRI and SEC). Both inputs must have the same frequency applied to them. A reset ($\overline{\text{RST}}$) must be performed after every frequency select input change. Operation with FS1 and FS2 both at logic low is reserved and must not be used. See Table 1.

FS2	FS1	Input Frequency
0	0	Reserved
0	1	8kHz
1	0	1.544MHz
1	1	2.048MHz

Table 1 - Input Frequency Selection

Time Interval Error (TIE) Corrector Circuit

The TIE corrector circuit, when enabled, prevents a step change in phase on the input reference signals (PRI or SEC) from causing a step change in phase at the input of the DPLL block of Figure 1.

During reference input rearrangement, such as during a switch from the primary reference (PRI) to the secondary reference (SEC), a step change in phase on the output signals will occur. A phase step at the input of the DPLL will lead to unacceptable phase changes in the output signal.

As shown in Figure 3, the TIE Corrector Circuit receives one of the two reference (PRI or SEC) signals, passes the signal through a programmable delay line, and uses this delayed signal as an internal virtual reference, which is input to the DPLL. Therefore, the virtual reference is a delayed version of the selected reference.

During a switch, from one reference to the other, the State Machine first changes the mode of the device

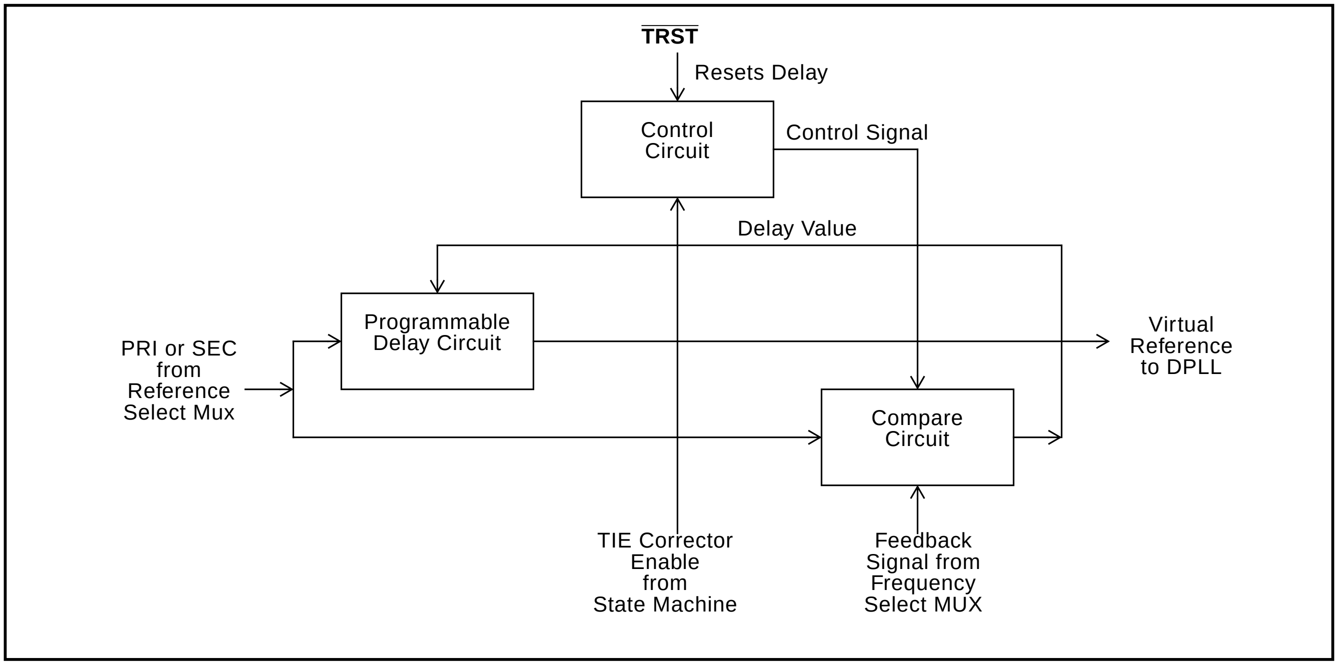


Figure 3 - TIE Corrector Circuit

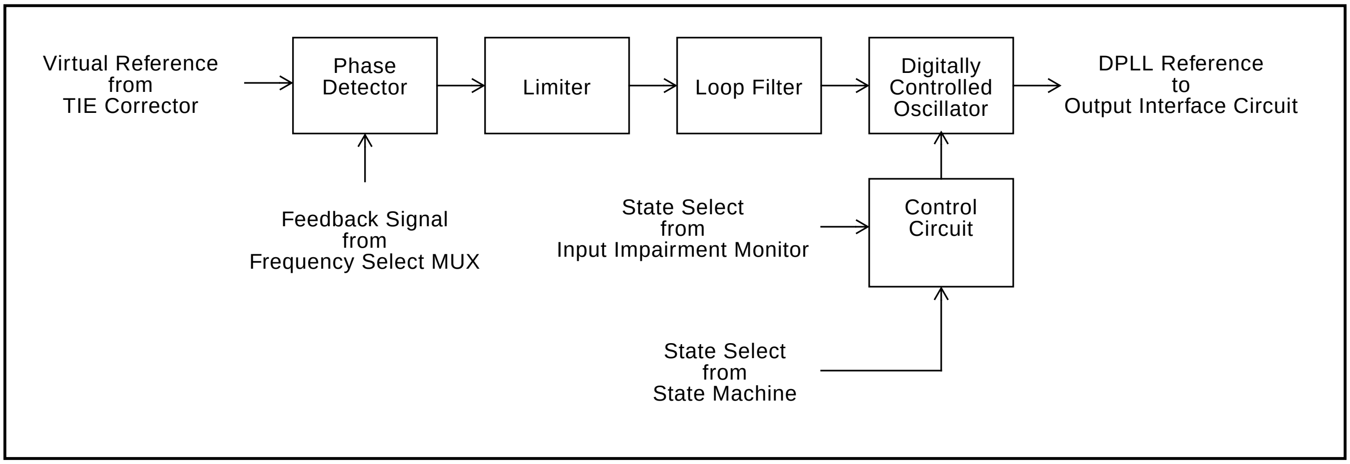


Figure 4 - DPLL Block Diagram

from Normal to Holdover. In Holdover Mode, the DPLL no longer uses the virtual reference signal, but generates an accurate clock signal using storage techniques. The Compare Circuit then measures the phase delay between the current phase (feedback signal) and the phase of the new reference signal. This delay value is passed to the Programmable Delay Circuit (See Figure 3). The new virtual reference signal is now at the same phase position as the previous reference signal would have been if the reference switch not taken place. The State Machine then returns the device to Normal Mode.

The DPLL now uses the new virtual reference signal, and since no phase step took place at the input of the DPLL, no phase step occurs at the output of the DPLL. In other words, reference switching will not create a phase change at the input of the DPLL, or at the output of the DPLL.

Since internal delay circuitry maintains the alignment between the old virtual reference and the new virtual reference, a phase error may exist between the selected input reference signal and the output signal of the DPLL. This phase error is a function of the difference in phase between the two input reference signals during reference rearrangements. Each time a reference switch is made, the delay between input signal and output signal will change. The value of this delay is the accumulation of the error measured during each reference switch.

The programmable delay circuit can be zeroed by applying a logic low pulse to the TIE Circuit Reset ($\overline{\text{TRST}}$) pin. A minimum reset pulse width is 300ns. This results in a phase alignment between the input reference signal and the output signal as shown in Figure 20. The speed of the phase alignment correction is limited to 5ns per 125us, and convergence is in the direction of least phase travel.

The state diagrams of Figure 7 and 8 indicate under which state changes the TIE Corrector Circuit is activated.

Digital Phase Lock Loop (DPLL)

As shown in Figure 4, the DPLL of the MT9042C consists of a Phase Detector, Limiter, Loop Filter, Digitally Controlled Oscillator, and a Control Circuit.

Phase Detector - the Phase Detector compares the virtual reference signal from the TIE Corrector circuit with the feedback signal from the Frequency Select MUX circuit, and provides an error signal corresponding to the phase difference between the two. This error signal is passed to the Limiter circuit. The Frequency Select MUX allows the proper feedback signal to be externally selected (e.g., 8kHz, 1.544MHz or 2.048MHz).

Limiter - the Limiter receives the error signal from the Phase Detector and ensures that the DPLL responds to all input transient conditions with a maximum output phase slope of 5ns per 125us. This is well within the maximum phase slope of 7.6ns per 125us or 81ns per 1.326ms specified by AT&T TR62411.

Loop Filter - the Loop Filter is similar to a first order low pass filter with a 1.9 Hz cutoff frequency for all three reference frequency selections (8kHz, 1.544MHz or 2.048MHz). This filter ensures that the jitter transfer requirements in ETS 300 011 and AT&T TR62411 are met.

Control Circuit - the Control Circuit uses status and control information from the State Machine and the Input Impairment Circuit to set the mode of the DPLL. The three possible modes are Normal, Holdover and Freerun.

Digitally Controlled Oscillator (DCO) - the DCO receives the limited and filtered signal from the Loop FIlter, and based on its value, generates a corresponding digital output signal. The synchronization method of the DCO is dependent on the state of the MT9042C.

In Normal Mode, the DCO provides an output signal which is frequency and phase locked to the selected input reference signal.

In Holdover Mode, the DCO is free running at a frequency equal to the last (less 30ms to 60ms) frequency the DCO was generating while in Normal Mode.

In Freerun Mode, the DCO is free running with an accuracy equal to the accuracy of the OSCi 20MHz source.

Output Interface Circuit

The output of the DCO (DPLL) is used by the Output Interface Circuit to provide the output signals shown in Figure 5. The Output Interface Circuit uses two Tapped Delay Lines followed by a T1 Divider Circuit and an E1 Divider Circuit to generate the required output signals.

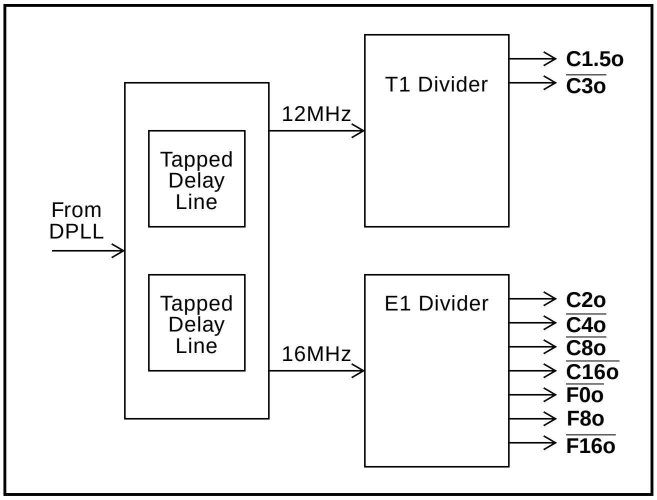


Figure 5 - Output Interface Circuit Block Diagram

Two tapped delay lines are used to generate a 16.384MHz signal and a 12.352MHz signal.

The E1 Divider Circuit uses the 16.384MHz signal to generate four clock outputs and three frame pulse outputs. The C8o, C4o and C2o clocks are generated by simply dividing the C16o clock by two, four and eight respectively. These outputs have a nominal 50% duty cycle.

The T1 Divider Circuit uses the 12.384MHz signal to generate two clock outputs. C1.5o and C3o are generated by dividing the internal C12 clock by four and eight respectively. These outputs have a nominal 50% duty cycle.

The frame pulse outputs (F0o, F8o, F16o) are generated directly from the C16 clock.

The T1 and E1 signals are generated from a common DPLL signal. Consequently, the clock outputs C1.5o, C3o, C2o, C4o, C8o, C16o, F0o and F16o are locked to one another for all operating states, and are also locked to the selected input reference in Normal Mode. See Figures 20 & 21.

All frame pulse and clock outputs have limited driving capability, and should be buffered when driving high capacitance (e.g., 30pF) loads.

Input Impairment Monitor

This circuit monitors the input signal to the DPLL and automatically enables the Holdover Mode (Auto-Holdover) when the frequency of the incoming signal is outside the auto-holdover capture range (See AC Electrical Characteristics - Performance). This includes a complete loss of incoming signal, or a large frequency shift in the incoming signal. When the incoming signal returns to normal, the DPLL is returned to Normal Mode with the output signal locked to the input signal. The holdover output signal is based on the incoming signal 30ms minimum to 60ms prior to entering the Holdover Mode. The amount of phase drift while in holdover is negligible because the Holdover Mode is very accurate (e.g., ±0.05ppm). The the Auto-Holdover circuit does not use TIE correction. Consequently, the phase delay between the input and output after switching back to Normal Mode is preserved (is the same as just prior to the switch to Auto-Holdover).

Automatic/Manual Control State Machine

The Automatic/Manual Control State Machine allows the MT9042C to be controlled automatically (i.e., LOS1, LOS2 and GTi signals) or controlled manually (i.e., MS1, MS2, GTi and RSEL signals). With manual control a single mode of operation (i.e., Normal, Holdover and Freerun) is selected. Under automatic control the state of the LOS1, LOS2 and GTi signals determines the sequence of modes that the MT9042C will follow.

As shown in Figure 1, this state machine controls the Reference Select MUX, the TIE Corrector Circuit, the

DPLL and the Guard Time Circuit. Control is based on the logic levels at the control inputs LOS1, LOS2, RSEL, MS1, MS2 and GTi of the Guard Time Circuit (See Figure 6).

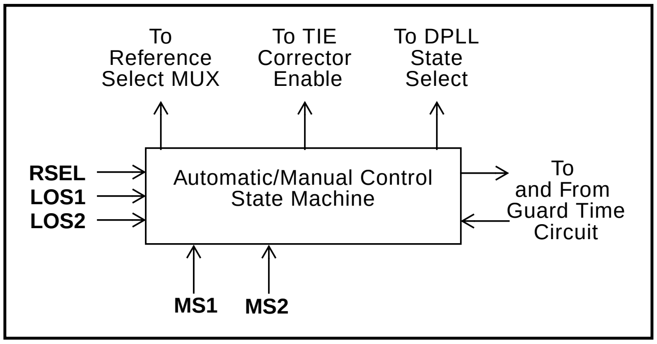


Figure 6 - Automatic/Manual Control State Machine Block Diagram

All state machine changes occur synchronously on the rising edge of F8o. See the Controls and Modes of Operation section for full details on Automatic Control and Manual Control.

Guard Time Circuit

The GTi pin is used by the Automatic/Manual Control State Machine in the MT9042C under either Manual or Automatic control. The logic level at the GTi pin performs two functions, it enables and disables the TIE Corrector Circuit (Manual and Automatic), and it selects which mode change takes place (Automatic only). See the Applications - Guard Time section.

For both Manual and Automatic control, when switching from Primary Holdover to Primary Normal, the TIE Corrector Circuit is enabled when GTi=1, and disabled when GTi=0.

Under Automatic control and in Primary Normal Mode, two state changes are possible (not counting Auto-Holdover). These are state changes to Primary Holdover or to Secondary Normal. The logic level at the GTi pin determines which state change occurs. When GTi=0, the state change is to Primary Holdover. When GTi=1, the state change is to Secondary Normal.

Master Clock

The MT9042C can use either a clock or crystal as the master timing source. For recommended master timing circuits, see the Applications - Master Clock section.

Control and Modes of Operation

The MT9042C can operate either in Manual or Automatic Control. Each control method has three possible modes of operation, Normal, Holdover and Freerun.

As shown in Table 3, Mode/Control Select pins MS2 and MS1 select the mode and method of control.

Control	RSEL	Input Reference
MANUAL	0	PRI
	1	SEC
AUTO	0	State Machine Control
	1	Reserved

Table 2 - Input Reference Selection

MS2	MS1	Control	Mode
0	0	MANUAL	NORMAL
0	1	MANUAL	HOLDOVER
1	0	MANUAL	FREERUN
1	1	AUTO	State Machine Control

Table 3 - Operating Modes and States

Manual Control

Manual Control should be used when either very simple MT9042C control is required, or when complex control is required which is not accommodated by Automatic Control. For example, very simple control could include operation in a system which only requires Normal Mode with reference switching using only a single input stimulus (RSEL). Very simple control would require no external circuitry. Complex control could include a system which requires state changes between Normal, Holdover and Freerun Modes based on numerous input stimuli. Complex control would require external circuitry, typically a microcontroller.

Under Manual Control, one of the three modes is selected by mode/control select pins MS2 and MS1. The active reference input (PRI or SEC) is selected by the RSEL pin as shown in Table 2. Refer to Table 4 and Figure 7 for details of the state change sequences.

Automatic Control

Automatic Control should be used when simple MT9042C control is required, which is more complex than the very simple control provide by Manual Control with no external circuitry, but not as complex as Manual Control with a microcontroller. For example, simple control could include operation in a system which can be accommodated by the Automatic Control State Diagram shown in Figure 8.

Automatic Control is also selected by mode/control pins MS2 and MS1. However, the mode and active reference source is selected automatically by the internal Automatic State Machine (See Figure 6). The mode and reference changes are based on the logic levels on the LOS1, LOS2 and GTi control pins. Refer to Table 5 and Figure 8 for details of the state change sequences.

Normal Mode

Normal Mode is typically used when a slave clock source, synchronized to the network is required.

In Normal Mode, the MT9042C provides timing (C1.5o, C2o, $\overline{\text{C3o}}$, $\overline{\text{C4o}}$, C8o and $\overline{\text{C16o}}$) and frame synchronization ($\overline{\text{F0o}}$, F8o, $\overline{\text{F16o}}$) signals, which are synchronized to one of two reference inputs (PRI or SEC). The input reference signal may have a nominal frequency of 8kHz, 1.544MHz or 2.048MHz.

From a reset condition, the MT9042C will take up to 25 seconds for the output signal to be phase locked to the selected reference.

The selection of input references is control dependent as shown in state tables 4 and 5. The reference frequencies are selected by the frequency control pins FS2 and FS1 as shown in Table 1.

Holdover Mode

Holdover Mode is typically used for short durations (e.g., 2 seconds) while network synchronization is temporarily disrupted.

In Holdover Mode, the MT9042C provides timing and synchronization signals, which are not locked to an external reference signal, but are based on storage techniques. The storage value is determined while the device is in Normal Mode and locked to an external reference signal.

When in Normal Mode, and locked to the input reference signal, a numerical value corresponding to the MT9042C output frequency is stored alternately in two memory locations every 30ms. When the device is switched into Holdover Mode, the value in memory from between 30ms and 60ms is used to set the output frequency of the device.

The frequency accuracy of Holdover Mode is ±0.05ppm, which translates to a worst case 35 frame (125us) slips in 24 hours. This exceeds the AT&T TR62411 Stratum 3 requirement of ±0.37ppm (255 frame slips per 24 hours).

Two factors affect the accuracy of Holdover Mode. One is drift on the Master Clock while in Holdover Mode, drift on the Master Clock directly affects the Holdover Mode accuracy. Note that the absolute Master Clock (OSCi) accuracy does not affect Holdover accuracy, only the change in OSCi accuracy while in Holdover. For example, a ±32ppm master clock may have a temperature coefficient of ±0.1ppm per degree C. So a 10 degree change in temperature, while the MT9042C is in Holdover Mode may result in an additional offset (over the ±0.05ppm) in frequency accuracy of ±1ppm. Which is much greater than the ±0.05ppm of the MT9042C.

The other factor affecting accuracy is large jitter on the reference input prior (30ms to 60ms) to the mode switch. For instance, jitter of 7.5UI at 700Hz may reduce the Holdover Mode accuracy from 0.05ppm to 0.10ppm.

Freerun Mode

Freerun Mode is typically used when a master clock source is required, or immediately following system power-up before network synchronization is achieved.

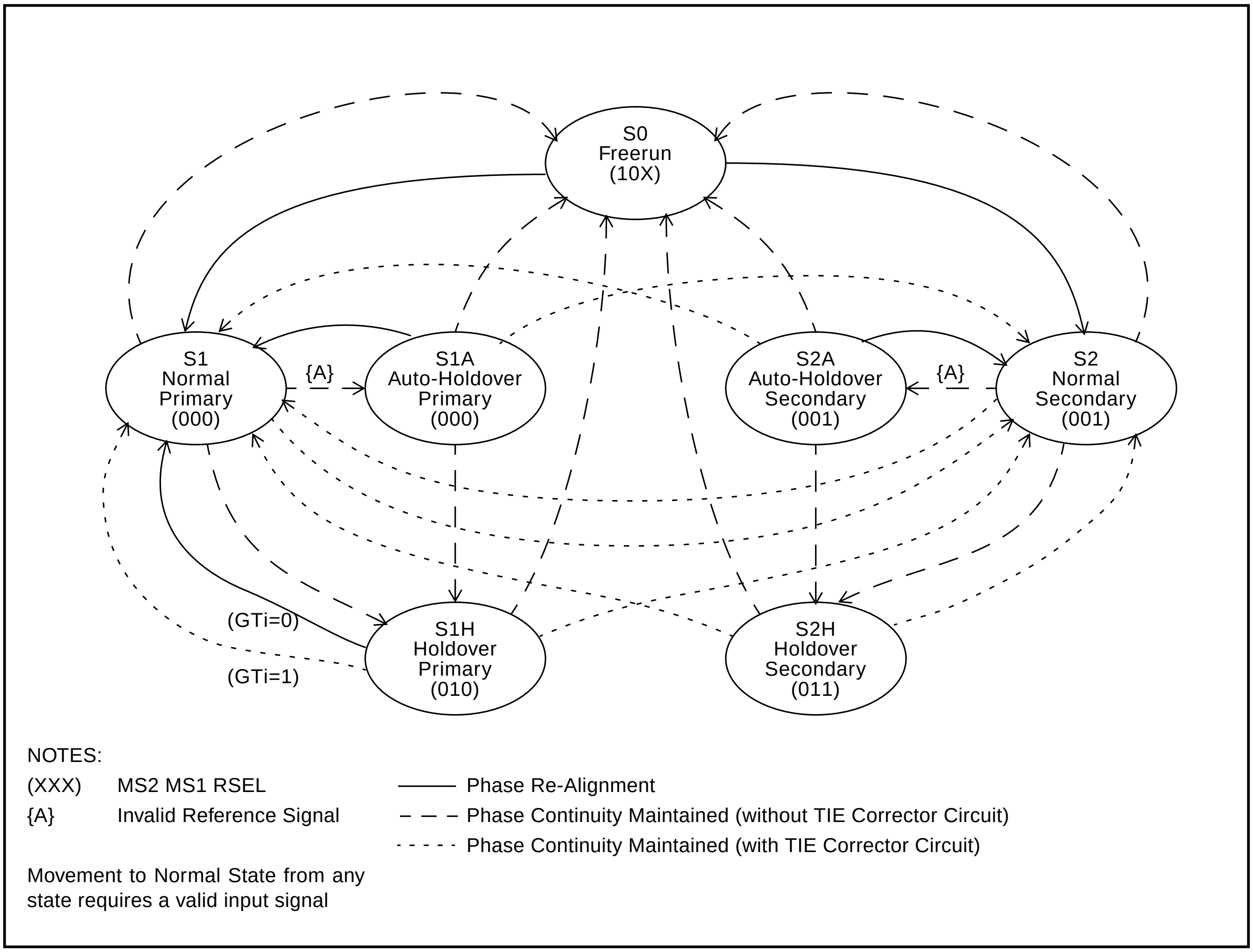
In Freerun Mode, the MT9042C provides timing and synchronization signals which are based on the master clock frequency (OSCi) only, and are not synchronized to the reference signals (PRI and SEC).

The accuracy of the output clock is equal to the accuracy of the master clock (OSCi). So if a ±32ppm output clock is required, the master clock must also be ±32ppm. See Applications - Crystal and Clock Oscillator sections.

Description				State				
Input Controls				Freerun	Normal (PRI)	Normal (SEC)	Holdover (PRI)	Holdover (SEC)
MS2	**MS1**	**RSEL**	**GTi**	**S0**	**S1**	**S2**	**S1H**	**S2H**
0	0	0	0	S1	-	S1 MTIE	S1	S1 MTIE
0	0	0	1	S1	-	S1 MTIE	S1 MTIE	S1 MTIE
0	0	1	X	S2	S2 MTIE	-	S2 MTIE	S2 MTIE
0	1	0	X	/	S1H	/	-	/
0	1	1	X	/	S2H	S2H	/	-
1	0	X	X	-	S0	S0	S0	S0

Legend:
- No Change
/ Not Valid
MTIE State change occurs with TIE Corrector Circuit
Refer to Manual Control State Diagram for state changes to and from Auto-Holdover State

Table 4 - Manual Control State Table



NOTES:
(XXX) MS2 MS1 RSEL
{A} Invalid Reference Signal

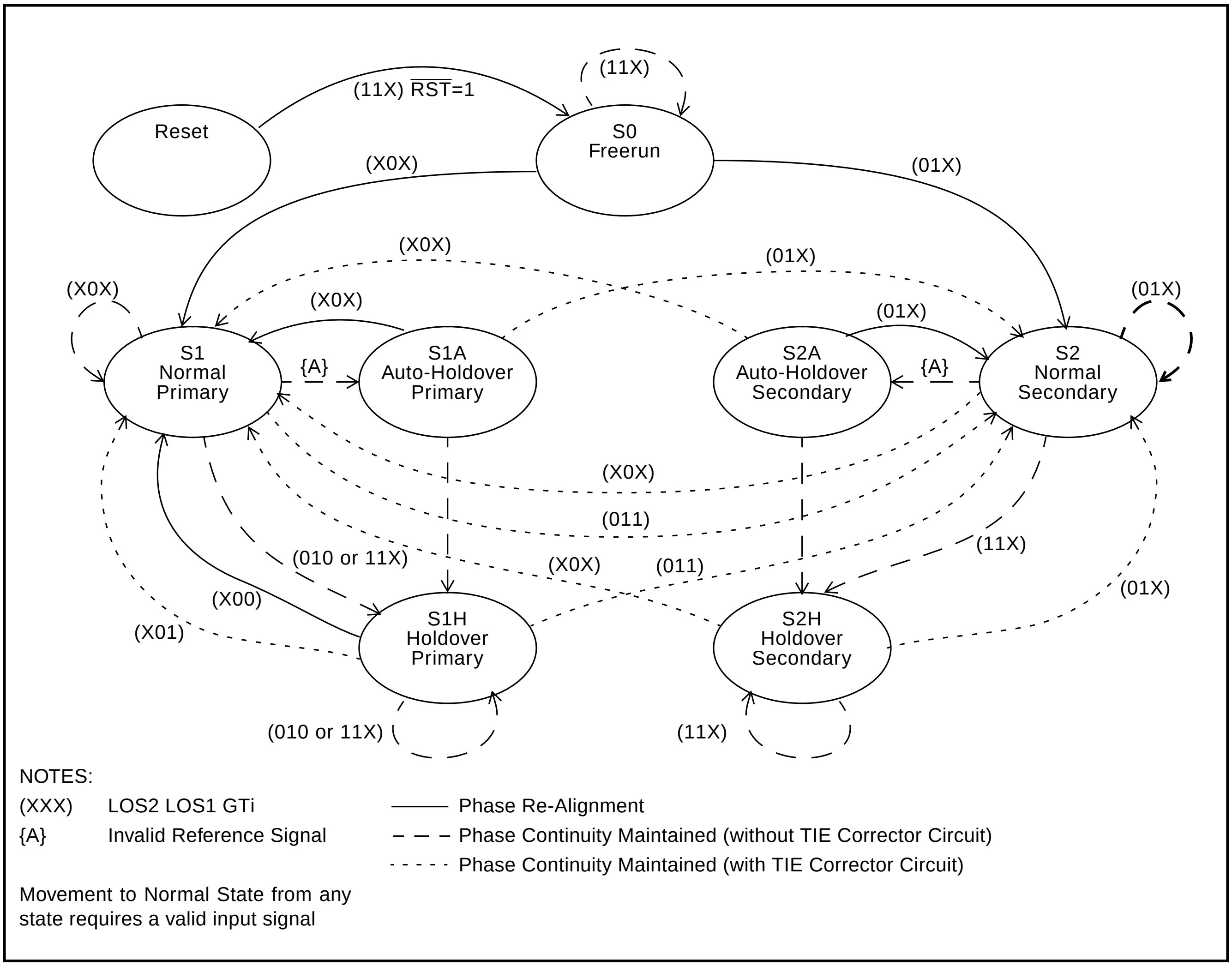
Movement to Normal State from any state requires a valid input signal

Figure 7 - Manual Control State Diagram

Description				**State**				
Input Controls				**Freerun**	**Normal (PRI)**	**Normal (SEC)**	**Holdover (PRI)**	**Holdover (SEC)**
LOS2	**LOS1**	**GTi**	**RST**	**S0**	**S1**	**S2**	**S1H**	**S2H**
1	1	X	0 to 1	-	S0	S0	S0	S0
X	0	0	1	S1	-	S1 MTIE	S1	S1 MTIE
X	0	1	1	S1	-	S1 MTIE	S1 MTIE	S1 MTIE
0	1	0	1	S1	S1H	-	-	S2 MTIE
0	1	1	1	S2	S2 MTIE	-	S2 MTIE	S2 MTIE
1	1	X	1	-	S1H	S2H	-	-

Legend:
- No Change
MTIE State change occurs with TIE Corrector Circuit
Refer to Automatic Control State Diagram for state changes to and from Auto-Holdover State

Table 5 - Automatic Control (MS1=MS2=1, RSEL=0) State Table



NOTES:
(XXX) LOS2 LOS1 GTi
{A} Invalid Reference Signal

——— Phase Re-Alignment
– – – Phase Continuity Maintained (without TIE Corrector Circuit)
- - - - Phase Continuity Maintained (with TIE Corrector Circuit)

Movement to Normal State from any state requires a valid input signal

Figure 8 - Automatic Control State Diagram

MT9042C Measures of Performance

The following are some synchronizer performance indicators and their corresponding definitions.

Intrinsic Jitter

Intrinsic jitter is the jitter produced by the synchronizing circuit and is measured at its output. It is measured by applying a reference signal with no jitter to the input of the device, and measuring its output jitter. Intrinsic jitter may also be measured when the device is in a non-synchronizing mode, such as free running or holdover, by measuring the output jitter of the device. Intrinsic jitter is usually measured with various bandlimiting filters depending on the applicable standards.

Jitter Tolerance

Jitter tolerance is a measure of the ability of a PLL to operate properly (i.e., remain in lock and or regain lock in the presence of large jitter magnitudes at various jitter frequencies) when jitter is applied to its reference. The applied jitter magnitude and jitter frequency depends on the applicable standards.

Jitter Transfer

Jitter transfer or jitter attenuation refers to the magnitude of jitter at the output of a device for a given amount of jitter at the input of the device. Input jitter is applied at various amplitudes and frequencies, and output jitter is measured with various filters depending on the applicable standards.

For the MT9042C, two internal elements determine the jitter attenuation. This includes the internal 1.9Hz low pass loop filter and the phase slope limiter. The phase slope limiter limits the output phase slope to 5ns/125us. Therefore, if the input signal exceeds this rate, such as for very large amplitude low frequency input jitter, the maximum output phase slope will be limited (i.e., attenuated) to 5ns/125us.

The MT9042C has eight outputs with three possible input frequencies for a total of 24 possible jitter transfer functions. However, the data sheet section on AC Electrical Characteristics - Jitter Transfer specifies transfer values for only three cases, 8kHz to 8kHz, 1.544MHz to 1.544MHz and 2.048MHz to 2.048MHz. Since all outputs are derived from the same signal, these transfer values apply to all outputs.

It should be noted that 1UI at 1.544MHz is 644ns, which is not equal to 1UI at 2.048MHz, which is 488ns. Consequently, a transfer value using different input and output frequencies must be calculated in common units (e.g., seconds) as shown in the following example.

What is the T1 and E1 output jitter when the T1 input jitter is 20UI (T1 UI Units) and the T1 to T1 jitter attenuation is 18dB?

$$OutputT1 = InputT1 \times 10^{\left(\frac{-A}{20}\right)}$$

$$OutputT1 = 20 \times 10^{\left(\frac{-18}{20}\right)} = 2.5UI(T1)$$

$$OutputE1 = OutputT1 \times \frac{(1UIT1)}{(1UIE1)}$$

$$OutputE1 = OutputT1 \times \frac{(644ns)}{(488ns)} = 3.3UI(T1)$$

Using the above method, the jitter attenuation can be calculated for all combinations of inputs and outputs based on the three jitter transfer functions provided.

Note that the resulting jitter transfer functions for all combinations of inputs (8kHz, 1.544MHz, 2.048MHz) and outputs (8kHz, 1.544MHz, 2.048MHz, 4.096MHz, 8.192MHz, 16.384MHz) for a given input signal (jitter frequency and jitter amplitude) are the same.

Since intrinsic jitter is always present, jitter attenuation will appear to be lower for small input jitter signals than for large ones. Consequently, accurate jitter transfer function measurements are usually made with large input jitter signals (e.g., 75% of the specified maximum jitter tolerance).

Frequency Accuracy

Frequency accuracy is defined as the absolute tolerance of an output clock signal when it is not locked to an external reference, but is operating in a free running mode. For the MT9042C, the Freerun accuracy is equal to the Master Clock (OSCi) accuracy.

Holdover Accuracy

Holdover accuracy is defined as the absolute tolerance of an output clock signal, when it is not locked to an external reference signal, but is operating using storage techniques. For the MT9042C, the storage value is determined while the device is in Normal Mode and locked to an external reference signal.

The absolute Master Clock (OSCi) accuracy of the MT9042C does not affect Holdover accuracy, but the change in OSCi accuracy while in Holdover Mode does.

Capture Range

Also referred to as pull-in range. This is the input frequency range over which the synchronizer must be able to pull into synchronization. The MT9042C capture range is equal to ±230ppm minus the accuracy of the master clock (OSCi). For example, a ±32ppm master clock results in a capture range of ±198ppm.

Lock Range

This is the input frequency range over which the synchronizer must be able to maintain synchronization. The lock range is equal to the capture range for the MT9042C.

Phase Slope

Phase slope is measured in seconds per second and is the rate at which a given signal changes phase with respect to an ideal signal. The given signal is typically the output signal. The ideal signal is of constant frequency and is nominally equal to the value of the final output signal or final input signal.

Time Interval Error (TIE)

TIE is the time delay between a given timing signal and an ideal timing signal.

Maximum Time Interval Error (MTIE)

MTIE is the maximum peak to peak delay between a given timing signal and an ideal timing signal within a particular observation period.

$$MTIE(S) = TIEmax(t) - TIEmin(t)$$

Phase Continuity

Phase continuity is the phase difference between a given timing signal and an ideal timing signal at the end of a particular observation period. Usually, the given timing signal and the ideal timing signal are of the same frequency. Phase continuity applies to the output of the synchronizer after a signal disturbance due to a reference switch or a mode change. The observation period is usually the time from the disturbance, to just after the synchronizer has settled to a steady state.

In the case of the MT9042C, the output signal phase continuity is maintained to within ±5ns at the instance (over one frame) of all reference switches and all mode changes. The total phase shift, depending on the switch or type of mode change, may accumulate up to ±200ns over many frames. The rate of change of the ±200ns phase shift is limited to a maximum phase slope of approximately 5ns/125us. This meets the AT&T TR62411 maximum phase slope requirement of 7.6ns/125us (81ns/1.326ms).

Phase Lock Time

This is the time it takes the synchronizer to phase lock to the input signal. Phase lock occurs when the input signal and output signal are not changing in phase with respect to each other (not including jitter).

Lock time is very difficult to determine because it is affected by many factors which include:

i) initial input to output phase difference
ii) initial input to output frequency difference
iii) synchronizer loop filter
iv) synchronizer limiter

Although a short lock time is desirable, it is not always possible to achieve due to other synchronizer requirements. For instance, better jitter transfer performance is achieved with a lower frequency loop filter which increases lock time. And better (smaller) phase slope performance (limiter) results in longer lock times. The MT9042C loop filter and limiter were optimized to meet the AT&T TR62411 jitter transfer and phase slope requirements. Consequently, phase lock time, which is not a standards requirement, may be longer than in other applications. See AC Electrical Characteristics - Performance for maximum phase lock time.

MT9042C and Network Specifications

The MT9042C fully meets all applicable PLL requirements (intrinsic jitter, jitter tolerance, jitter transfer, frequency accuracy, holdover accuracy, capture range, phase change slope and MTIE during reference rearrangement) for the following specifications.

1. AT&T TR62411 (DS1) December 1990 for Stratum 3, Stratum 4 Enhanced and Stratum 4
2. ANSI T1.101 (DS1) February 1994 for Stratum 3, Stratum 4 Enhanced and Stratum 4
3. ETSI 300 011 (E1) April 1992 for Single Access and Multi Access
4. TBR 4 November 1995
5. TBR 12 December 1993
6. TBR 13 January 1996
7. ITU-T I.431 March 1993

Applications

This section contains MT9042C application specific details for clock and crystal operation, guard time usage, reset operation, power supply decoupling, Manual Control operation and Automatic Control operation.

Master Clock

The MT9042C can use either a clock or crystal as the master timing source.

In Freerun Mode, the frequency tolerance at the clock outputs is identical to the frequency tolerance of the source at the OSCi pin. For applications not requiring an accurate Freerun Mode, tolerance of the master timing source may be ±100ppm. For applications requiring an accurate Freerun Mode, such as AT&T TR62411, the tolerance of the master timing source must Be no greater than ±32ppm.

Another consideration in determining the accuracy of the master timing source is the desired capture range. The sum of the accuracy of the master timing source and the capture range of the MT9042C will always equal ±230ppm. For example, if the master timing source is ±100ppm, then the capture range will be ±130ppm.

Clock Oscillator - when selecting a Clock Oscillator, numerous parameters must be considered. This includes absolute frequency, frequency change over temperature, output rise and fall times, output levels and duty cycle. See AC Electrical Characteristics.

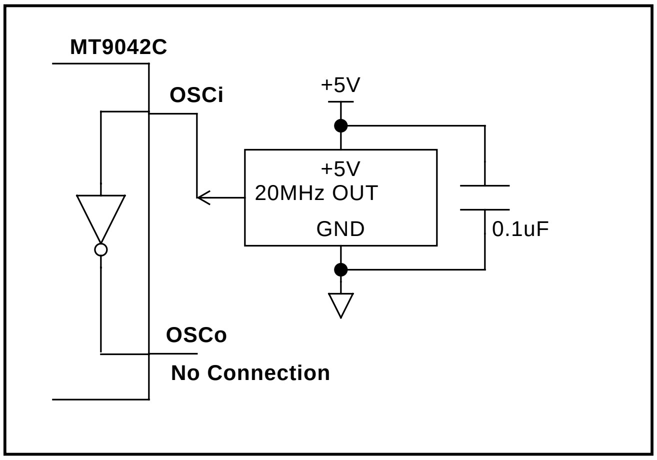


Figure 9 - Clock Oscillator Circuit

For applications requiring ±32ppm clock accuracy, the following clock oscillator module may be used.

CTS CXO-65-HG-5-C-20.0MHz

Frequency:	*20MHz*
Tolerance:	*25ppm 0C to 70C*
Rise & Fall Time:	*8ns (0.5V 4.5V 50pF)*
Duty Cycle:	*45% to 55%*

The output clock should be connected directly (not AC coupled) to the OSCi input of the MT9042C, and the OSCo output should be left open as shown in Figure 9.

Crystal Oscillator - Alternatively, a Crystal Oscillator may be used. A complete oscillator circuit made up of a crystal, resistor and capacitors is shown in Figure 10.

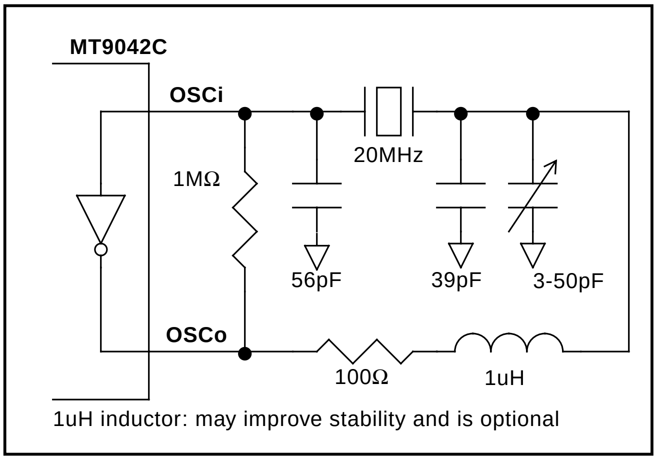


Figure 10 - Crystal Oscillator Circuit

The accuracy of a crystal oscillator depends on the crystal tolerance as well as the load capacitance tolerance. Typically, for a 20MHz crystal specified with a 32pF load capacitance, each 1pF change in load capacitance contributes approximately 9ppm to the frequency deviation. Consequently, capacitor tolerances, and stray capacitances have a major effect on the accuracy of the oscillator frequency.

The trimmer capacitor shown in Figure 10 may be used to compensate for capacitive effects. If accuracy is not a concern, then the trimmer may be removed, the 39pF capacitor may be increased to 56pF, and a wider tolerance crystal may be substituted.

The crystal should be a fundamental mode type - not an overtone. The fundamental mode crystal permits a simpler oscillator circuit with no additional filter components and is less likely to generate spurious responses. The crystal specification is as follows.

Frequency:	*20MHz*
Tolerance:	*As required*
Oscillation Mode:	*Fundamental*
Resonance Mode:	*Parallel*
Load Capacitance:	*32pF*
Maximum Series Resistance:	*35Ω*
Approximate Drive Level:	*1mW*

e.g., CTS R1027-2BB-20.0MHZ

(±20ppm absolute, ±6ppm 0C to 50C, 32pF, 25Ω)

Guard Time Adjustment

AT&T TR62411 recommends that excessive switching of the timing reference should be minimized. And that switching between references only be performed when the primary signal is degraded (e.g., error bursts of 2.5 seconds).

Minimizing switching (from PRI to SEC) in the MT9042C can be realized by first entering Holdover Mode for a predetermined maximum time (i.e., guard time). If the degraded signal returns to normal before the expiry of the guard time (e.g., 2.5 seconds), then the MT9042C is returned to its Normal Mode (with no reference switch taking place). Otherwise, the reference input may be changed from Primary to Secondary.

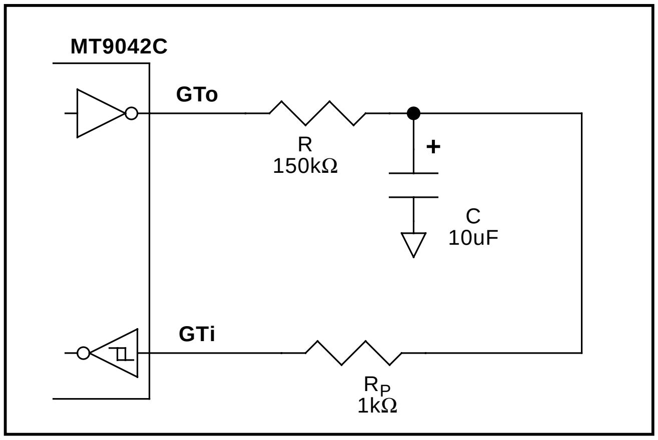


Figure 11 - Symmetrical Guard Time Circuit

A simple way to control the guard time (using Automatic Control) is with an RC circuit as shown in Figure 11. Resistor R_P is for protection only and limits the current flowing into the GTi pin during power down conditions. The guard time can be calculated as follows.

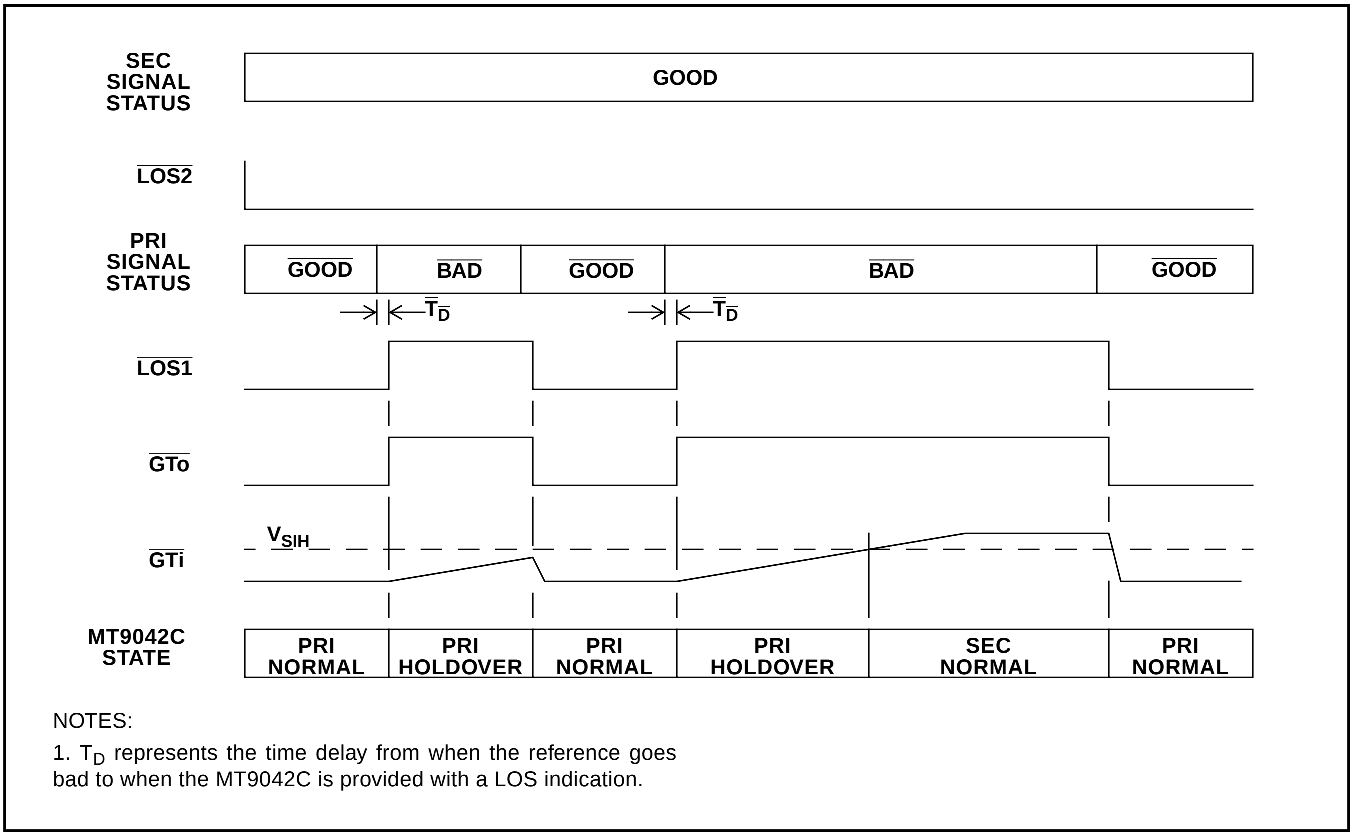
$$guard_{time} = RC \times \ln\left(\frac{V_{DD}}{V_{DD} - V_{SIH}}\right)$$

$$guard_{time} \approx RC \times 0.6$$

example

$$guard_{time} \approx 150k \times 10u \times 0.6 = 0.9s$$

- *V_{SIH} is the logic high going threshold level for the GTi Schmitt Trigger input, see DC Electrical Characteristics*



NOTES:

1. T_D represents the time delay from when the reference goes bad to when the MT9042C is provided with a LOS indication.

Figure 12 - Automatic Control, Unsymmetrical Guard Time Circuit Timing Example

In cases where fast toggling might be expected of the LOS1 input, then an unsymmetrical Guard Time Circuit is recommended. This ensures that reference switching doesn't occur until the full guard time value has expired. An unsymmetrical Guard Time Circuit is shown in Figure 12.

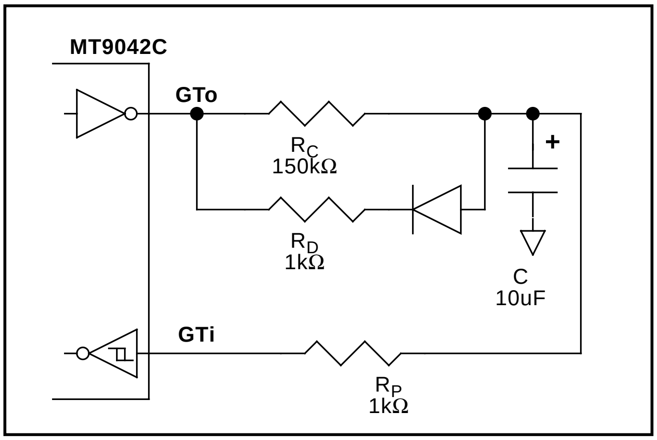


Figure 13 - Unsymmetrical Guard Time Circuit

Figure 13 shows a typical timing example of an unsymmetrical Guard Time Circuit with the MT9042C in Automatic Control.

TIE Correction (using GTi)

When Primary Holdover Mode is entered for short time periods, TIE correction should not be enabled. This will prevent unwanted accumulated phase change between the input and output. This is mainly applicable to Manual Control, since Automatic Control together with the Guard Time Circuit inherently operate in this manner.

For instance, 10 Normal to Holdover to Normal mode change sequences occur, and in each case Holdover was entered for 2s. Each mode change sequence could account for a phase change as large as 350ns. Thus, the accumulated phase change could be as large as 3.5us, and, the overall MTIE could be as large as 3.5us.

$$Phase_{hold} = 0.05ppm \times 2s = 100ns$$

$$Phase_{state} = 50ns + 200ns = 250ns$$

$$Phase_{10} = 10 \times (250ns + 100ns) = 3.5us$$

- *0.05ppm is the accuracy of Holdover Mode*
- *50ns is the maximum phase continuity of the MT9042C from Normal Mode to Holdover Mode*
- *200ns is the maximum phase continuity of the MT9042C from Holdover Mode to Normal Mode (with or without TIE Corrector Circuit)*

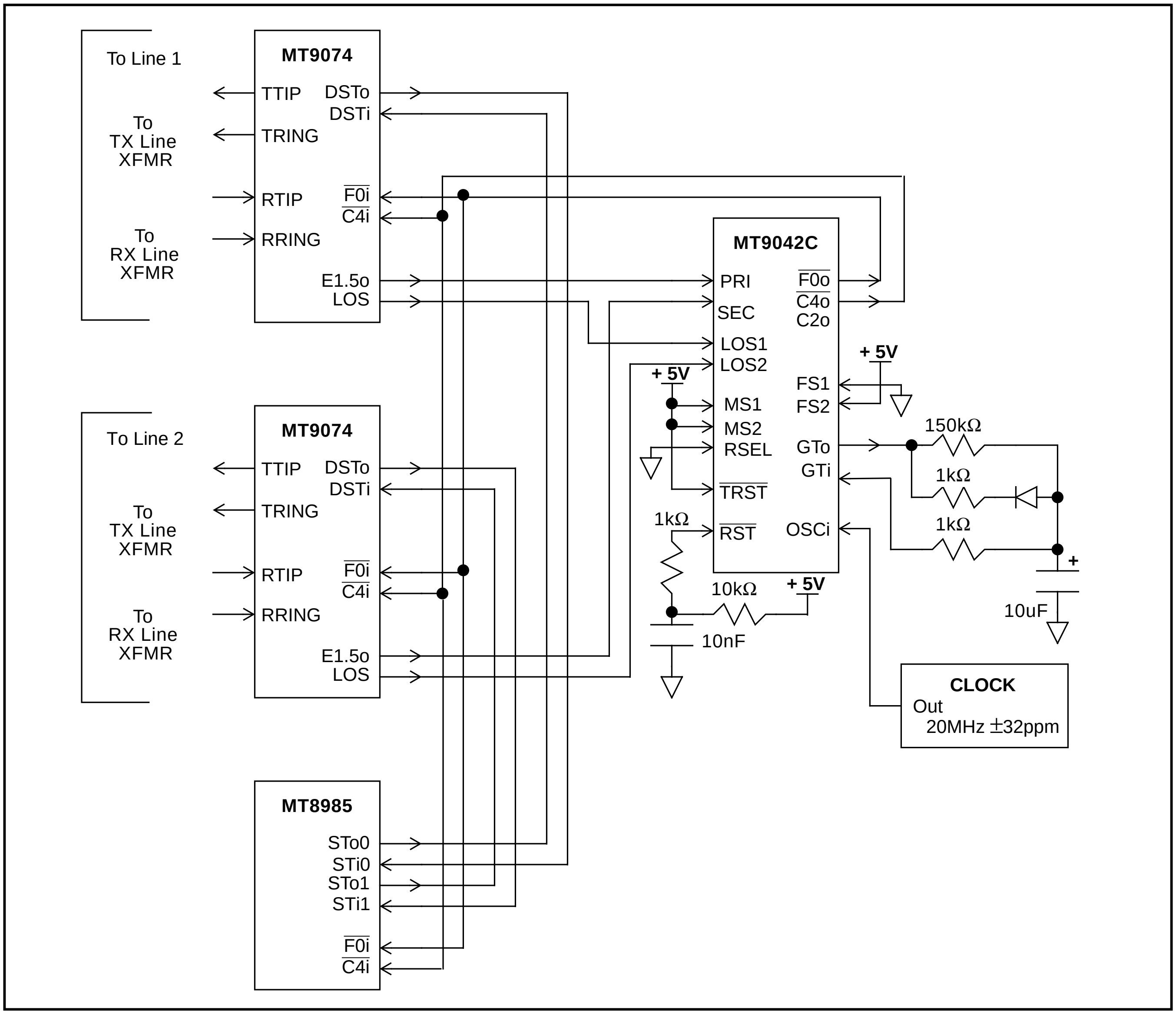


Figure 14 - Dual T1 Reference Sources with MT9042C in 1.544MHz Automatic Control

When 10 Normal to Holdover to Normal mode change sequences occur without MTIE enabled, and in each case holdover was entered for 2s, each mode change sequence could still account for a phase change as large as 350ns. However, there would be no accumulated phase change, since the input to output phase is re-aligned after every Holdover to Normal state change. The overall MTIE would only be 350ns.

Reset Circuit

A simple power up reset circuit with about a 50us reset low time is shown in Figure 15. Resistor R_P is for protection only and limits current into the $\overline{RST}$ pin during power down conditions. The reset low time is not critical but should be greater than 300ns.

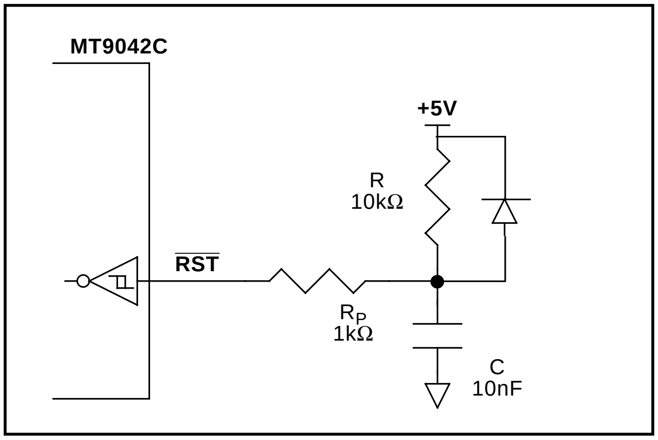


Figure 15 - Power-Up Reset Circuit

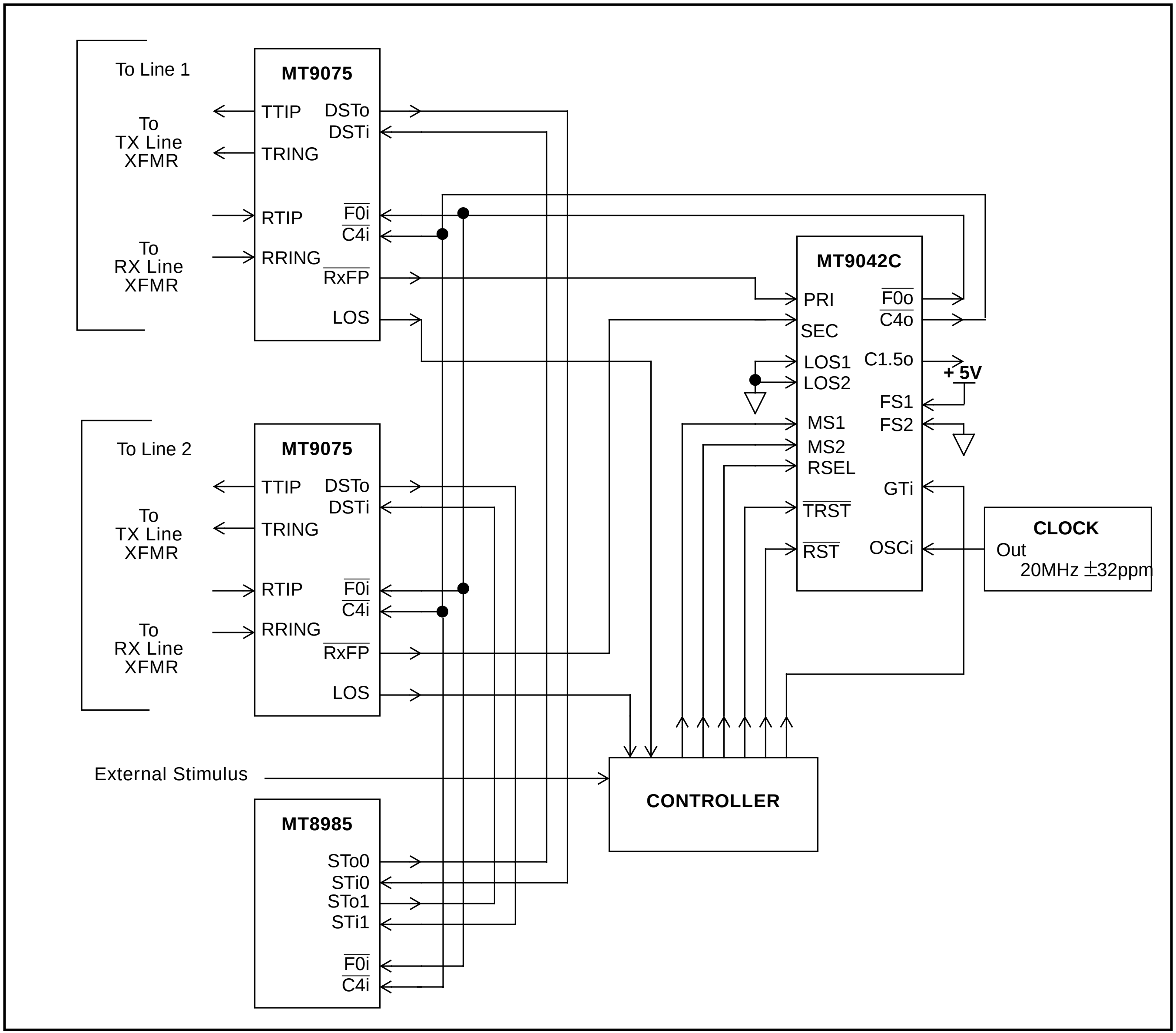


Figure 16 - Dual E1 Reference Sources with MT9042C in 8kHz Manual Control

Power Supply Decoupling

The MT9042C has two VDD (+5V) pins and two VSS (GND) pins. Power and decoupling capacitors should be included as shown in Figure 17.

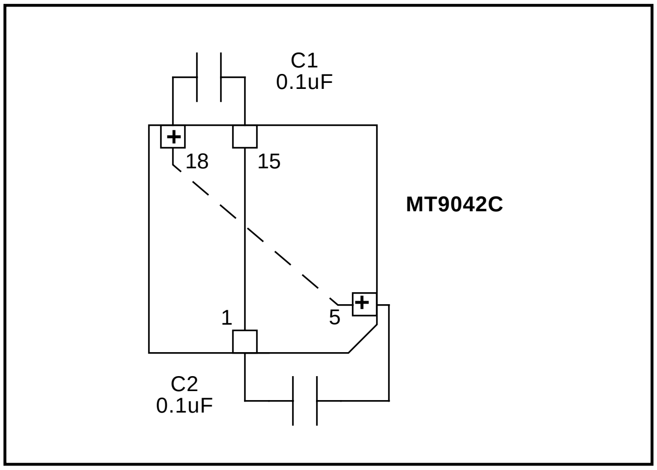


Figure 17 - Power Supply Decoupling

Absolute Maximum Ratings* - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Symbol	Min	Max	Units
1	Supply voltage	V_{DD}	-0.3	7.0	V
2	Voltage on any pin	V_{PIN}	-0.3	V_{DD}+0.3	V
3	Current on any pin	I_{PIN}		20	mA
4	Storage temperature	T_{ST}	-55	125	°C
5	PLCC package power dissipation	P_{PD}		900	mW

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions* - * Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Max	Units
1	Supply voltage	V_{DD}	4.5	5.5	V
2	Operating temperature	T_A	-40	85	C

DC Electrical Characteristics* - * Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Max	Units	Conditions/Notes
1	Supply current with: OSCi = 0V	I_{DDS}		10	mA	Outputs unloaded
2	OSCi = Clock	I_{DD}		60	mA	Outputs unloaded
3	TTL high-level input voltage	V_{IH}	2.0		V	
4	TTL low-level input voltage	V_{IL}		0.8	V	
5	CMOS high-level input voltage	V_{CIH}	0.7V_{DD}		V	OSCi
6	CMOS low-level input voltage	V_{CIL}		0.3V_{DD}	V	OSCi
7	Schmitt high-level input voltage	V_{SIH}	2.3		V	GTi, $\overline{RST}$
8	Schmitt low-level input voltage	V_{SIL}		0.8	V	GTi, $\overline{RST}$
9	Schmitt hysteresis voltage	V_{HYS}	0.4		V	GTi, $\overline{RST}$
10	Input leakage current	I_{IL}	-10	+10	uA	V_I=V_{DD} or 0V
11	High-level output voltage	V_{OH}	0.8V_{DD}		V	I_{OH}=4mA
12	Low-level output voltage	V_{OL}		0.2V_{DD}	V	I_{OL}=4mA

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

AC Electrical Characteristics - Performance

	Characteristics		Sym	Min	Max	Units	Conditions/Notes†
1	Freerun Mode accuracy with OSCi at:	±0ppm		-0	+0	ppm	5-8
2		±32ppm		-32	+32	ppm	5-8
3		±100ppm		-100	+100	ppm	5-8
4	Holdover Mode accuracy with OSCi at:	±0ppm		-0.05	+0.05	ppm	1,2,4,6-8,40
5		±32ppm		-0.05	+0.05	ppm	1,2,4,6-8,40
6		±100ppm		-0.05	+0.05	ppm	1,2,4,6-8,40
7	Capture range with OSCi at:	±0ppm		-230	+230	ppm	1-3,6-8
8		±32ppm		-198	+198	ppm	1-3,6-8
9		±100ppm		-130	+130	ppm	1-3,6-8
10	Phase lock time				30	s	1-3,6-14
11	Output phase continuity with:	reference switch			200	ns	1-3,6-14
12		mode switch to Normal			200	ns	1-2,4-14
13		mode switch to Freerun			200	ns	1-,4,6-14
14		mode switch to Holdover			50	ns	1-3,6-14
15	MTIE (maximum time interval error)				600	ns	1-14,27
16	Output phase slope				45	us/s	1-14,27
17	Reference input for Auto-Holdover with:	8kHz		-18k	+18k	ppm	1-3,6,9-11
18		1.544MHz		-36k	+36k	ppm	1-3,7,9-11
19		2.048MHz		-36k	+36k	ppm	1-3,8-11

† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - Timing Parameter Measurement Voltage Levels* - Voltages are with respect to ground (VSS) unless otherwise stated.

	Characteristics	Sym	Schmitt	TTL	CMOS	Units
1	Threshold Voltage	V_T	1.5	1.5	$0.5V_{DD}$	V
2	Rise and Fall Threshold Voltage High	V_{HM}	2.3	2.0	$0.7V_{DD}$	V
3	Rise and Fall Threshold Voltage Low	V_{LM}	0.8	0.8	$0.3V_{DD}$	V

* Supply voltage and operating temperature are as per Recommended Operating Conditions.
* Timing for input and output signals is based on the worst case result of the combination of TTL and CMOS thresholds.
* See Figure 18.

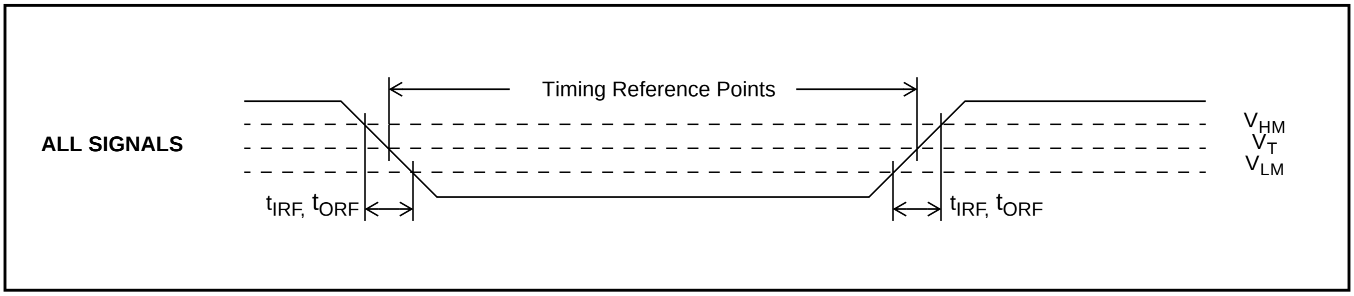
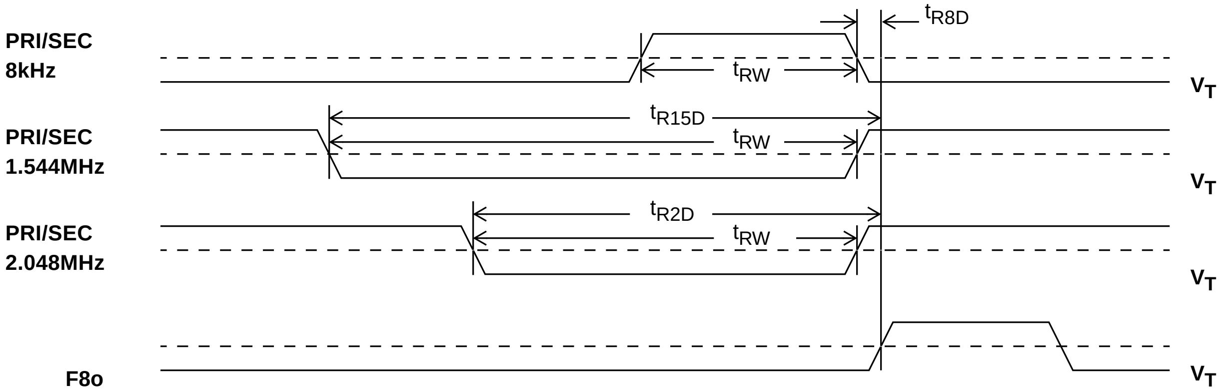


Figure 18 - Timing Parameter Measurement Voltage Levels

AC Electrical Characteristics - Input/Output Timing

	Characteristics	Sym	Min	Max	Units
1	Reference input pulse width high or low	t_{RW}	100		ns
2	Reference input rise or fall time	t_{IRF}		10	ns
3	8kHz reference input to F8o delay	t_{R8D}	-21	6	ns
4	1.544MHz reference input to F8o delay	t_{R15D}	337	363	ns
5	2.048MHz reference input to F8o delay	t_{R2D}	222	238	ns
6	F8o to $\overline{\text{F0o}}$ delay	t_{F0D}	110	134	ns
7	$\overline{\text{F16o}}$ setup to $\overline{\text{C16o}}$ falling	t_{F16S}	11	35	ns
8	$\overline{\text{F16o}}$ hold from $\overline{\text{C16o}}$ rising	t_{F16H}	0	20	ns
9	F8o to C1.5o delay	t_{C15D}	-51	-37	ns
10	F8o to $\overline{\text{C3o}}$ delay	t_{C3D}	-51	-37	ns
11	F8o to C2o delay	t_{C2D}	-13	2	ns
12	F8o to $\overline{\text{C4o}}$ delay	t_{C4D}	-13	2	ns
13	F8o to C8o delay	t_{C8D}	-13	2	ns
14	F8o to $\overline{\text{C16o}}$ delay	t_{C16D}	-13	2	ns
15	C1.5o pulse width high or low	t_{C15W}	309	339	ns
16	$\overline{\text{C3o}}$ pulse width high or low	t_{C3W}	149	175	ns
17	C2o pulse width high or low	t_{C2W}	230	258	ns
18	$\overline{\text{C4o}}$ pulse width high or low	t_{C4W}	111	133	ns
19	C8o pulse width high or low	t_{C8W}	52	70	ns
20	$\overline{\text{C16o}}$ pulse width high or low	t_{C16WL}	24	35	ns
21	$\overline{\text{F0o}}$ pulse width low	t_{F0WL}	230	258	ns
22	F8o pulse width high	t_{F8WH}	111	133	ns
23	$\overline{\text{F16o}}$ pulse width low	t_{F16WL}	52	70	ns
24	Output clock and frame pulse rise or fall time	t_{ORF}		9	ns
25	Input Controls Setup Time	t_S	100		ns
26	Input Controls Hold Time	t_H	100		ns

† See "Notes" following AC Electrical Characteristics tables.



NOTES:

1. Input to output delay values are valid after a $\overline{\text{TRST}}$ or $\overline{\text{RST}}$ with no further state changes

Figure 19 - Input to Output Timing (Normal Mode)

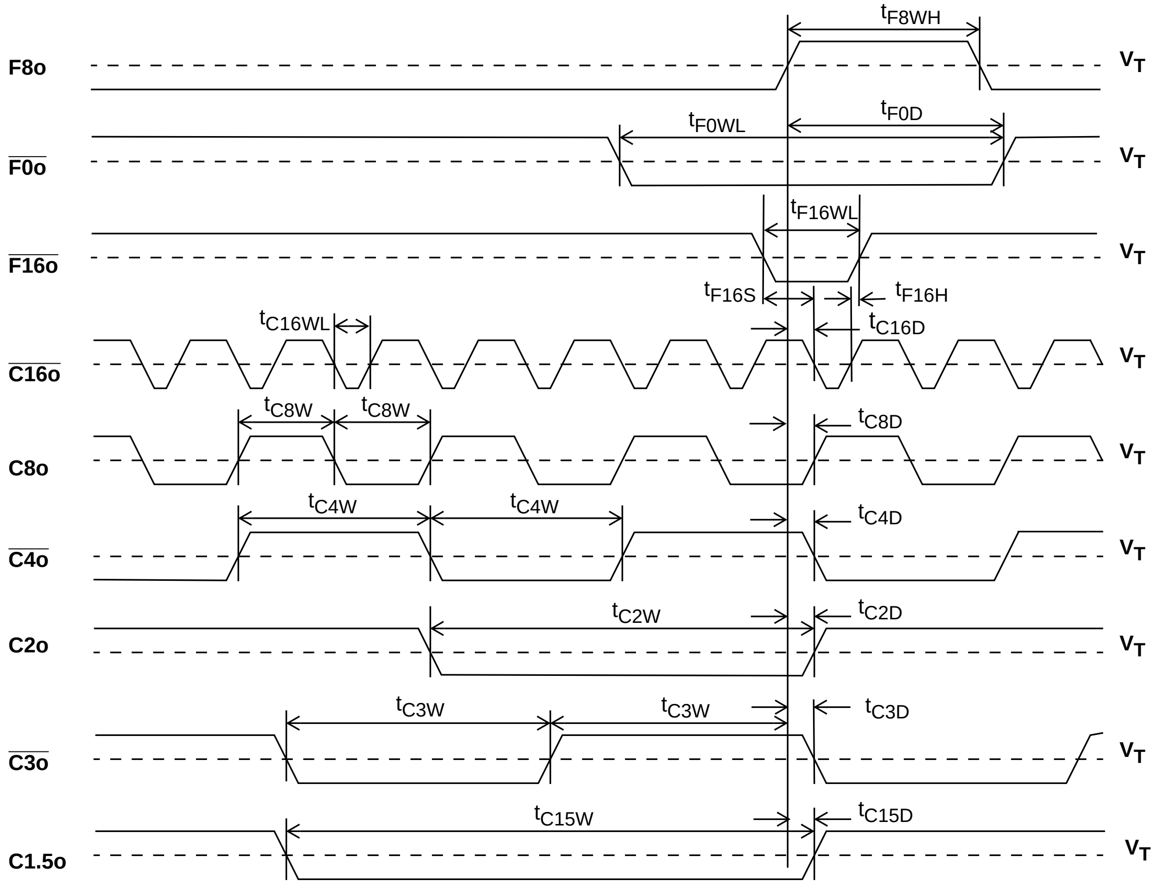


Figure 20 - Output Timing 1

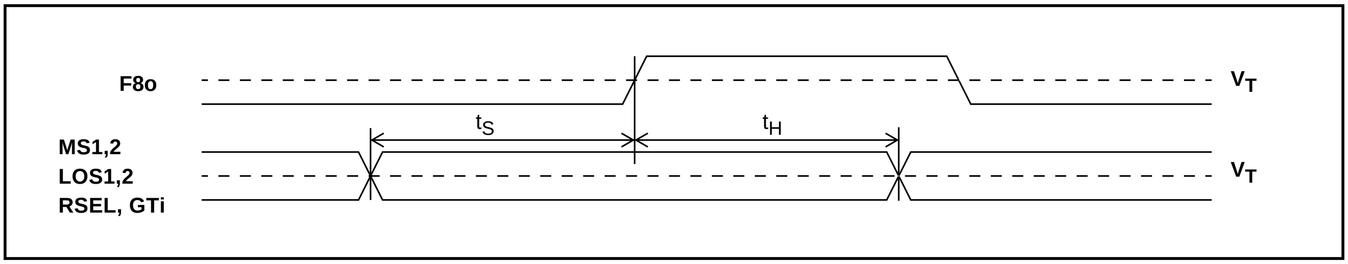


Figure 21 - Input Controls Setup and Hold Timing

AC Electrical Characteristics - Intrinsic Jitter Unfiltered

	Characteristics	Sym	Min	Max	Units	Conditions/Notes†
1	Intrinsic jitter at F8o (8kHz)			0.0002	UIpp	1-14,21-24,28
2	Intrinsic jitter at $\overline{\text{F0o}}$ (8kHz)			0.0002	UIpp	1-14,21-24,28
3	Intrinsic jitter at $\overline{\text{F16o}}$ (8kHz)			0.0002	UIpp	1-14,21-24,28
4	Intrinsic jitter at C1.5o (1.544MHz)			0.030	UIpp	1-14,21-24,29
5	Intrinsic jitter at C2o (2.048MHz)			0.040	UIpp	1-14,21-24,30
6	Intrinsic jitter at $\overline{\text{C3o}}$ (3.088MHz)			0.060	UIpp	1-14,21-24,31
7	Intrinsic jitter at $\overline{\text{C4o}}$ (4.096MHz)			0.080	UIpp	1-14,21-24,32
8	Intrinsic jitter at C8o (8.192MHz)			0.160	UIpp	1-14,21-24,33
9	Intrinsic jitter at $\overline{\text{C16o}}$ (16.384MHz)			0.320	UIpp	1-14,21-24,34

† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - C1.5o (1.544MHz) Intrinsic Jitter Filtered

	Characteristics	Sym	Min	Max	Units	Conditions/Notes†
1	Intrinsic jitter (4Hz to 100kHz filter)			0.015	UIpp	1-14,21-24,29
2	Intrinsic jitter (10Hz to 40kHz filter)			0.010	UIpp	1-14,21-24,29
3	Intrinsic jitter (8kHz to 40kHz filter)			0.010	UIpp	1-14,21-24,29
4	Intrinsic jitter (10Hz to 8kHz filter)			0.005	UIpp	1-14,21-24,29

† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - C2o (2.048MHz) Intrinsic Jitter Filtered

	Characteristics	Sym	Min	Max	Units	Conditions/Notes†
1	Intrinsic jitter (4Hz to 100kHz filter)			0.015	UIpp	1-14,21-24,30
2	Intrinsic jitter (10Hz to 40kHz filter)			0.010	UIpp	1-14,21-24,30
3	Intrinsic jitter (8kHz to 40kHz filter)			0.010	UIpp	1-14,21-24,30
4	Intrinsic jitter (10Hz to 8kHz filter)			0.005	UIpp	1-14,21-24,30

† See "Notes" following AC Electrical Characteristics tables

AC Electrical Characteristics - 8kHz Input to 8kHz Output Jitter Transfer

	Characteristics	Sym	Min	Max	Units	Conditions/Notes†
1	Jitter attenuation for 1Hz@0.01UIpp input		0	6	dB	1-3,6,9-14,21-22,24,28,35
2	Jitter attenuation for 1Hz@0.54UIpp input		6	16	dB	1-3,6,9-14,21-22,24,28,35
3	Jitter attenuation for 10Hz@0.10UIpp input		12	22	dB	1-3,6,9-14,21-22,24,28,35
4	Jitter attenuation for 60Hz@0.10UIpp input		28	38	dB	1-3,6,9-14,21-22,24,28,35
5	Jitter attenuation for 300Hz@0.10UIpp input		42		dB	1-3,6,9-14,21-22,24,28,35
6	Jitter attenuation for 3600Hz@0.005UIpp input		45		dB	1-3,6,9-14,21-22,24,28,35

† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - 1.544MHz Input to 1.544MHz Output Jitter Transfer

	Characteristics	Sym	Min	Max	Units	Conditions/Notes†
1	Jitter attenuation for 1Hz@20UIpp input		0	6	dB	1-3,7,9-14,21-22,24,29,35
2	Jitter attenuation for 1Hz@104UIpp input		6	16	dB	1-3,7,9-14,21-22,24,29,35
3	Jitter attenuation for 10Hz@20UIpp input		12	22	dB	1-3,7,9-14,21-22,24,29,35
4	Jitter attenuation for 60Hz@20UIpp input		28	38	dB	1-3,7,9-14,21-22,24,29,35
5	Jitter attenuation for 300Hz@20UIpp input		42		dB	1-3,7,9-14,21-22,24,29,35
6	Jitter attenuation for 10kHz@0.3UIpp input		45		dB	1-3,7,9-14,21-22,24,29,35
7	Jitter attenuation for 100kHz@0.3UIpp input		45		dB	1-3,7,9-14,21-22,24,29,35

† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - 2.048MHz Input to 2.048 MHz Output Jitter Transfer

	Characteristics	Sym	Min	Max	Units	Conditions/Notes†
1	Jitter at output for 1Hz@3.00UIpp input			2.9	UIpp	1-3,8,9-14,21-22,24,30,35
2	with 40Hz to 100kHz filter			0.09	UIpp	1-3,8,9-14,21-22,24,30,36
3	Jitter at output for 3Hz@2.33UIpp input			1.3	UIpp	1-3,8,9-14,21-22,24,30,35
4	with 40Hz to 100kHz filter			0.10	UIpp	1-3,8,9-14,21-22,24,30,36
5	Jitter at output for 5Hz@2.07UIpp input			0.80	UIpp	1-3,8,9-14,21-22,24,30,35
6	with 40Hz to 100kHz filter			0.10	UIpp	1-3,8,9-14,21-22,24,30,36
7	Jitter at output for 10Hz@1.76UIpp input			0.40	UIpp	1-3,8,9-14,21-22,24,30,35
8	with 40Hz to 100kHz filter			0.10	UIpp	1-3,8,9-14,21-22,24,30,36
9	Jitter at output for 100Hz@1.50UIpp input			0.06	UIpp	1-3,8,9-14,21-22,24,30,35
10	with 40Hz to 100kHz filter			0.05	UIpp	1-3,8,9-14,21-22,24,30,36
11	Jitter at output for 2400Hz@1.50UIpp input			0.04	UIpp	1-3,8,9-14,21-22,24,30,35
12	with 40Hz to 100kHz filter			0.03	UIpp	1-3,8,9-14,21-22,24,30,36
13	Jitter at output for 100kHz@0.20UIpp input			0.04	UIpp	1-3,8,9-14,21-22,24,30,35
14	with 40Hz to 100kHz filter			0.02	UIpp	1-3,8,9-14,21-22,24,30,36

† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - 8kHz Input Jitter Tolerance

	Characteristics	Sym	Min	Max	Units	Conditions/Notes†
1	Jitter tolerance for 1Hz input		0.80		UIpp	1-3,6,9-14,21-22,24-26,28
2	Jitter tolerance for 5Hz input		0.70		UIpp	1-3,6,9-14,21-22,24-26,28
3	Jitter tolerance for 20Hz input		0.60		UIpp	1-3,6,9-14,21-22,24-26,28
4	Jitter tolerance for 300Hz input		0.20		UIpp	1-3,6,9-14,21-22,24-26,28
5	Jitter tolerance for 400Hz input		0.15		UIpp	1-3,6,9-14,21-22,24-26,28
6	Jitter tolerance for 700Hz input		0.08		UIpp	1-3,6,9-14,21-22,24-26,28
7	Jitter tolerance for 2400Hz input		0.02		UIpp	1-3,6,9-14,21-22,24-26,28
8	Jitter tolerance for 3600Hz input		0.01		UIpp	1-3,6,9-14,21-22,24-26,28

† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - 1.544MHz Input Jitter Tolerance

	Characteristics	Sym	Min	Max	Units	Conditions/Notes†
1	Jitter tolerance for 1Hz input		150		UIpp	1-3,7,9-14,21-22,24-26,29
2	Jitter tolerance for 5Hz input		140		UIpp	1-3,7,9-14,21-22,24-26,29
3	Jitter tolerance for 20Hz input		130		UIpp	1-3,7,9-14,21-22,24-26,29
4	Jitter tolerance for 300Hz input		35		UIpp	1-3,7,9-14,21-22,24-26,29
5	Jitter tolerance for 400Hz input		25		UIpp	1-3,7,9-14,21-22,24-26,29
6	Jitter tolerance for 700Hz input		15		UIpp	1-3,7,9-14,21-22,24-26,29
7	Jitter tolerance for 2400Hz input		4		UIpp	1-3,7,9-14,21-22,24-26,29
8	Jitter tolerance for 10kHz input		1		UIpp	1-3,7,9-14,21-22,24-26,29
9	Jitter tolerance for 100kHz input		0.5		UIpp	1-3,7,9-14,21-22,24-26,29

† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - 2.048MHz Input Jitter Tolerance

	Characteristics	Sym	Min	Max	Units	Conditions/Notes†
1	Jitter tolerance for 1Hz input		150		UIpp	1-3,8,9-14,21-22,24-26,30
2	Jitter tolerance for 5Hz input		140		UIpp	1-3,8,9-14,21-22,24-26,30
3	Jitter tolerance for 20Hz input		130		UIpp	1-3,8,9-14,21-22,24-26,30
4	Jitter tolerance for 300Hz input		50		UIpp	1-3,8,9-14,21-22,24-26,30
5	Jitter tolerance for 400Hz input		40		UIpp	1-3,8,9-14,21-22,24-26,30
6	Jitter tolerance for 700Hz input		20		UIpp	1-3,8,9-14,21-22,24-26,30
7	Jitter tolerance for 2400Hz input		5		UIpp	1-3,8,9-14,21-22,24-26,30
8	Jitter tolerance for 10kHz input		1		UIpp	1-3,8,9-14,21-22,24-26,30
9	Jitter tolerance for 100kHz input		1		UIpp	1-3,8,9-14,21-22,24-26,30

† See "Notes" following AC Electrical Characteristics tables.

AC Electrical Characteristics - OSCi 20MHz Master Clock Input

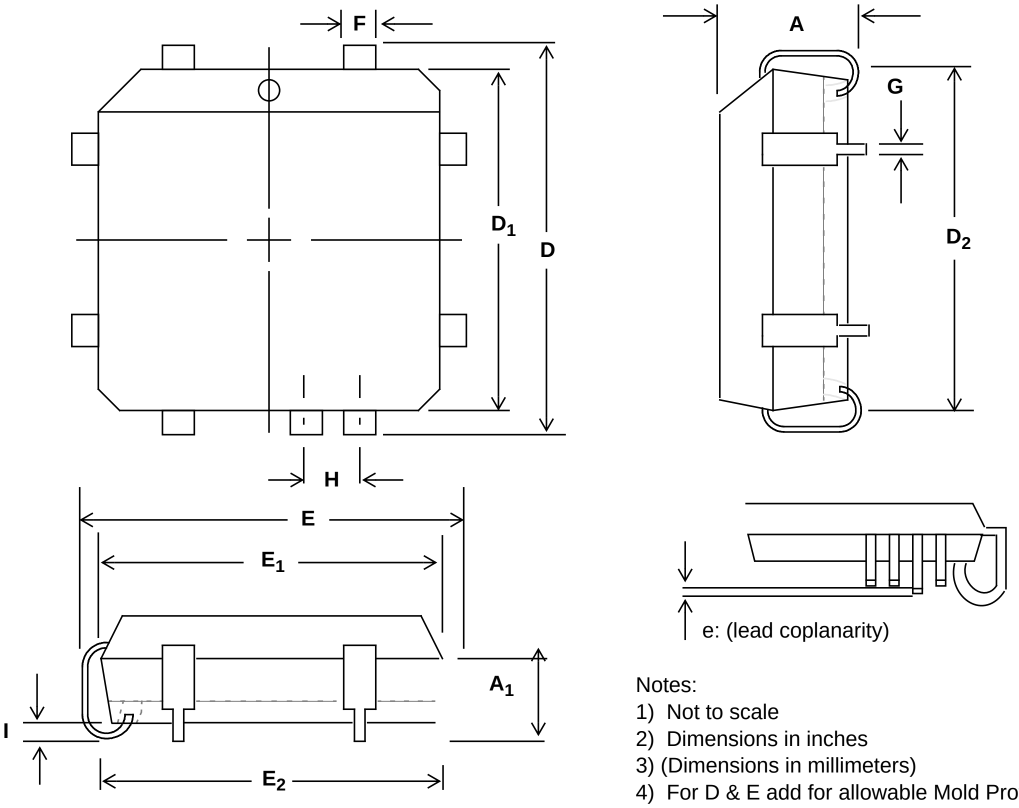
	Characteristics	Sym	Min	Max	Units	Conditions/Notes†
1	Frequency accuracy (20 MHz nominal)		-0	+0	ppm	15,18
2			-32	+32	ppm	16,19
3			-100	+100	ppm	17,20
4	Duty cycle		40	60	%	
5	Rise time			10	ns	
6	Fall time			10	ns	

† See "Notes" following AC Electrical Characteristics tables.

† Notes:

Voltages are with respect to ground (V_{SS}) unless otherwise stated.
Supply voltage and operating temperature are as per Recommended Operating Conditions.
Timing parameters are as per AC Electrical Characteristics - Timing Parameter Measurement Voltage Levels

1. PRI reference input selected.
2. SEC reference input selected.
3. Normal Mode selected.
4. Holdover Mode selected.
5. Freerun Mode selected.
6. 8kHz Frequency Mode selected.
7. 1.544MHz Frequency Mode selected.
8. 2.048MHz Frequency Mode selected.
9. Master clock input OSCi at 20MHz ±0ppm.
10. Master clock input OSCi at 20MHz ±32ppm.
11. Master clock input OSCi at 20MHz ±100ppm.
12. Selected reference input at ±0ppm.
13. Selected reference input at ±32ppm.
14. Selected reference input at ±100ppm.
15. For Freerun Mode of ±0ppm.
16. For Freerun Mode of ±32ppm.
17. For Freerun Mode of ±100ppm.
18. For capture range of ±230ppm.
19. For capture range of ±198ppm.
20. For capture range of ±130ppm.
21. 25pF capacitive load.
22. OSCi Master Clock jitter is less than 2nspp, or 0.04UIpp where1UIpp=1/20MHz.
23. Jitter on reference input is less than 7nspp.
24. Applied jitter is sinusoidal.
25. Minimum applied input jitter magnitude to regain synchronization.
26. Loss of synchronization is obtained at slightly higher input jitter amplitudes.
27. Within 10ms of the state, reference or input change.
28. 1UIpp = 125us for 8kHz signals.
29. 1UIpp = 648ns for 1.544MHz signals.
30. 1UIpp = 488ns for 2.048MHz signals.
31. 1UIpp = 323ns for 3.088MHz signals.
32. 1UIpp = 244ns for 4.096MHz signals.
33. 1UIpp = 122ns for 8.192MHz signals.
34. 1UIpp = 61ns for 16.384MHz signals.
35. No filter.
36. 40Hz to 100kHz bandpass filter.
37. With respect to reference input signal frequency.
38. After a $\overline{\text{RST}}$ or $\overline{\text{TRST}}$.
39. Master clock duty cycle 40% to 60%.
40. Prior to Holdover Mode, device was in Normal Mode and phase locked.



Notes:
1) Not to scale
2) Dimensions in inches
3) (Dimensions in millimeters)
4) For D & E add for allowable Mold Protrusion 0.010"

Dim	20-Pin		28-Pin		44-Pin		68-Pin		84-Pin	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	0.165 (4.20)	0.180 (4.57)	0.165 (4.20)	0.180 (4.57)	0.165 (4.20)	0.180 (4.57)	0.165 (4.20)	0.200 (5.08)	0.165 (4.20)	0.200 (5.08)
A_1	0.090 (2.29)	0.120 (3.04)	0.090 (2.29)	0.120 (3.04)	0.090 (2.29)	0.120 (3.04)	0.090 (2.29)	0.130 (3.30)	0.090 (2.29)	0.130 (3.30)
D/E	0.385 (9.78)	0.395 (10.03)	0.485 (12.32)	0.495 (12.57)	0.685 (17.40)	0.695 (17.65)	0.985 (25.02)	0.995 (25.27)	1.185 (30.10)	1.195 (30.35)
D_1/E_1	0.350 (8.890)	0.356 (9.042)	0.450 (11.430)	0.456 (11.582)	0.650 (16.510)	0.656 (16.662)	0.950 (24.130)	0.958 (24.333)	1.150 (29.210)	1.158 (29.413)
D_2/E_2	0.290 (7.37)	0.330 (8.38)	0.390 (9.91)	0.430 (10.92)	0.590 (14.99)	0.630 (16.00)	0.890 (22.61)	0.930 (23.62)	1.090 (27.69)	1.130 (28.70)
e	0	0.004	0	0.004	0	0.004	0	0.004	0	0.004
F	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)
G	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)
H	0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)	
I	0.020 (0.51)		0.020 (0.51)		0.020 (0.51)		0.020 (0.51)		0.020 (0.51)	

Plastic J-Lead Chip Carrier - P-Suffix

Notes:

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