

SRAM

32K x 9 SRAM

5 VOLT SRAM

FEATURES

- High speed: 15, 17, 20 and 25ns
- High-performance, low-power CMOS double-metal process
- Single +5V $\pm 10\%$ power supply
- Easy memory expansion with $\overline{CE1}$, CE2 and \overline{OE} options
- All inputs and outputs are TTL compatible

OPTIONS

- Timing
 - 15ns access
 - 17ns access
 - 20ns access
 - 25ns access
- Packages
 - Plastic SOJ (300 mil)
- 2V data retention
- Part Number Example: MT5C2889DJ-25 L

MARKING

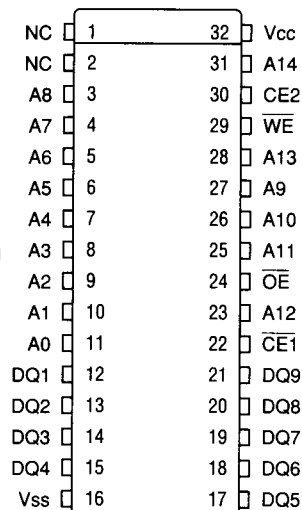
-15
-17
-20
-25

DJ

L

PIN ASSIGNMENT (Top View)

32-Pin SOJ (SD-4)



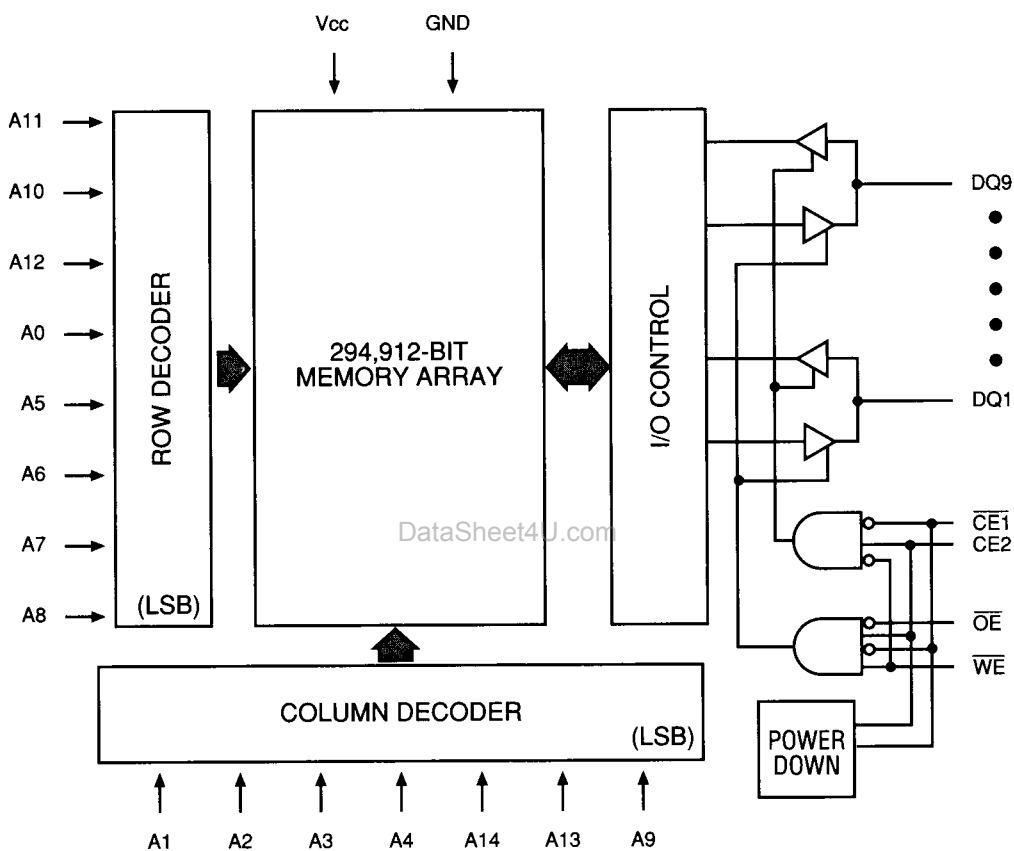
GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. They are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers dual chip enables ($\overline{CE1}$, CE2) and output enable (\overline{OE}) control signals. This enhancement can place the outputs in High-Z for additional flexibility in system design. The dual chip enables may be used to directly address multiple banks of SRAM without external logic.

Writing to these devices is accomplished when write enable (\overline{WE}) and $\overline{CE1}$ inputs are both LOW while CE2 is HIGH. Reading is accomplished when \overline{WE} and CE2 remain HIGH while $\overline{CE1}$ and \overline{OE} go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM

TRUTH TABLE

MODE	OE	CE1	CE2	WE	DQ	POWER
STANDBY	X	H	X	X	HIGH-Z	STANDBY
STANDBY	X	X	L	X	HIGH-Z	STANDBY
READ	L	L	H	H	Q	ACTIVE
READ	H	L	H	H	HIGH-Z	ACTIVE
WRITE	X	L	H	L	D	ACTIVE

MICRON**MT5C2889
32K x 9 SRAM****5 VOLT SRAM****ABSOLUTE MAXIMUM RATINGS***

Voltage on V _{CC} Supply Relative to V _{SS}	-1V to +7V
Storage Temperature	-55°C to +150°C
Power Dissipation	1W
Short Circuit Output Current	50mA
Voltage on any pin relative to V _{SS}	-1V to V _{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS(0°C ≤ T_A ≤ 70°C, V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V _{IH}	2.2	V _{CC} +1	V	1
Input Low (Logic 0) Voltage		V _{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V _{IN} ≤ V _{CC}	I _{LI}	-5	5	μA	
Output Leakage Current	Output(s) Disabled 0V ≤ V _{OUT} ≤ V _{CC}	I _{LO}	-5	5	μA	
Output High Voltage	I _{OH} = -4.0mA	V _{OH}	2.4		V	1
Output Low Voltage	I _{OL} = 8.0mA	V _{OL}		0.4	V	1
Supply Voltage		V _{CC}	4.5	5.5	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX				UNITS	NOTES
				-15	-17	-20	-25		
Power Supply Current: Operating	CE1 ≤ V _{IL} ; CE2 ≥ V _{IH} f = MAX = 1/4RC V _{CC} = MAX; Outputs Open	I _{CC}	90	145	130	120	110	mA	3, 14
Power Supply Current: Standby	CE1 ≥ V _{IH} or CE2 ≤ V _{IL} f = MAX = 1/4RC V _{CC} = MAX; Outputs Open	I _{SB1}	13	35	35	30	30	mA	14
	CE2 ≤ V _{SS} + 0.2V; CE1 ≥ V _{CC} - 0.2V; V _{CC} = MAX V _{IN} ≤ V _{SS} + 0.2V or V _{IN} ≥ V _{CC} - 0.2V; f = 0	I _{SB2}	0.7	7	7	7	7	mA	14

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T _A = 25°C; f = 1 MHz V _{CC} = 5V	C _I	7	pF	4
Output Capacitance		C _O	5	pF	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

 (Note 5) ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$)

5 VOLT SRAM

DESCRIPTION	SYM	-15		-17		-20		-25		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle											
READ cycle time	t_{RC}	15		17		20		25		ns	
Address access time	t_{AA}		15		17		20		25	ns	
Chip Enable access time	t_{ACE}		15		17		20		25	ns	
Output hold from address change	t_{OH}	3		3		3		5		ns	
Chip Enable to output in Low-Z	t_{LZCE}	4		4		4		4		ns	7
Chip disable to output in High-Z	t_{HZCE}		8		8		8		8	ns	6, 7
Chip Enable to power up time	t_{PU}	0		0		0		0		ns	
Chip disable to power down time	t_{PD}		15		17		20		25	ns	
Output Enable access time	t_{AOE}		8		8		8		8	ns	
Output Enable to output in Low-Z	t_{LZOE}	0		0		0		0		ns	
Output disable to output in High-Z	t_{HZOE}		7		7		7		7	ns	6
WRITE Cycle											
WRITE cycle time	t_{WC}	15		17		20		25		ns	
Chip Enable to end of write	t_{CW}	10		13		15		20		ns	
Address valid to end of write	t_{AW}	10		13		15		20		ns	
Address setup time	t_{AS}	0		0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		0		ns	
WRITE pulse width	t_{WP1}	10		13		15		20		ns	
WRITE pulse width	t_{WP2}	12		13		15		20		ns	
Data setup time	t_{DS}	7		8		10		10		ns	
Data hold time	t_{DH}	0		0		0		0		ns	
Write disable to output in Low-Z	t_{LZWE}	4		4		4		4		ns	7
Write Enable to output in High-Z	t_{HZWE}		7		8		10		10	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	V _{ss} to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

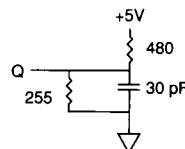


Fig. 1 OUTPUT LOAD EQUIVALENT

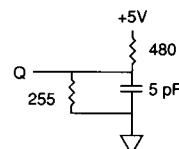


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

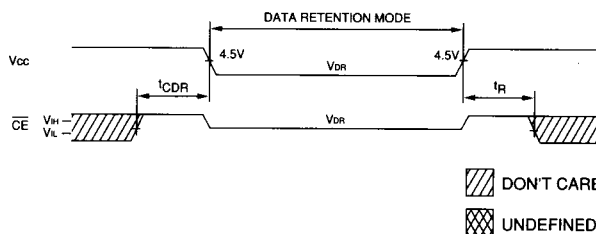
- All voltages referenced to V_{ss} (GND).
- 3V for pulse width < t_{RC}/2.
- I_{CC} is dependent on output loading and cycle rates.
- This parameter is sampled.
- Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- t_{HZCE}, t_{HZOE} and t_{HZWE} are specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE}.
- \overline{WE} is HIGH for READ cycle.
- Device is continuously selected. All chip enables are held in their active state.
- Address valid prior to, or coincident with, latest occurring chip enable.
- t_{RC} = Read Cycle Time.
- CE2 timing is identical to $\overline{CE1}$ timing. The waveform is inverted.
- Either $\overline{CE1}$, CE2 or \overline{WE} can initiate or terminate WRITE cycles.
- Typical values are measured at 5V, 25°C and 20ns cycle time.

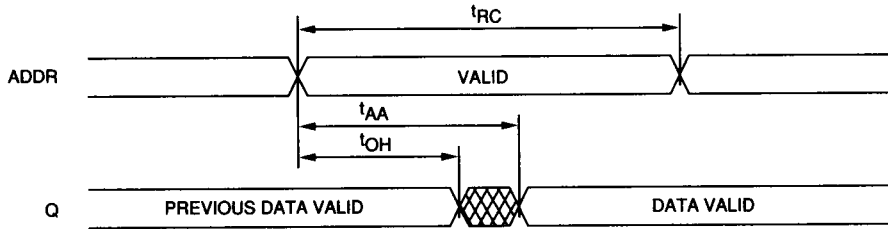
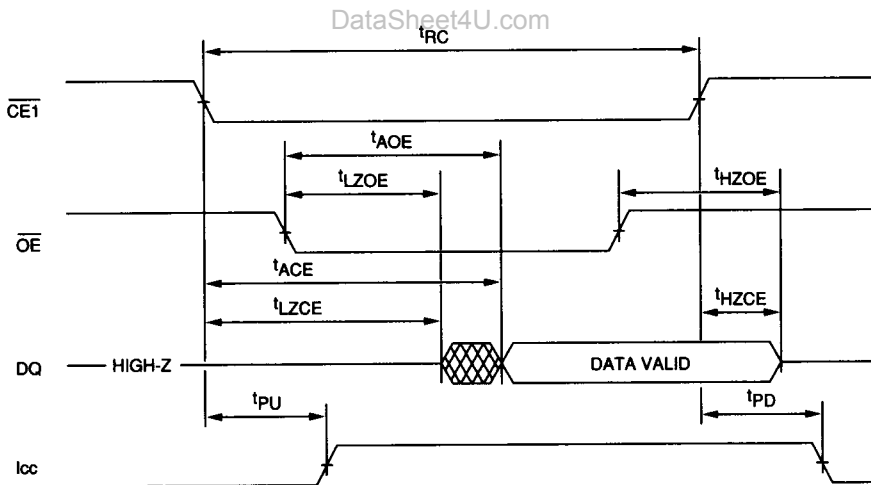
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DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V _{cc} for Retention Data		V _{DR}	2			V	
Data Retention Current	$\overline{CE} \geq (V_{CC} - 0.2V)$ $V_{IN} \geq (V_{CC} - 0.2V)$ or $\leq 0.2V$	I _{CCDR}	V _{CC} = 2V	40	400	μA	
	V _{CC} = 3V		100	600	μA		
Chip Deselect to Data Retention Time		t _{CDR}	0			ns	4
Operation Recovery Time		t _R	t _{RC}			ns	4, 11

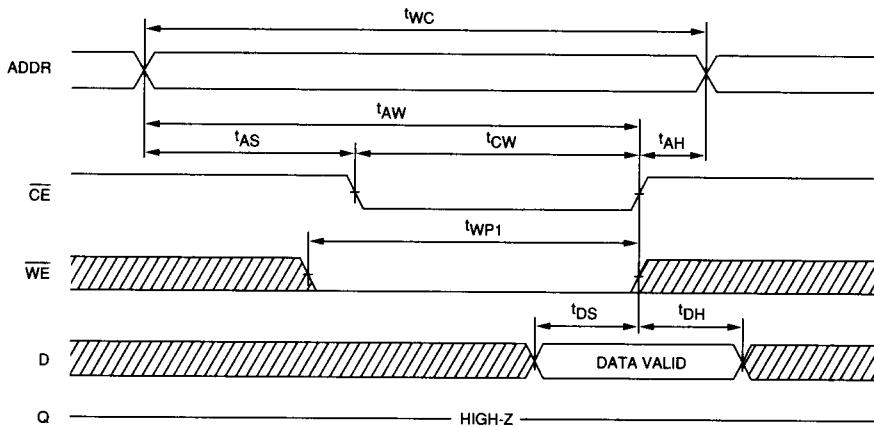
LOW V_{CC} DATA RETENTION WAVEFORM



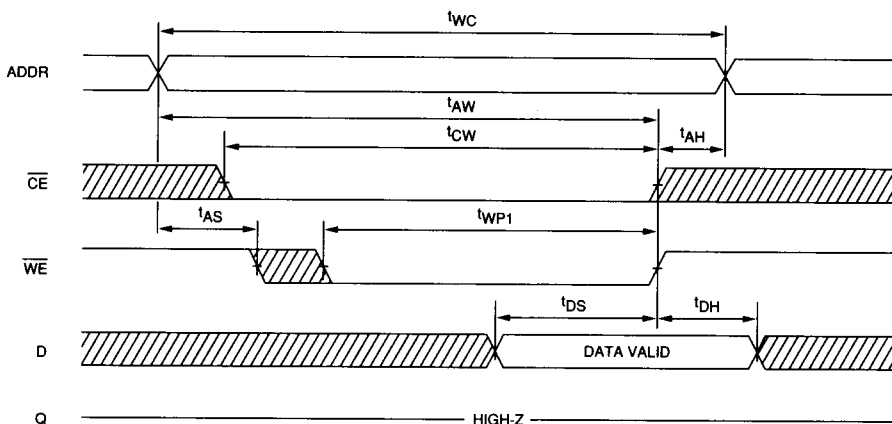
MICRON**MT5C2889**
32K x 9 SRAM**READ CYCLE NO. 1** ^{8, 9}**READ CYCLE NO. 2** ^{7, 8, 10, 12}

DON'T CARE

UNDEFINED

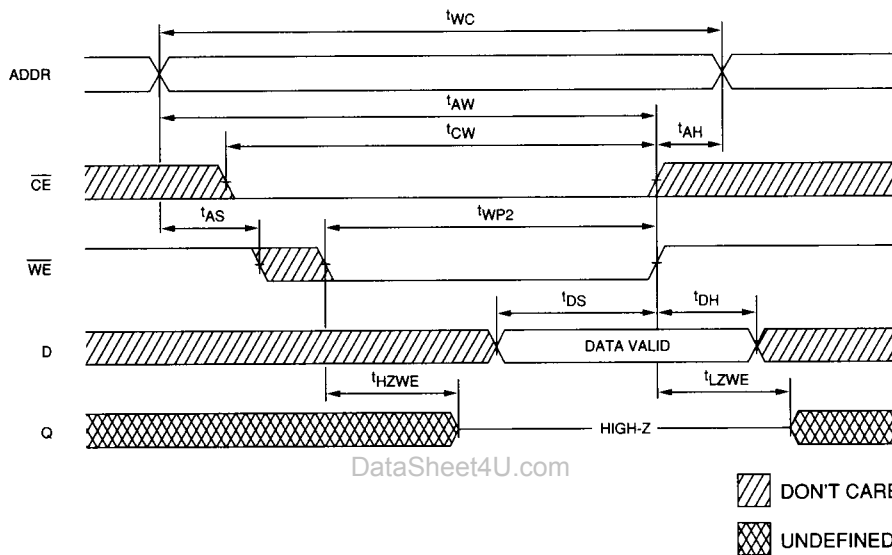
WRITE CYCLE NO. 1 ^{12, 13}
 (Chip Enable Controlled)


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WRITE CYCLE NO. 2 ^{12, 13}
 (Write Enable Controlled)


DON'T CARE
 UNDEFINED

NOTE: Output enable (\overline{OE}) is inactive (HIGH).

WRITE CYCLE NO. 3 7, 12, 13
 (Write Enable Controlled)


NOTE: Output enable (\overline{OE}) is active (LOW).