128K x 8 SRAM
WITH DUAL CHIP ENABLE ULTRA LOW POWER

AVAILABLE AS MILITARY SPECIFICATIONS
•MIL-STD-883, para. 1.2.2 compliant

FEATURES
- High Speed: 30 ns
- Low active power: 715 mW worst case
- Low CMOS standby power: 3.3 mW worst case
- 2.0V data retention, Ultra Low 0.3mW worst case power dissipation
- Battery backup applications
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with CE1\, CE2, and OE\ options

OPTIONS — MARKING

- **Timing**
  30ns access — -30
- **Package(s)**
  Ceramic DIP (400 mil) — C — No. 111
- **Temperature**
  Military (-55°C to +125°C) — MIL
- **Options**
  2V data retention/very low power — LL

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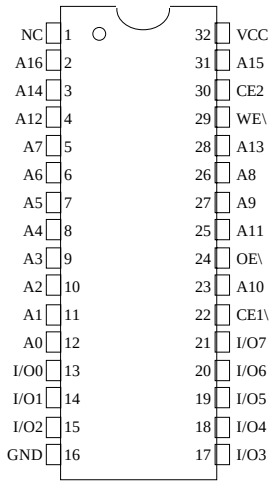
PIN ASSIGNMENT
(Top View)

32-Pin DIP (C)



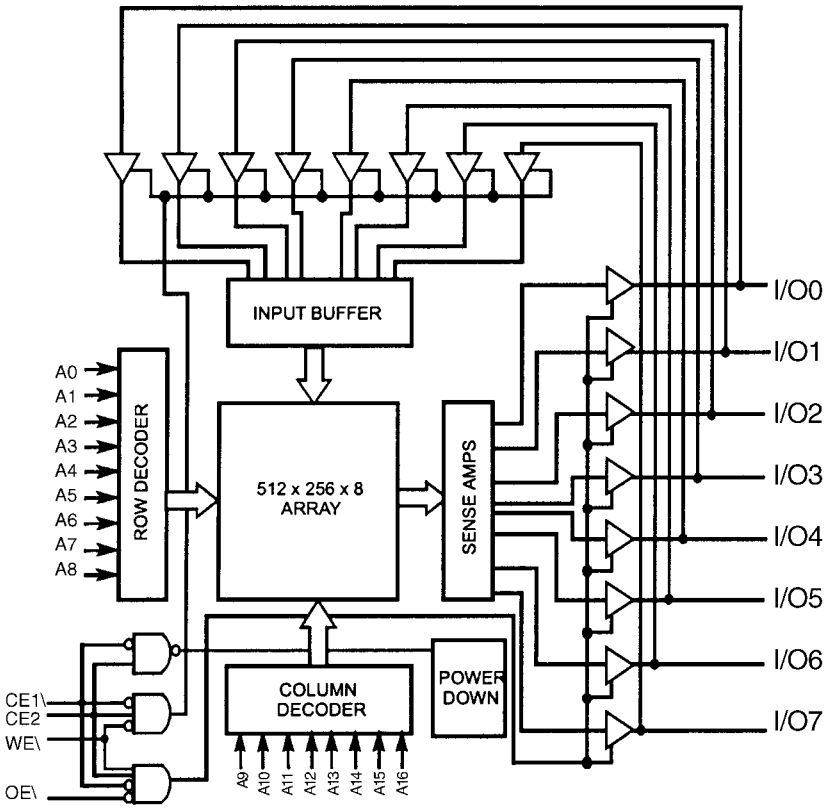
GENERAL DESCRIPTION

The MT5C1008 SRAM is a high-performance CMOS static RAM organized as 131, 072 words by 8 bits, offering low active power and ultra low standby and data retention current levels. Easy memory expansion is provided by an active LOW Chip Enable (CE1\), an active HIGH Chip Enable (CE2), and active Low Output Enable (OE\), and three-state drivers. Writing to the device is accomplished by taking Chip Enable One (CE1\) and Write Enable (WE\) inputs LOW and Chip Enable Two (CE2) input HIGH. Data on the eight I/O pins (I/O0 through I/O7) is then written into the location specified on the address pins (A0 through A16).

Reading from the device is accomplished by taking Chip Enable One (CE_1\) and Output Enable (OE\) LOW while forcing Write Enable (WE\) and Chip Enable Two (CE_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output (I/O0 through I/O7) are placed in a high-impedance state when the device is deselected (CE1\) HIGH or CE2 LOW), the outputs are disabled (OE\ HIGH), or during a write operation (CE1\ LOW, CE2 HIGH, and WE\ LOW).

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	OE\	CE1\	CE2	WE\	I/O0 - I/O7	POWER
Power-Down	X	H	X	X	High Z	Standby (I_{SB})
Power-Down	X	X	L	X	High Z	Standby (I_{SB})
Read	L	L	H	H	Data Out	Active (I_{CC})
Write	X	L	H	L	Data In	Active (I_{CC})
Selected, Outputs Disabled	H	L	H	H	High Z	Active (I_{CC})

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage Range on Vcc to Relative GND[1]..-0.5V to +7.0V
Storage Temperature .....-65°C to +150°C
Ambient Temperature with Power Applied.....-55°C to +125°C
DC Voltage Applied to Outputs
in High Z State[1].....-0.5V to Vcc + 0.5V
DC Input Voltage[1].....-0.5V to Vcc + 0.5V

*Stresses at or greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods will affect reliability. Refer to page 17 of this data sheet for a technical note on this subject.

** Junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow, and humidity.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

($-55^oC < T_C < 125^oC$; V_{CC} = 5.0V +10%)

			-30			
PARAMETER	**CONDITIONS**	**SYM**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output HIGH Voltage	Vcc = MIN, I_{OH} = -4.0 mA	V_{OH}	2.4		V	
Output LOW Voltage	Vcc = MIN, I_{OL} = 8.0 mA	V_{OL}		0.4	V	
Input HIGH Voltage		V_{IH}	2.2	V_{CC}+0.3	V	
Input LOW Voltage		V_{IL}	-0.3	0.8	V	1
Input Load Current	GND ≤ V_I ≤ Vcc	I_{IX}	-10	+10	µA	
Output Leakage Current	GND ≤ V_I ≤ Vcc, Output Disabled	I_{OZ}	-10	+10	µA	
Vcc Operating Supply Current	Vcc = MAX, I_{OUT} = 0 mA f = f = $1/t_{RC}$	I_{CC}		130	mA	
Automatic CE Power-Down Current - TTL Inputs	MAX Vcc, CE1\ ≥ V_{IH} or CE2 ≤ V_{IL}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	I_{SB1}		4	mA	
Automatic CE Power-Down Current - CMOS Inputs	MAX Vcc, CE1\ ≥ Vcc - 0.3V, or CE2 ≤ 0.3V, V_{IN} ≥ Vcc - 0.3V, or V_{IN} ≤ 0.3V, f = 0	I_{SB2}		0.6	mA	

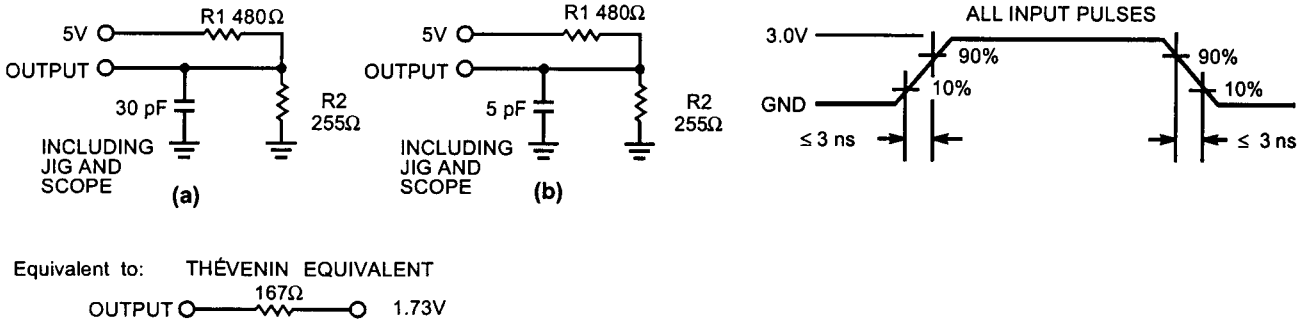
NOTES:
1. VIL(MIN) = -2.0V for pulse durations of less than 20ns.

CAPACITANCE[1]

PARAMETER	CONDITIONS	SYM	MAX	UNITS
Input Capacitance (A0 - A16)	TA = 25°C, f = 1MHz, Vcc = 5.0V	C_{IN}	8	pF
Input Capacitance (CE\, WE\, OE\)		C_{CLK}	10	pF
Output Capacitance		C_{OUT}	12	pF

NOTES:
1. Tested initially and after any design or process changes that may effect these parameters.

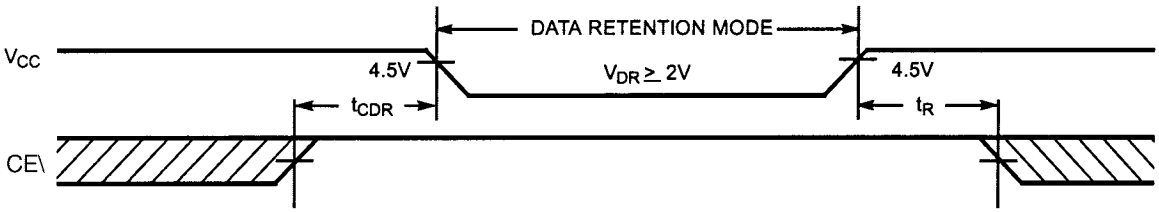
AC TEST LOADS AND WAVEFORMS



DATA RETENTION CHARACTERISTICS (-55°C < T_C < 125°C; V_{CC} = 5.0V +10%)

PARAMETER	CONDITIONS	SYM	MIN	MAX	UNITS
Vcc for Data Retention	0.2V, Vcc = V_{DR} = 2.0V, CE1\ ≥ Vcc - 0.3V or CE2 ≤ 0.3V, V_{IN} ≥ Vcc - 0.3V or V_{IN} ≤ 0.3V	V_{DR}	2.0		V
Data Retention Current		I_{CCDR}		150	µA
Chip Deselect to Data Retention Time		t_{CDR}	0		ns
Operation Recovery Time		t_R	200		µs

DATA RETENTION WAVEFORM



SWITCHING CHARACTERISTICS[1] (-55°C < T_C < 125°C; V_{CC} = 5.0V +10%)

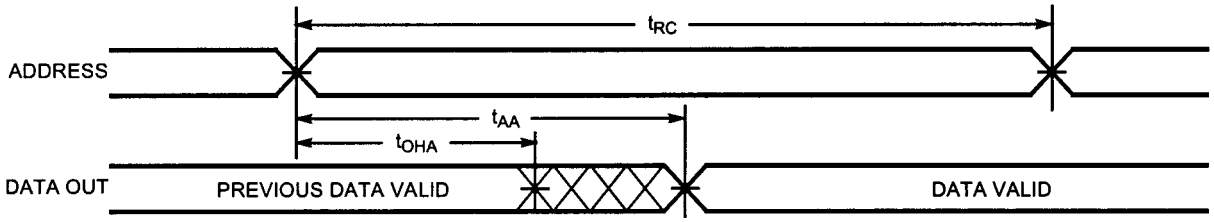
		-30			
PARAMETER	**SYM**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ CYCLE					
Read Cycle Time	t_{RC}	30		ns	
Address to Data Valid	t_{AA}		30	ns	
Data Hold from Address Change	t_{OHA}	3		ns	
CE1\ LOW to Data Valid, CE2 HIGH to Data Valid	t_{ACE}		30	ns	
OE\ LOW to Data Valid	t_{DOE}		12	ns	
OE\ LOW to Low Z	t_{LZOE}	0		ns	
OE\ HIGH to High Z	t_{HZOE}		8	ns	2, 3
CE1\ LOW to Low Z, CE2 HIGH to Low Z	t_{LZCE}	3		ns	3
CE1\ HIGH to High Z, CE2 LOW to High Z	t_{HZCE}		15	ns	2, 3
WRITE CYCLE[4]					
Write Cycle Time	t_{WC}	30		ns	5
CE1\ LOW to Write End, CE2 HIGH to Write End	t_{SCE}	22		ns	
Address Set-Up to Write End	t_{AW}	22		ns	
Address Hold from Write End	t_{HA}	0		ns	
Address Set-Up to Write Start	t_{SA}	0		ns	
WE\ Pulse Width	t_{PWE}	22		ns	
Data Set-up to Write End	t_{SD}	18		ns	
Data Hold from Write End	t_{HD}	0		ns	
WE\ HIGH to Low Z	t_{LZWE}	5		ns	3
WE\ LOW to High Z	t_{HZWE}		8	ns	2, 3

NOTES:

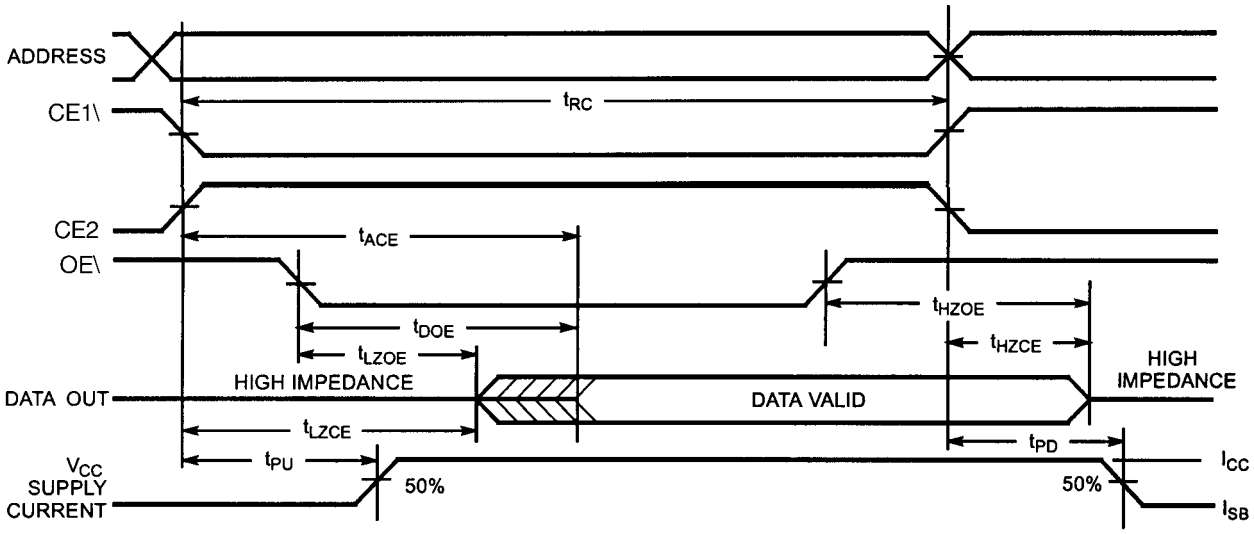
1. Test conditions assume signal transition time of 3ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30pF load capacitance.
2. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5pF as in part (b) of AC Test Loads. Transition is measured ±500mV from steady-state voltage.
3. At any given temperature and voltage condition, $t_{HZCE} < t_{LZCE}$, $t_{HZOE} < t_{LZOE}$, and $t_{HZWE} < t_{LZWE}$ for any given device.
4. The internal write time of the memory is defined by the overlap of CE1\ LOW, CE2 HIGH, and WE\ LOW. CE1\ and WE\ must be LOW and CE2 HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data setup and hold timing should be referenced to the leading edge of the signal that terminates the write.
5. The minimum write cycle time for Write Cycle No. 3 (WE\ controlled, OE\ LOW) is the sum of t_{HZWE} and t_{SD}.

SWITCHING WAVEFORMS

Read Cycle No. 1[1,2]



Read Cycle No. 2 (OE\ Controlled)[2,3]

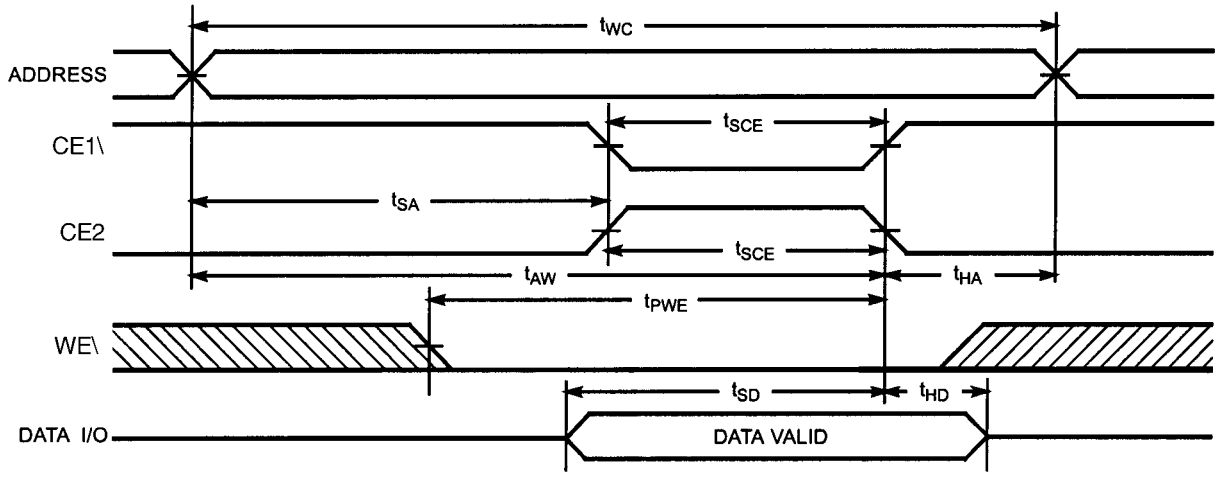


NOTES:

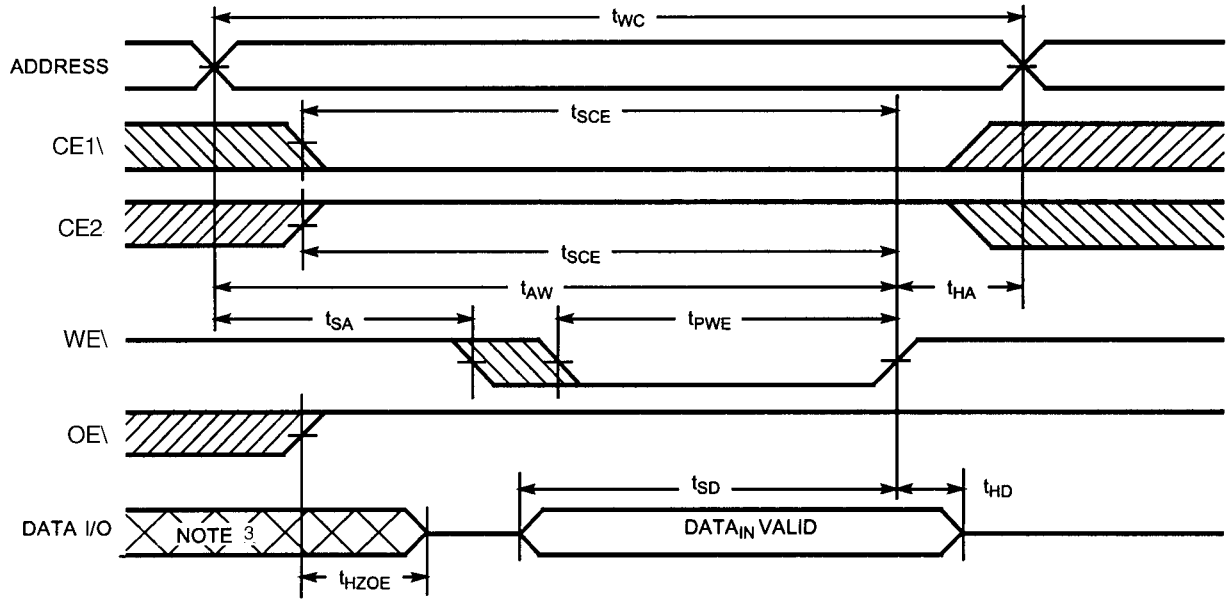
1. Device is continuously selected. OE\, CE1\ = V_{IL}, CE2 = V_{IH}.
2. WE\ is HIGH for read cycle.
3. Address valid prior to or coincident with CE1\ transition LOW and CE2 transition HIGH.

SWITCHING WAVEFORMS (continued)

Write Cycle No. 1 (CE1\ or CE2 Controlled)[1,2]



Write Cycle No. 2 (WE\ Controlled, OE\ HIGH During Write)[1,2]

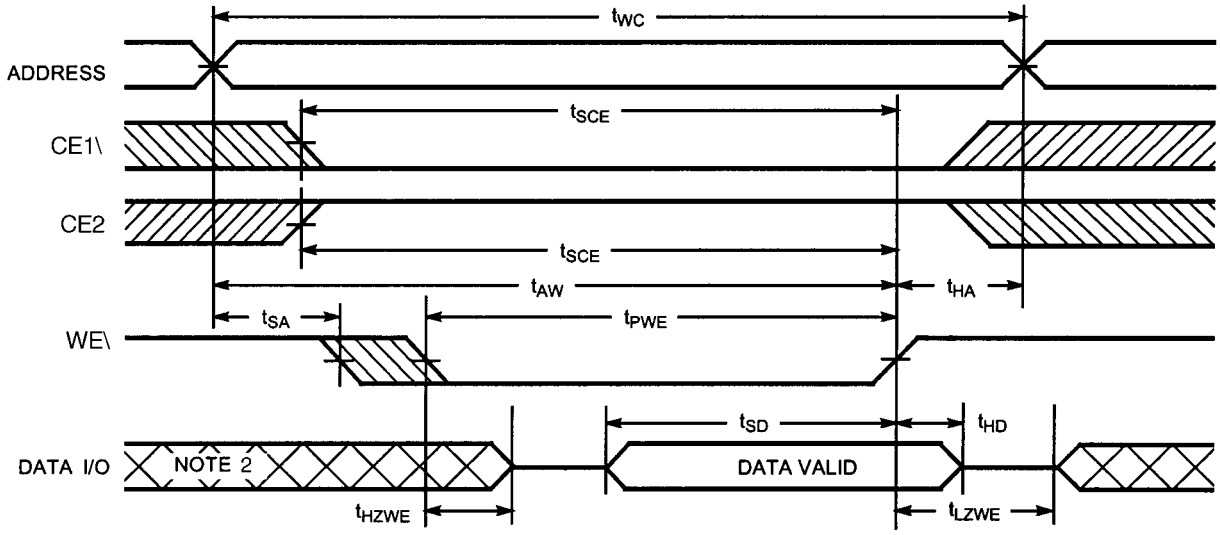


NOTES:

1. Data I/O is high impedance if OE\ = VIH.
2. If CE1\ goes HIGH or CE2 goes LOW simultaneously with WE\ going HIGH, the output remains in a high-impedance state.
3. During this period the I/Os are in the output state and input signals should not be applied.

SWITCHING WAVEFORMS (continued)

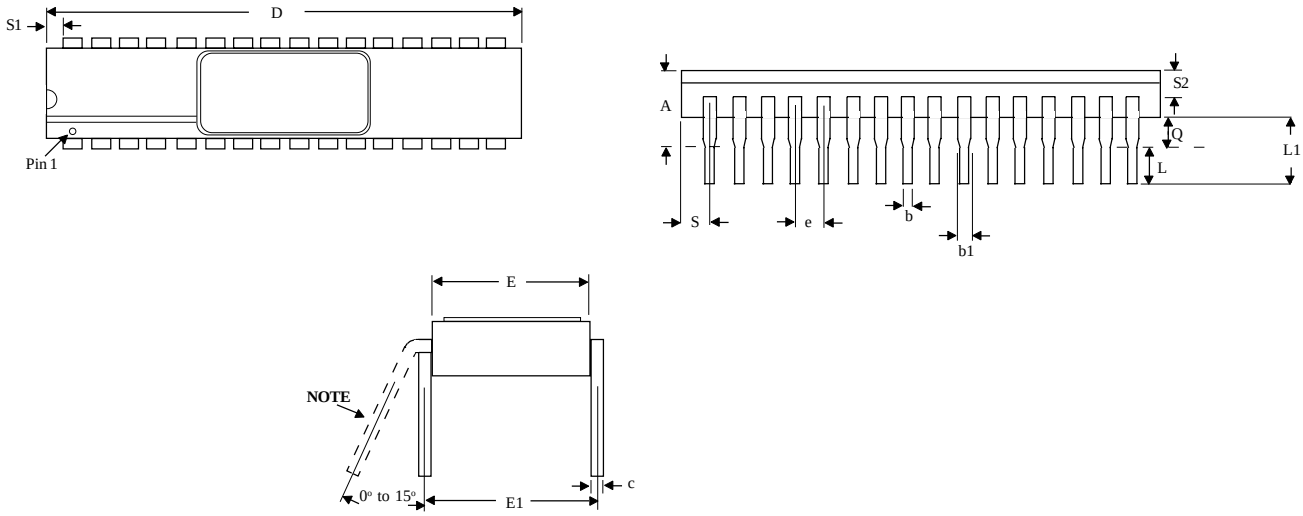
Write Cycle No. 3 (WE\ Controlled, OE\ LOW)[1]



NOTES:
1. If CE1\ goes HIGH or CE2 goes LOW simultaneously with WE\ going HIGH, the output remains in a high-impedance state.
2. During this period the I/Os are in the output state and input signals should not be applied.

MECHANICAL DEFINITIONS*

ASI Case #111 (Package Designator C)



Detail A

SYMBOL	ASI SPECIFICATIONS	
	MIN	MAX
A	---	0.232
b	0.014	0.023
b1	0.038	0.065
c	0.008	0.015
D	---	1.700
E	0.350	0.405
E1	0.390	0.420
e	0.100 BSC	
L	0.125	0.200
L1	0.150	---
Q	0.015	0.060
S	---	0.100
S1	0.005	---
S2	0.005	---
NOTE: Either configuration in detail A is allowed.		

All measurements are in inches.

ORDERING INFORMATION

EXAMPLE: MT5C1008C-30LL/MIL

Device Number	Package Type	Speed ns	Options**	Process
MT5C1008	C	-30	LL	/*

***AVAILABLE PROCESSES**

MIL = Military Processing
(MIL-STD-883, para. 1.2.2 compliant) -55°C to +125°C

**** OPTIONS**

LL = 2V Data Retention/Ultra Low Power

NOTE: For other speeds and options, see the MT5C1008 data sheet (available from www.austinsemiconductor.com).