ADVANCE

SMALL-OUTLINE DRAM MODULE

MT2LDT432H (X)(S), MT4LDT832H (X)(S)

For the latest data sheet, please refer to the Micron Web site: www.micronsemi.com/datasheets/datasheet.html

FEATURES

- JEDEC pinout in a 72-pin, small-outline, dual in-line memory module (SODIMM)
- 16MB (4 Meg x 32) and 32MB (8 Meg x 32)
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All inputs, outputs and clocks are TTL-compatible
- 4,096-cycle CAS#-BEFORE-RAS# (CBR) refresh distributed across 64ms
- FAST PAGE MODE (FPM) or Extended Data-Out (EDO) PAGE MODE access cycles
- Optional self refresh (S) for low-power data retention

OPTIONS / MARKING

- Package
  72-pin SODIMM (gold) — G
- Timing
  50ns access — -5
  60ns access — -6
- Access Cycles
  FAST PAGE MODE — None
  EDO PAGE MODE — X
- Refresh Rates
  Standard Refresh — None
  Self Refresh (128ms period) — S

PART NUMBERS

EDO Operating Mode

PART NUMBER	CONFIGURATION	REFRESH
MT2LDT432HG-xX	4 Meg x 32	Standard
MT2LDT432HG-xXS	4 Meg x 32	Self
MT4LDT832HG-xX	8 Meg x 32	Standard
MT4LDT832HG-xXS	8 Meg x 32	Self

x = speed

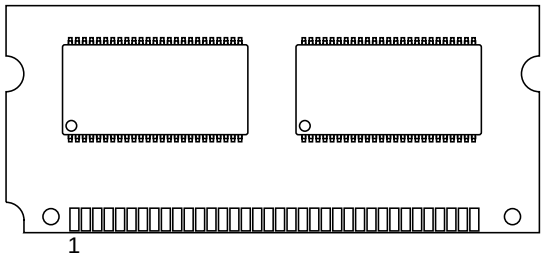
FPM Operating Mode

PART NUMBER	CONFIGURATION	REFRESH
MT2LDT432HG-x	4 Meg x 32	Standard
MT2LDT432HG-xS	4 Meg x 32	Self
MT4LDT832HG-x	8 Meg x 32	Standard
MT4LDT832HG-xS	8 Meg x 32	Self

x = speed

PIN ASSIGNMENT (Front View)

72-Pin Small-Outline DIMM



PIN	FRONT	PIN	BACK	PIN	FRONT	PIN	BACK
1	VSS	2	DQ0	37	DQ16	38	DQ17
3	DQ1	4	DQ2	39	VSS	40	CAS0#
5	DQ3	6	DQ4	41	CAS2#	42	CAS3#
7	DQ5	8	DQ6	43	CAS1#	44	RAS0#
9	DQ7	10	VDD	45	NC/RAS1#*	46	NC (A12)
11	PRD1	12	A0	47	WE#	48	NC (A13)
13	A1	14	A2	49	DQ18	50	DQ19
15	A3	16	A4	51	DQ20	52	DQ21
17	A5	18	A6	53	DQ22	54	DQ23
19	A10	20	NC	55	NC	56	DQ24
21	DQ8	22	DQ9	57	DQ25	58	DQ26
23	DQ10	24	DQ11	59	DQ28	60	DQ27
25	DQ12	26	DQ13	61	VDD	62	DQ29
27	DQ14	28	A7	63	DQ30	64	DQ31
29	A11	30	VDD	65	NC	66	PRD2
31	A8	32	A9	67	PRD3	68	PRD4
33	NC/RAS3#*	34	RAS2#	69	PRD5	70	PRD6
35	DQ15	36	NC	71	PRD7	72	VSS

*32MB version only

NOTE: Symbols in parentheses are not used on these modules but may be used for other modules in this product family. They are for reference only.

KEY TIMING PARAMETERS

EDO Operating Mode

SPEED	tRC	tRAC	tPC	tAA	tCAC	tCAS
-5	84ns	50ns	20ns	25ns	13ns	8ns
-6	104ns	60ns	25ns	30ns	15ns	10ns

FPM Operating Mode

SPEED	tRC	tRAC	tPC	tAA	tCAC	tRP
-5	90ns	50ns	30ns	25ns	13ns	30ns
-6	110ns	60ns	35ns	30ns	15ns	40ns

GENERAL DESCRIPTION

The MT2LDT432H (X)(S) and MT4LDT832H (X)(S) are randomly accessed 16MB and 32MB memories organized in a small-outline x32 configuration. They are specially processed to operate from 3V to 3.6V for low-voltage memory systems.

During READ or WRITE cycles, each bit is uniquely addressed through the address bits, which are entered 12 bits (A0-A11) at a time. RAS# is used to latch the first 12 bits and CAS# the latter 10 bits.

READ and WRITE cycles are selected with the WE# input. A logic HIGH on WE# dictates read mode, while a logic LOW on WE# dictates write mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. If WE# goes LOW prior to CAS# going LOW, the output pin(s) remain open (High-Z) until the next CAS# cycle.

FAST PAGE MODE

FAST-PAGE-MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST-PAGE-MODE cycle is always initiated with a row address strobed in by RAS#, followed by a column address strobed in by CAS#. Additional columns may be accessed by providing valid column addresses, strobing CAS# and holding RAS# LOW, thus executing faster memory cycles. Returning RAS# HIGH terminates the FAST-PAGE-MODE operation.

EDO PAGE MODE

EDO PAGE MODE, designated by the "X" version, is an accelerated FAST-PAGE-MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS# goes back HIGH. EDO provides for CAS# precharge time (^{t}CP) to occur without the output data going invalid. This elimination of CAS# output control provides for pipelined READs.

FAST-PAGE-MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. EDO operates as any DRAM READ or FAST-PAGE-MODE READ, except data will be held valid or become valid after CAS# goes HIGH, as long as RAS# and OE# are held LOW. (Refer to the 4 Meg x 16 [MT4LC4M16R6] DRAM data sheet for additional information on EDO functionality.)

REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# refresh cycle (RAS#-ONLY, CBR or HIDDEN) so that all combinations of RAS# addresses are executed at least every ^{t}REF, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS# addressing.

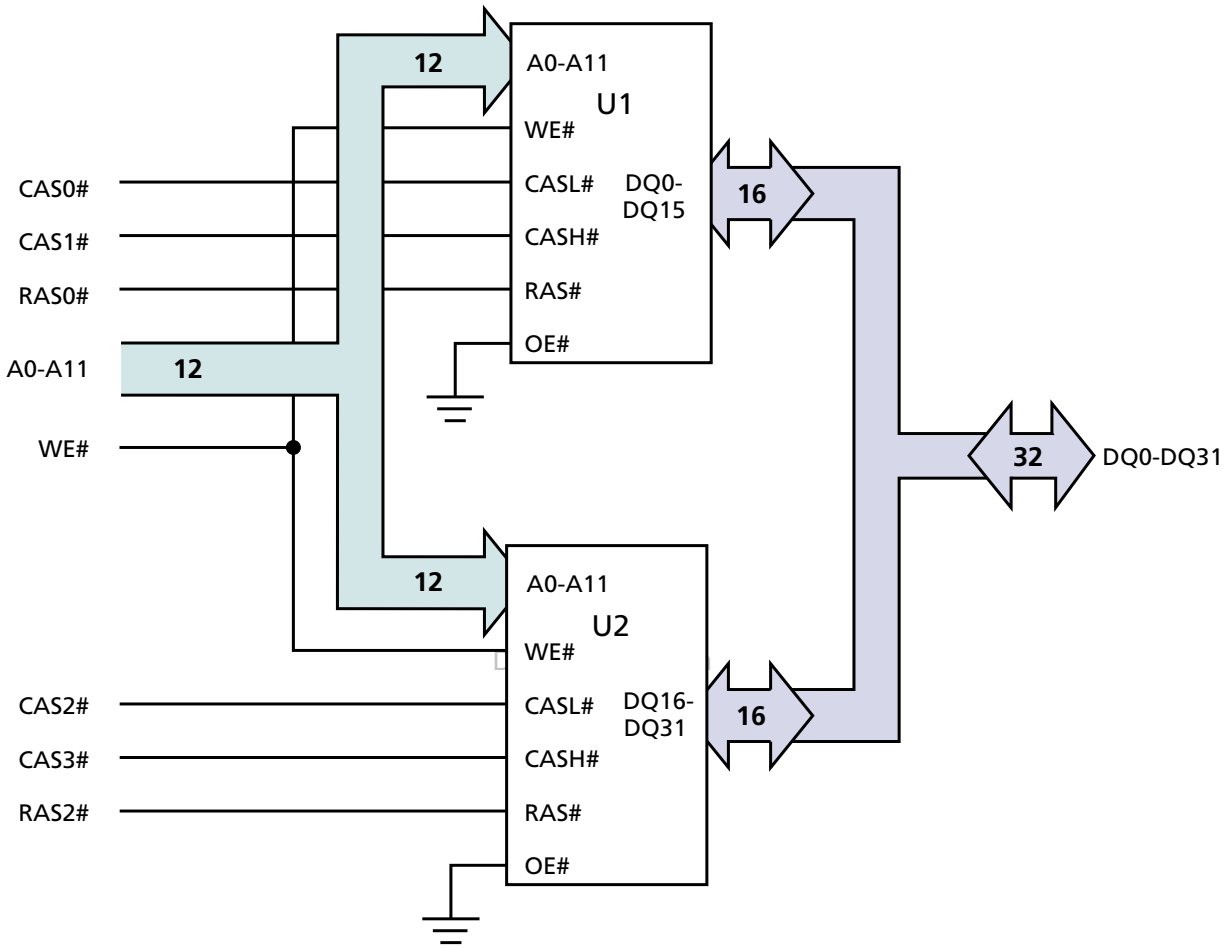
An optional self refresh mode is also available. The "S" option allows the user the choice of a fully static, low-power data retention mode or a dynamic refresh mode at the extended refresh period of 128ms. The optional self refresh feature is initiated by performing a CBR REFRESH cycle and holding RAS# LOW for the specified ^{t}RASS.

The self refresh mode is terminated by driving RAS# HIGH for a minimum time of ^{t}RPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS# LOW-to-HIGH transition. If the DRAM controller uses a distributed refresh sequence, a burst refresh is not required upon exiting self refresh. However, if the DRAM controller utilizes a RAS#-ONLY or burst refresh sequence, all rows must be refreshed within the average internal refresh rate, prior to the resumption of normal operation.

STANDBY

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS# HIGH time.

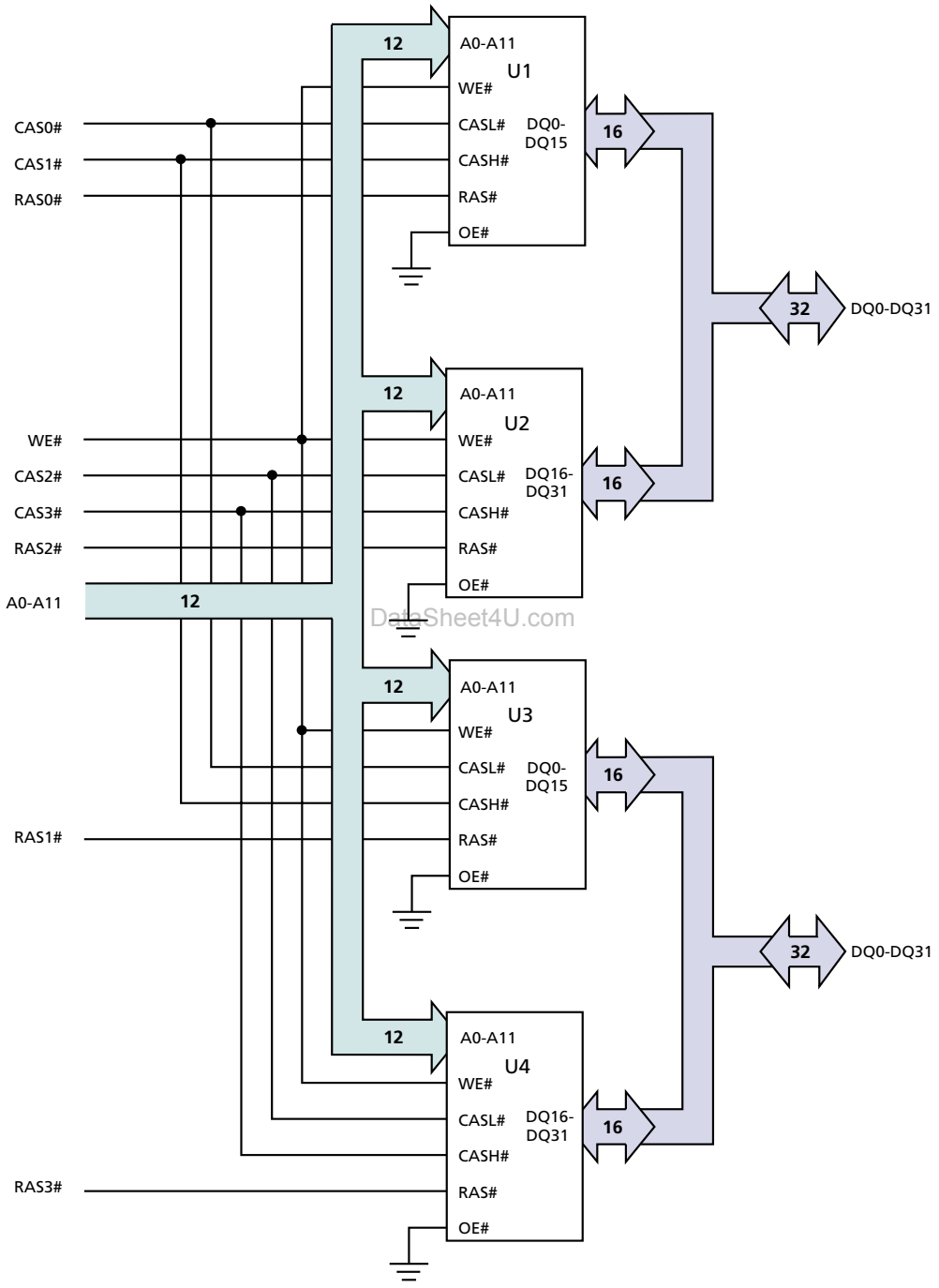
FUNCTIONAL BLOCK DIAGRAM
MT2LDT432H (X)(S) (16MB)



U1-U2 = MT4LC4M16R6TG (S) EDO PAGE MODE

U1-U2 = MT4LC4M16F5TG (S) FAST PAGE MODE

FUNCTIONAL BLOCK DIAGRAM
MT4LDT832H (X)(S) (32MB)



U1-U4 = MT4LC4M16R6TG (S) EDO PAGE MODE

U1-U4 = MT4LC4M16F5TG (S) FAST PAGE MODE

JEDEC-DEFINED PRESENCE-DETECT – MT2LDT432H (X)(S) (16MB)

SYMBOL	PIN	-5	-6
PRD1	11	NC	NC
PRD2	66	NC	NC
PRD3	67	Vss	Vss
PRD4	68	NC	NC
PRD5	69	Vss	NC
PRD6	70	Vss	NC
PRD7	71	X*	X*

JEDEC-DEFINED PRESENCE-DETECT – MT4LDT832H (X)(S) (32MB)

SYMBOL	PIN	-5	-6
PRD1	11	NC	NC
PRD2	66	NC	NC
PRD3	67	Vss	Vss
PRD4	68	Vss	Vss
PRD5	69	Vss	NC
PRD6	70	Vss	NC
PRD7	71	X*	X*

*X = NC (Normal Refresh) or Vss (Self Refresh)

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Supply
Relative to V_{SS} ..... -1V to +4.6V
Voltage on Inputs or I/O Pins
Relative to V_{SS} ..... -1V to +4.6V
Operating Temperature, T_A (ambient) .. 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +125°C
Power Dissipation 4W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION		SYMBOL	SIZE	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE		V_{DD}	ALL	3	3.6	V	
INPUT HIGH VOLTAGE: Valid Logic 1; All inputs		V_{IH}	ALL	2	V_{DD} + 0.3	V	26
INPUT LOW VOLTAGE: Valid Logic 0; All inputs		V_{IL}	ALL	-0.3	0.8	V	26
INPUT LEAKAGE CURRENT: Any input at V_{IN} (0V £ V_{IN} £ V_{DD} + 0.3V); All other pins not under test = 0V	CAS0#-CAS3#	I_{IL1}	16MB 32MB	-2 -4	2 4	µA	
	A0-A11, WE#	I_{I2}	16MB 32MB	-4 -8	4 8	µA	
	RAS0#-RAS3#	I_{I3}	16MB 32MB	-2 -2	2 2	µA	
OUTPUT LEAKAGE CURRENT: DQ is disabled; 0V £ V_{OUT} £ V_{DD} + 0.3V	DQ0-DQ31	I_{OZ}	16MB 32MB	-5 -10	5 10	µA	
OUTPUT LEVELS: Output High Voltage (I_{OUT} = -2mA)		V_{OH}	ALL	2.4	–	V	
Output Low Voltage (I_{OUT} = 2mA)		V_{OL}	ALL	–	0.4	V	

IDD OPERATING CONDITIONS AND MAXIMUM LIMITS

(Notes: 1, 5, 6) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -5	MAX -6	UNITS	NOTES
STANDBY CURRENT: TTL (RAS# = CAS# = V_{IH})	I_{DD1}	16MB 32MB	2 4	2 4	mA	
STANDBY CURRENT: CMOS (RAS# = CAS# • V_{DD} - 0.2V; DQs may be left open; Other inputs: V_{IN} • V_{DD} - 0.2V or V_{IN} £ 0.2V)	I_{DD2}	16MB 32MB	1 2	1 2	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, address cycling: ^{t}RC = ^{t}RC [MIN])	I_{DD3}	16MB 32MB	350 352	330 332	mA	3, 22
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS# = V_{IL}, CAS#, address cycling: ^{t}PC = ^{t}PC [MIN])	I_{DD4}	16MB 32MB	210 212	190 192	mA	3, 22
OPERATING CURRENT: EDO PAGE MODE ("X" version only) Average power supply current (RAS# = V_{IL}, CAS#, address cycling: ^{t}PC = ^{t}PC [MIN])	I_{DD5} (X only)	16MB 32MB	310 312	250 252	mA	3, 22
REFRESH CURRENT: RAS#-ONLY Average power supply current (RAS# cycling, CAS# = V_{IH}: ^{t}RC = ^{t}RC [MIN])	I_{DD6}	16MB 32MB	350 352	330 332	mA	3, 22
REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, address cycling: ^{t}RC = ^{t}RC [MIN])	I_{DD7}	16MB 32MB	350 352	330 332	mA	3, 4
REFRESH CURRENT: SELF ("S" version only) Average power supply current: CBR with RAS# • $^{t}RASS$ (MIN) and CAS# held LOW; WE# = V_{DD} - 0.2V; A0-A11, OE# and D_{IN} = V_{DD} - 0.2V or 0.2V (D_{IN} may be left open)	I_{DD8} (S only)	16MB 32MB	0.8 1.6	0.8 1.6	mA	3, 4

CAPACITANCE

PARAMETER	SYMBOL	MAX 16MB	MAX 32MB	UNITS	NOTES
Input Capacitance: A0-A11	C_{I1}	14	24	pF	2
Input Capacitance: WE#	C_{I2}	18	32	pF	2
Input Capacitance: RAS0#-RAS3#	C_{I3}	10	10	pF	2
Input Capacitance: CAS0#-CAS3#	C_{I4}	10	18	pF	2
Input/Output Capacitance: DQ0-DQ31	C_{IO}	10	18	pF	2

FAST PAGE MODE
AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12, 19) (V_{DD} = +3.3V ±0.3V)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-5		-6			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column address	^tAA		25		30	ns	
Column-address hold time (referenced to RAS#)	^tAR	40		45		ns	
Column-address setup time	^tASC	0		0		ns	
Row-address setup time	^tASR	0		0		ns	
Access time from CAS#	^tCAC		13		15	ns	
Column-address hold time	^tCAH	8		10		ns	
CAS# pulse width	^tCAS	13	10,000	15	10,000	ns	
CAS# LOW to "Don't Care" during Self Refresh	^tCHD	15		15		ns	25
CAS# hold time (CBR Refresh)	^tCHR	15		15		ns	4
CAS# to output in Low-Z	^tCLZ	3		3		ns	21
CAS# precharge time (FAST PAGE MODE)	^tCP	8		10		ns	13
Access time from CAS# precharge	^tCPA		30		35	ns	
CAS# to RAS# precharge time	^tCRP	5		5		ns	
CAS# hold time	^tCSH	50		60		ns	
CAS# setup time (CBR Refresh)	^tCSR	5		5		ns	4
WRITE command to CAS# lead time	^tCWL	13		15		ns	
Data-in hold time	^tDH	8		10		ns	18
Data-in setup time	^tDS	0		0		ns	18
Output buffer turn-off delay	^tOFF	3	13	3	15	ns	17, 21, 23
OE# setup prior to RAS# during HIDDEN REFRESH cycle	^tORD	0		0		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	30		35		ns	
Access time from RAS#	^tRAC		50		60	ns	
RAS# to column-address delay time	^tRAD	13		15		ns	15

FAST PAGE MODE
AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12, 19) (V_{DD} = +3.3V ±0.3V)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-5		-6			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Row-address hold time	^tRAH	8		10		ns	
RAS# pulse width	^tRAS	50	10,000	60	10,000	ns	
RAS# pulse width (Self Refresh)	^tRASS	100		100		µs	25
RAS# pulse width (FAST PAGE MODE)	^tRASP	50	125,000	60	125,000	ns	
Random READ or WRITE cycle time	^tRC	90		110		ns	
RAS# to CAS# delay time	^tRCD	18		20		ns	14
READ command hold time (referenced to CAS#)	^tRCH	0		0		ns	16
READ command setup time	^tRCS	0		0		ns	
Refresh period (4,096 cycles)	^tREF		64		64	ms	
Refresh period "S" version	^tREF		128		128	ms	25
RAS# precharge time	^tRP	30		40		ns	
RAS# to CAS# precharge time	^tRPC	0		0		ns	
RAS# precharge time (Self Refresh)	^tRPS	90		105		ns	25
READ command hold time (referenced to RAS#)	^tRRH	0		0		ns	16
RAS# hold time	^tRSH	13		15		ns	
WRITE command to RAS# lead time	^tRWL	13		15		ns	
Transition time (rise or fall)	^tT	2	50	2	50	ns	
WRITE command hold time	^tWCH	8		10		ns	
WRITE command hold time (referenced to RAS#)	^tWCR	40		45		ns	
WE# command setup time	^tWCS	0		0		ns	
WRITE command pulse width	^tWP	8		10		ns	
WE# hold time (CBR Refresh)	^tWRH	10		10		ns	
WE# setup time (CBR Refresh)	^tWRP	10		10		ns	

EDO PAGE MODE
AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12, 19) (V_{DD} = +3.3V ±0.3V)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-5		-6			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column address	^tAA		25		30	ns	
Column-address setup to CAS# precharge	^tACH	12		15		ns	
Column-address hold time (referenced to RAS#)	^tAR	38		45		ns	
Column-address setup time	^tASC	0		0		ns	
Row-address setup time	^tASR	0		0		ns	
Access time from CAS#	^tCAC		13		15	ns	
Column-address hold time	^tCAH	8		10		ns	
CAS# pulse width	^tCAS	8	10,000	10	10,000	ns	
CAS# LOW to "Don't Care" during Self Refresh	^tCHD	15		15		ns	25
CAS# hold time (CBR Refresh)	^tCHR	8		10		ns	4
CAS# to output in Low-Z	^tCLZ	0		0		ns	
Data output hold after next CAS# LOW	^tCOH	3		3		ns	
CAS# precharge time	^tCP	8		10		ns	13
Access time from CAS# precharge	^tCPA		28		35	ns	
CAS# to RAS# precharge time	^tCRP	5		5		ns	
CAS# hold time	^tCSH	38		45		ns	
CAS# setup time (CBR Refresh)	^tCSR	5		5		ns	4
WRITE command to CAS# lead time	^tCWL	8		10		ns	
Data-in hold time	^tDH	8		10		ns	18
Data-in setup time	^tDS	0		0		ns	18
Output buffer turn-off delay	^tOFF	0	12	0	15	ns	17, 23
EDO-PAGE-MODE READ or WRITE cycle time	^tPC	20		25		ns	
Access time from RAS#	^tRAC		50		60	ns	
RAS# to column-address delay time	^tRAD	9		12		ns	15
Row-address hold time	^tRAH	9		10		ns	
RAS# pulse width	^tRAS	50	10,000	60	10,000	ns	
RAS# pulse width (EDO PAGE MODE)	^tRASP	50	125,000	60	125,000	ns	
RAS# pulse width during Self Refresh	^tRASS	100		100		µs	25
Random READ or WRITE cycle time	^tRC	84		104		ns	
RAS# to CAS# delay time	^tRCD	11		14		ns	14

EDO PAGE MODE
AC ELECTRICAL CHARACTERISTICS

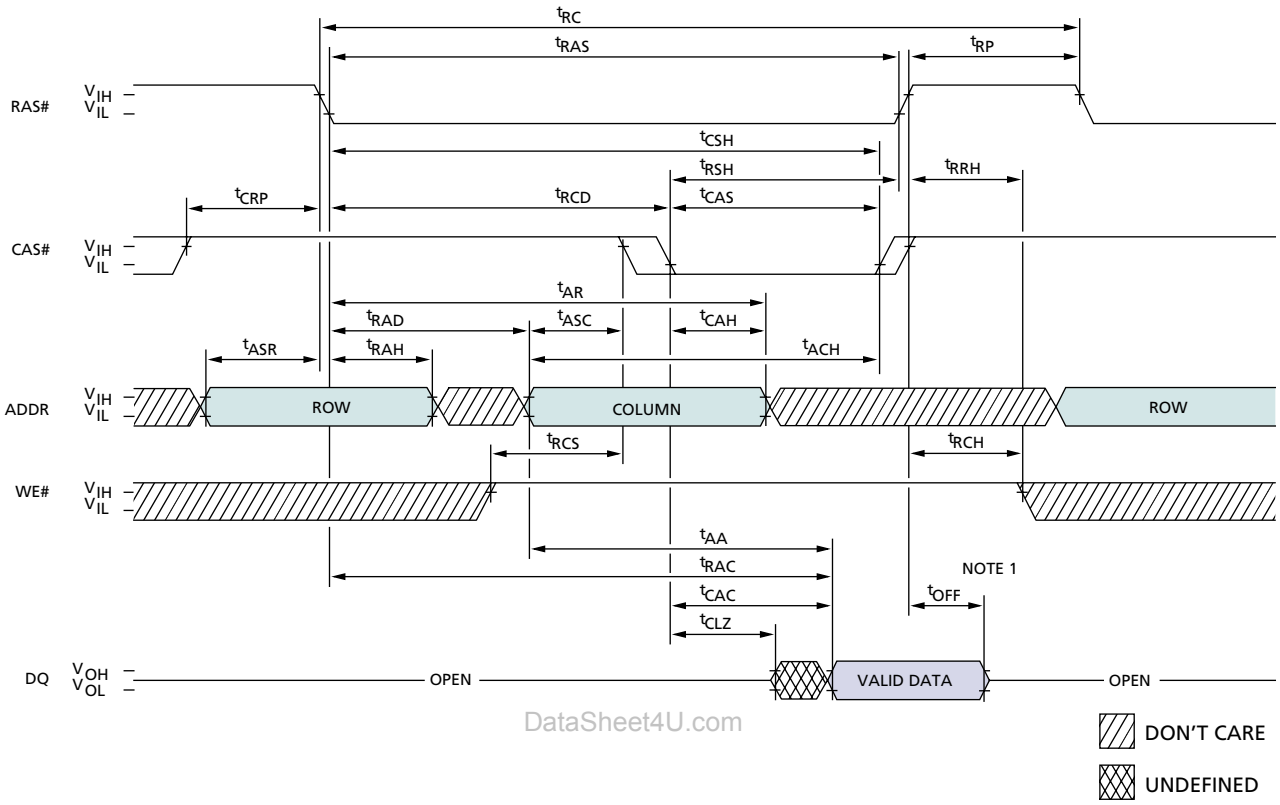
(Notes: 5, 6, 7, 8, 9, 10, 11, 12, 19) (V_{DD} = +3.3V ±0.3V)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-5		-6			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
READ command hold time (referenced to CAS#)	^{t}RCH	0		0		ns	16
READ command setup time	^{t}RCS	0		0		ns	
Refresh period (4,096 cycles)	^{t}REF		64		64	ms	
Refresh period "S" version	^{t}REF		128		128	ms	25
RAS# precharge time	^{t}RP	30		40		ns	
RAS# to CAS# precharge time	^{t}RPC	5		5		ns	
RAS# precharge time exiting Self Refresh	^{t}RPS	90		105		ns	25
READ command hold time (referenced to RAS#)	^{t}RRH	0		0		ns	16
RAS# hold time	^{t}RSH	13		15		ns	
WRITE command to RAS# lead time	^{t}RWL	13		15		ns	
Transition time (rise or fall)	^{t}T	2	50	2	50	ns	
WRITE command hold time	^{t}WCH	8		10		ns	
WRITE command hold time (referenced to RAS#)	^{t}WCR	38		45		ns	
WE# command setup time	^{t}WCS	0		0		ns	
Output disable delay from WE#	^{t}WHZ	0	12	0	15	ns	
WRITE command pulse width	^{t}WP	5		5		ns	
WE# pulse to disable at CAS# HIGH	^{t}WPZ	10		10		ns	
WE# hold time (CBR Refresh)	^{t}WRH	8		10		ns	
WE# setup time (CBR Refresh)	^{t}WRP	8		10		ns	

NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{DD} = +3.3V; f = 1 MHz.
3. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
6. An initial pause of 100µs is required after power-up, followed by eight RAS# REFRESH cycles (RAS#-ONLY or CBR with WE# HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
7. AC characteristics assume ^{t}T = 5ns for FPM and ^{t}T = 2.5ns for EDO.
8. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
9. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
10. For FPM: If CAS# = V_{IH}, data output is High-Z. For EDO: If CAS# and RAS# = V_{IH}, data output is High-Z.
11. If CAS# = V_{IL}, data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates and 100pF, V_{OL} = 0.8V and V_{OH} = 2V.
13. If CAS# is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for ^{t}CP.
14. The ^{t}RCD (MAX) limit is no longer specified. ^{t}RCD (MAX) was specified as a reference point only. If ^{t}RCD was greater than the specified ^{t}RCD (MAX) limit, then access time was controlled exclusively by ^{t}CAC (^{t}RAC [MIN] no longer applied). With or without the ^{t}RCD (MAX) limit, ^{t}AA and ^{t}CAC must always be met.
15. The ^{t}RAD (MAX) limit is no longer specified. ^{t}RAD (MAX) was specified as a reference point only. If ^{t}RAD was greater than the specified ^{t}RAD (MAX) limit, then access time was controlled exclusively by ^{t}AA (^{t}RAC and ^{t}CAC no longer applied). With or without the ^{t}RAD (MAX) limit, ^{t}AA, ^{t}RAC and ^{t}CAC must always be met.
16. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
17. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
18. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles.
19. OE# is tied permanently LOW; LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# = LOW and OE# = HIGH.
21. The 3ns minimum is a parameter guaranteed by design.
22. Column address changed once each cycle.
23. With the FPM option, ^{t}OFF is determined by the first RAS# or CAS# signal to transition HIGH. In comparison, ^{t}OFF on an EDO option is determined by the latter of the RAS# and CAS# signals to transition HIGH.
24. Applies to both FPM and EDO operating modes.
25. "S" version only.
26. V_{IH} overshoot: V_{IH} (MAX) = V_{DD} + 2V for a pulse width £ 10ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = -2V for a pulse width £ 10ns, and the pulse width cannot be greater than one third of the cycle rate.

READ CYCLE [24]



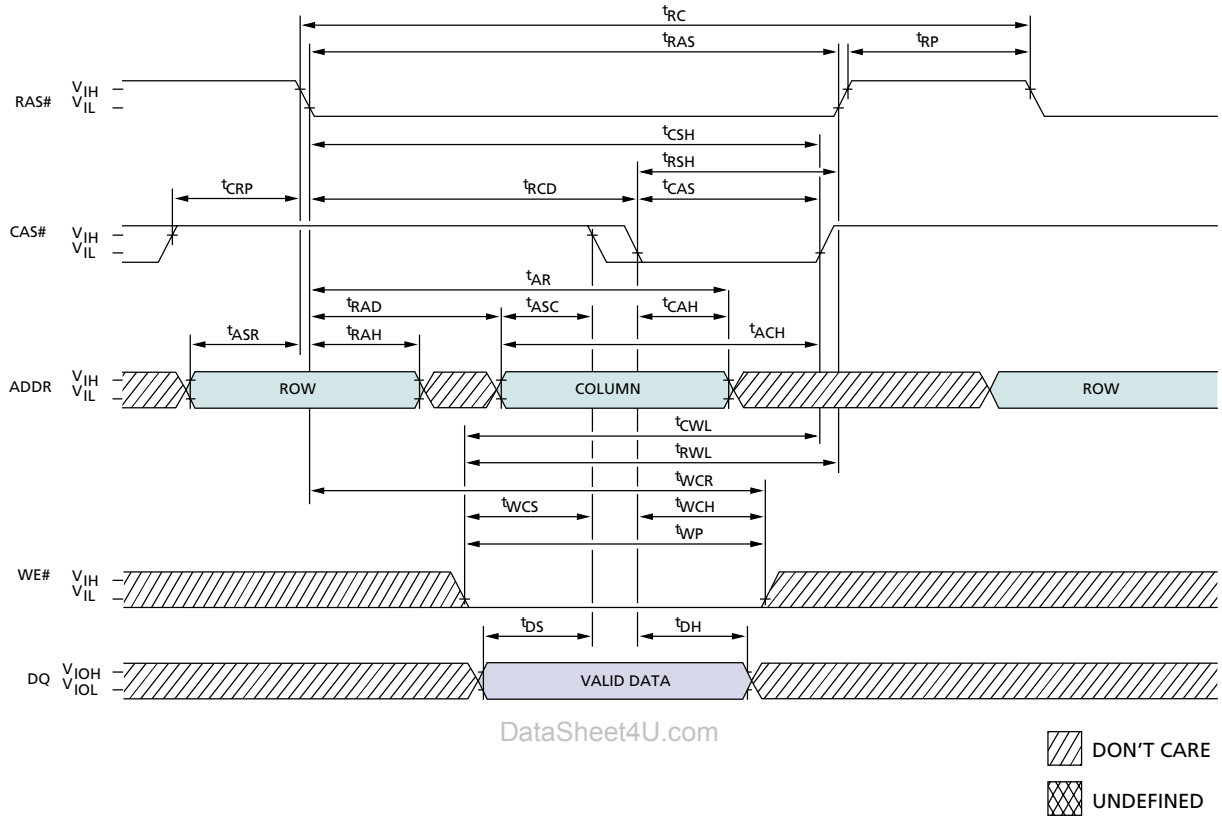
FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tACH (EDO)	12		15		ns
tAR (EDO)	38		45		ns
tAR (FPM)	40		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS (EDO)	8	10,000	10	10,000	ns
tCAS (FPM)	13	10,000	15	10,000	ns
tCLZ (EDO)	0		0		ns
tCLZ (FPM)	3		3		ns
tCRP	5		5		ns
tCSH (EDO)	38		45		ns
tCSH (FPM)	50		60		ns
tOFF (EDO)	0	12	0	15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOFF (FPM)	3	13	3	15	ns
tRAC		50		60	ns
tRAD (EDO)	9		12		ns
tRAD (FPM)	13		15		ns
tRAH (EDO)	9		10		ns
tRAH (FPM)	8		10		ns
tRAS	50	10,000	60	10,000	ns
tRC (EDO)	84		104		ns
tRC (FPM)	90		110		ns
tRCD (EDO)	11		14		ns
tRCD (FPM)	18		20		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRRH	0		0		ns
tRSH	13		15		ns

NOTE: 1. For EDO, tOFF is referenced from rising edge of RAS# or CAS#, whichever occurs last. For FPM, tOFF is referenced from rising edge of RAS# or CAS#, whichever occurs first.

EARLY WRITE CYCLE [24]

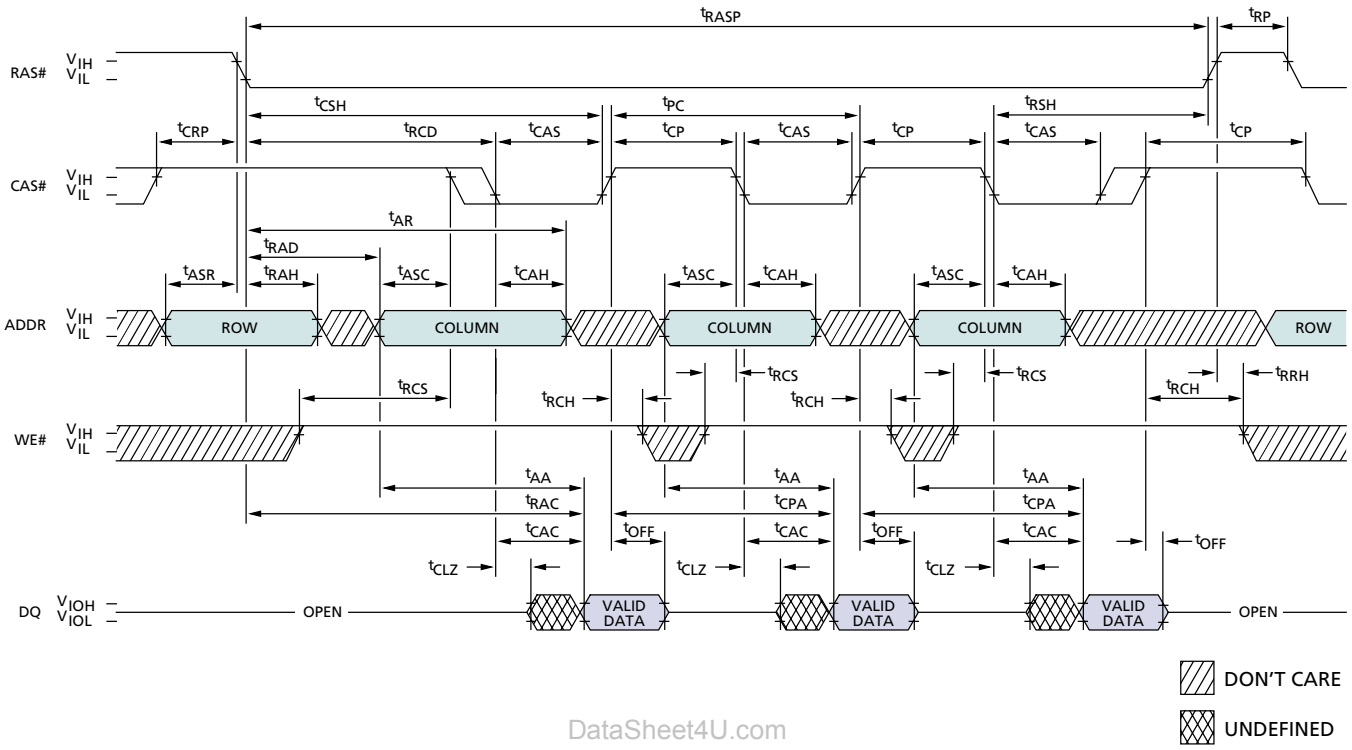


FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tACH (EDO)	12		15		ns
tAR (EDO)	38		45		ns
tAR (FPM)	40		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAH	8		10		ns
tCAS (FPM)	13	10,000	15	10,000	ns
tCAS (EDO)	8	10,000	10	10,000	ns
tCRP	5		5		ns
tCSH (FPM)	50		60		ns
tCSH (EDO)	38		45		ns
tCWL (FPM)	13		15		ns
tCWL (EDO)	8		10		ns
tDH	8		10		ns
tDS	0		0		ns
tRAD (FPM)	13		15		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tRAD (EDO)	9		12		ns
tRAH (EDO)	9		10		ns
tRAH (FPM)	8		10		ns
tRAS	50	10,000	60	10,000	ns
tRC (FPM)	90		110		ns
tRC (EDO)	84		104		ns
tRCD (FPM)	18		20		ns
tRCD (EDO)	11		14		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWL	13		15		ns
tWCH	8		10		ns
tWCR (EDO)	38		45		ns
tWCR (FPM)	40		45		ns
tWCS	0		0		ns
tWP (FPM)	8		10		ns
tWP (EDO)	5		5		ns

FAST-PAGE-MODE READ CYCLE

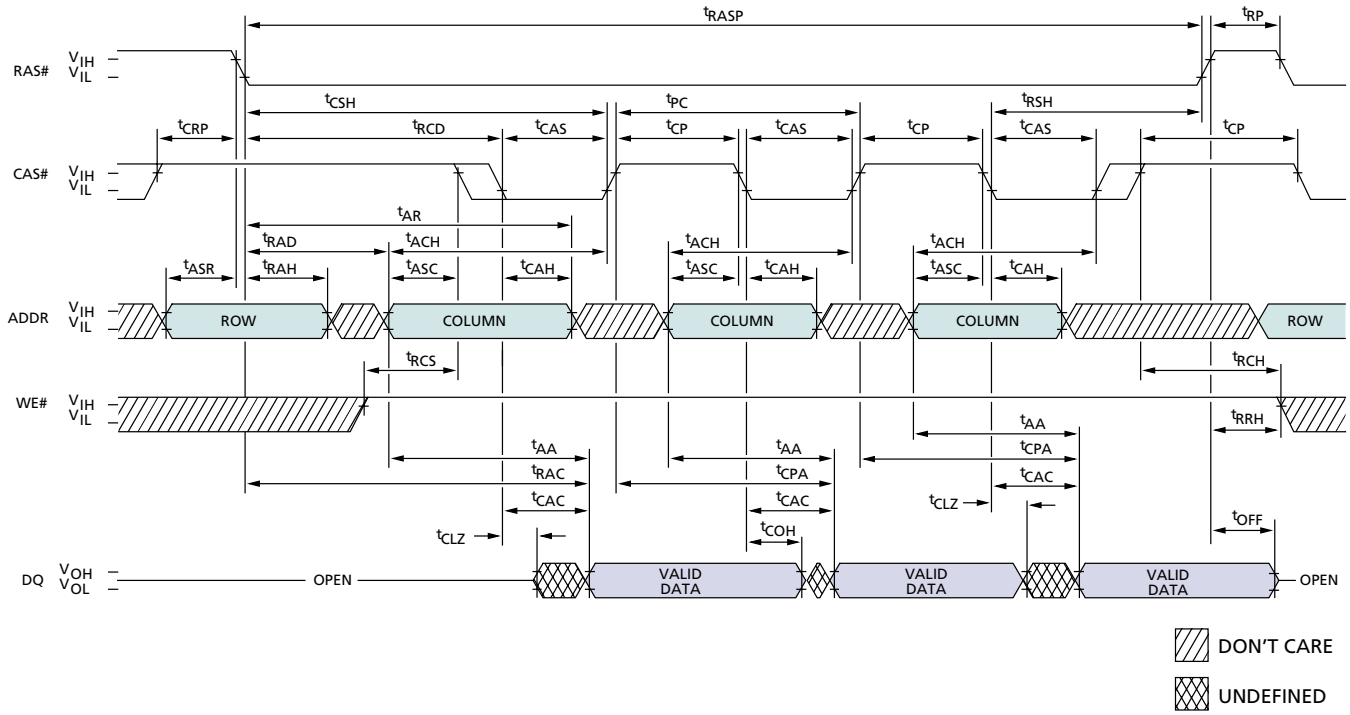


FAST PAGE MODE TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	40		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	13	10,000	15	10,000	ns
tCLZ	3		3		ns
tCP	8		10		ns
tCPA		30		35	ns
tCRP	5		5		ns
tCSH	50		60		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOFF	3	13	3	15	ns
tPC	30		35		ns
tRAC		50		60	ns
tRAD	13		15		ns
tRAH	8		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	18		20		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRRH	0		0		ns
tRSH	13		15		ns

EDO-PAGE-MODE READ CYCLE

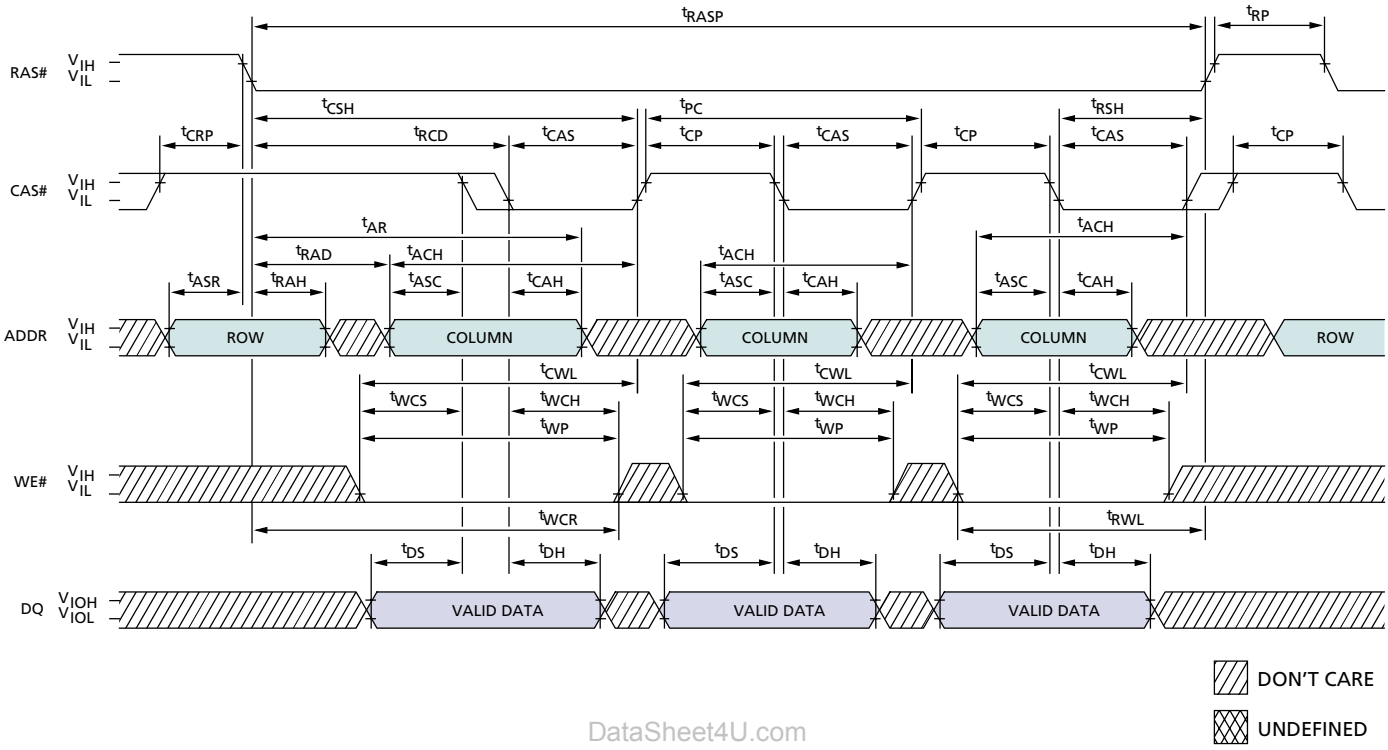


EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tACH	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLZ	0		0		ns
tCOH	3		3		ns
tCP	8		10		ns
tCPA		28		35	ns
tCRP	5		5		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tCSH	38		45		ns
tOFF	0	12	0	15	ns
tPC	20		25		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRRH	0		0		ns
tRSH	13		15		ns

FAST/EDO-PAGE-MODE EARLY WRITE CYCLE[24]

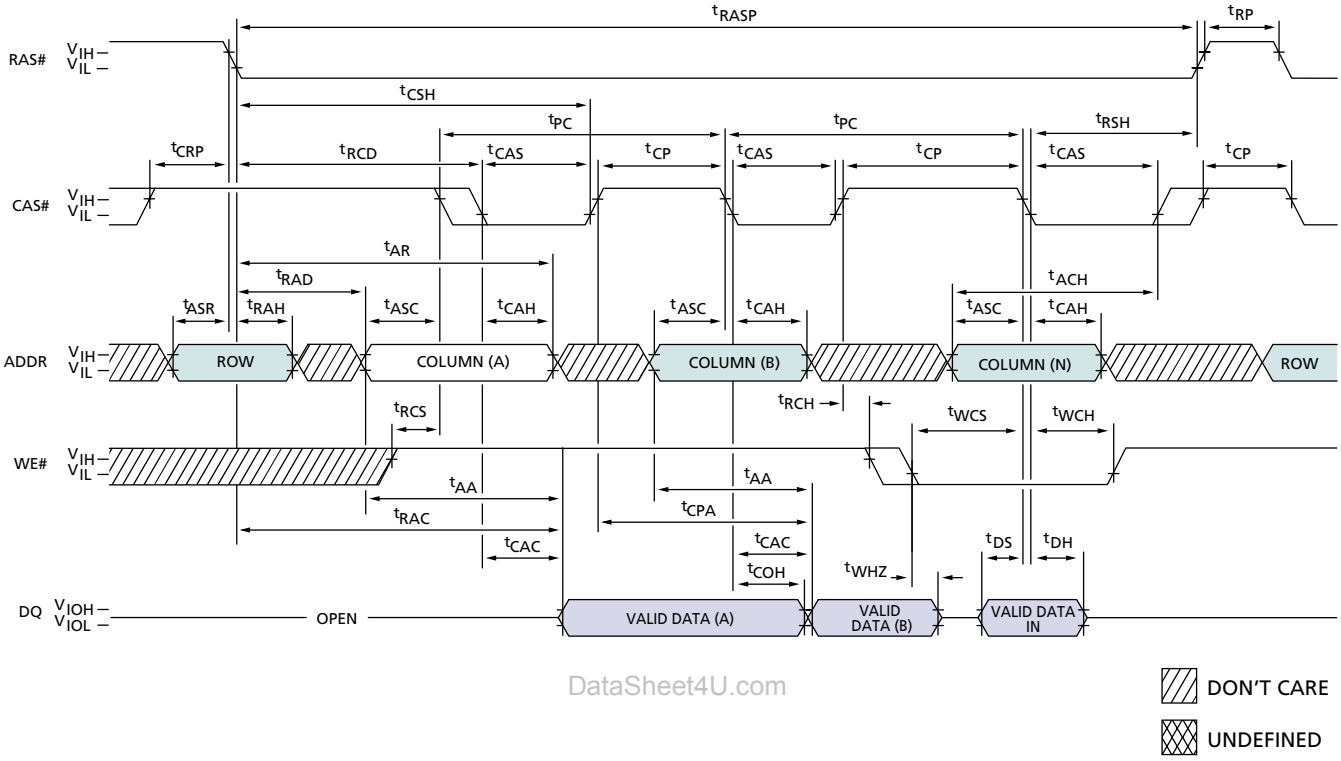


FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tACH (EDO)	12		15		ns
tAR (EDO)	38		45		ns
tAR (FPM)	40		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAH	8		10		ns
tCAS (EDO)	8	10,000	10	10,000	ns
tCAS (FPM)	13	10,000	15	10,000	ns
tCP	8		10		ns
tCRP	5		5		ns
tCSH (EDO)	38		45		ns
tCSH (FPM)	50		60		ns
tCWL (EDO)	8		10		ns
tCWL (FPM)	13		15		ns
tDH	8		10		ns
tDS	0		0		ns
tPC (EDO)	20		25		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tPC (FPM)	30		35		ns
tRAD (EDO)	9		12		ns
tRAD (FPM)	13		15		ns
tRAH (EDO)	9		10		ns
tRAH (FPM)	8		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD (EDO)	11		14		ns
tRCD (FPM)	18		20		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWL	13		15		ns
tWCH	8		10		ns
tWCR (EDO)	38		45		ns
tWCR (FPM)	40		45		ns
tWCS	0		0		ns
tWP (EDO)	5		5		ns
tWP (FPM)	8		10		ns

EDO-PAGE-MODE READ EARLY WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)

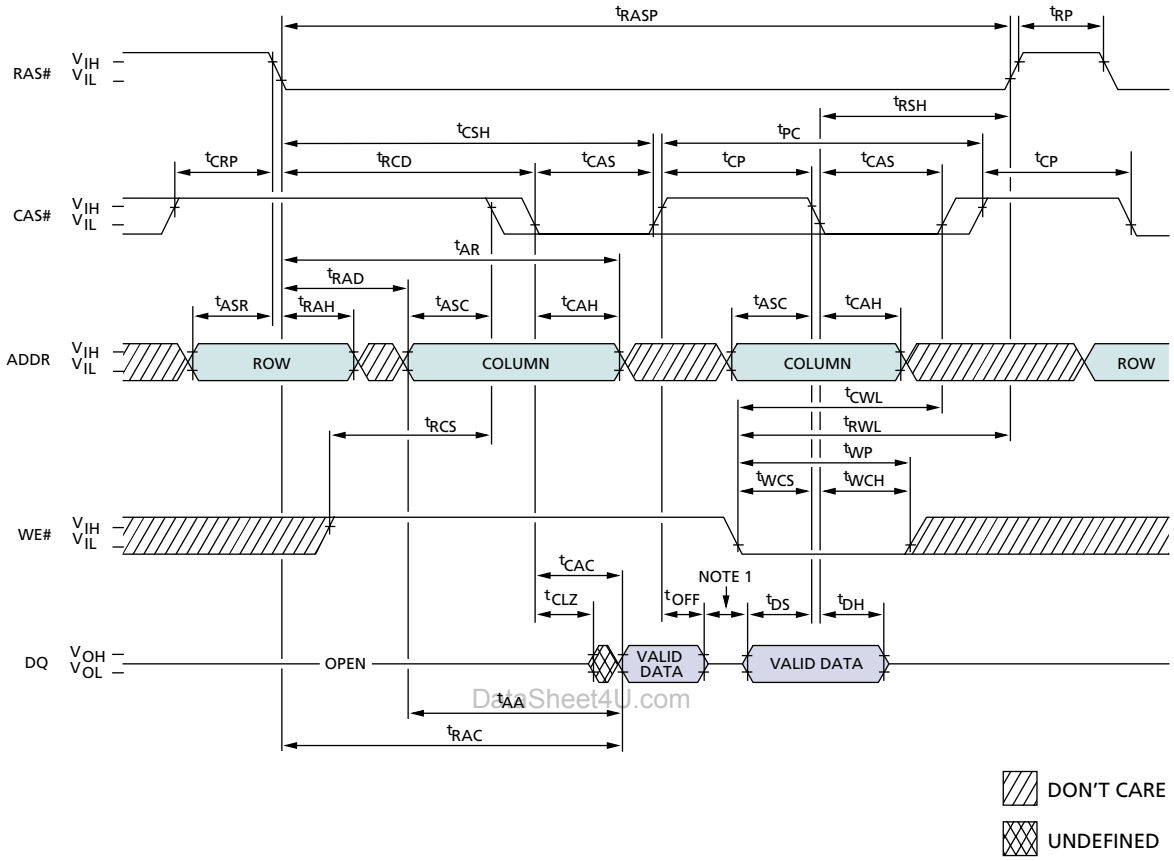


EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tACH	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCOH	3		3		ns
tCP	8		10		ns
tCPA		28		35	ns
tCRP	5		5		ns
tCSH	38		45		ns
tDH	8		10		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tDS	0		0		ns
tPC	20		25		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tWCH	8		10		ns
tWCS	0		0		ns
tWHZ	0	12	0	15	ns

FAST-PAGE-MODE READ EARLY WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



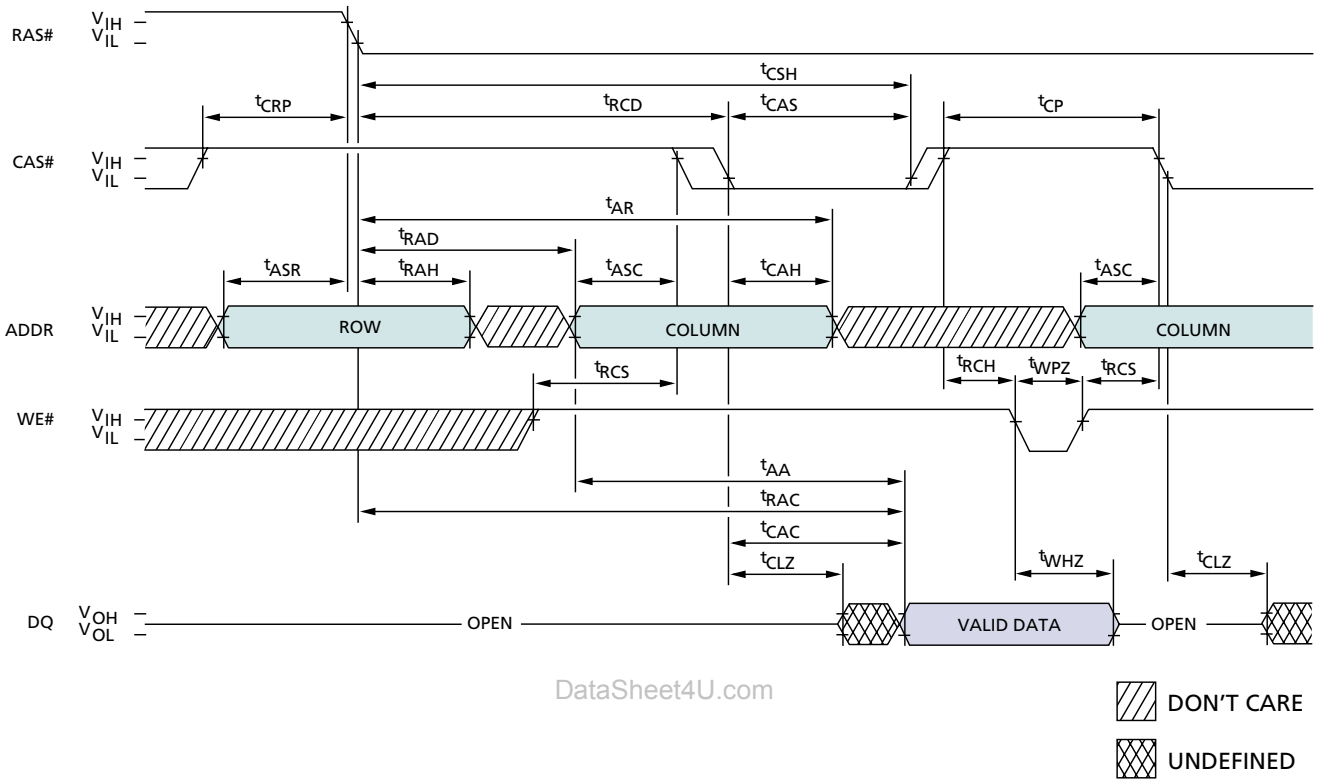
FAST PAGE MODE TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	40		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	13	10,000	15	10,000	ns
tCLZ	3		3		ns
tCP	8		10		ns
tCRP	5		5		ns
tCSH	50		60		ns
tCWL	13		15		ns
tDH	8		10		ns
tDS	0		0		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOFF	3	13	3	15	ns
tPC	30		35		ns
tRAC		50		60	ns
tRAD	13		15		ns
tRAH	8		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	18		20		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWL	13		15		ns
tWCH	8		10		ns
tWCS	0		0		ns
tWP	8		10		ns

NOTE: 1. Do not drive input data prior to output data going High-Z.

EDO READ CYCLE
(with WE#-controlled disable)

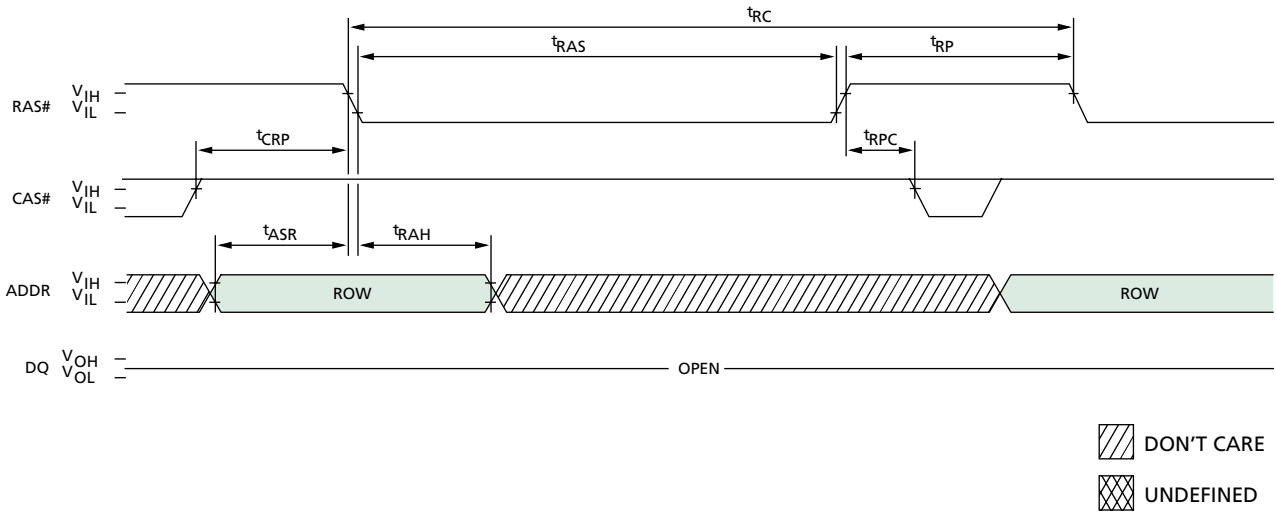


EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLZ	0		0		ns
tCP	8		10		ns
tCRP	5		5		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tCSH	38		45		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRCD	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tWHZ	0	12	0	15	ns
tWPZ	10		10		ns

RAS#-ONLY REFRESH CYCLE[24]
(OE# and WE# = DON'T CARE)

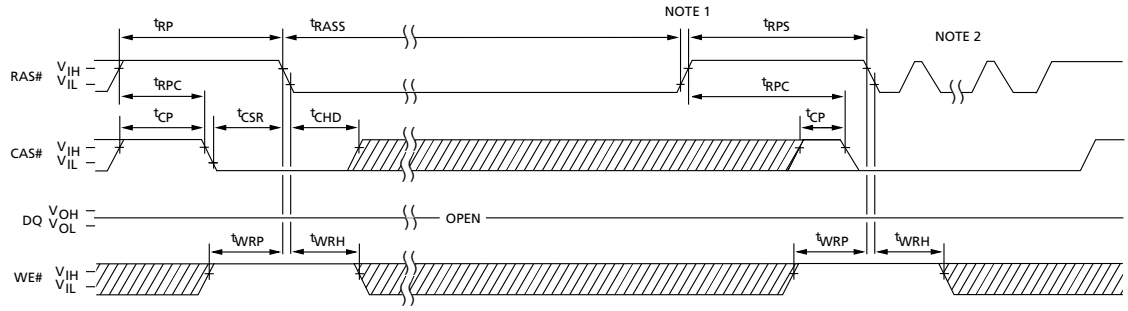


FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

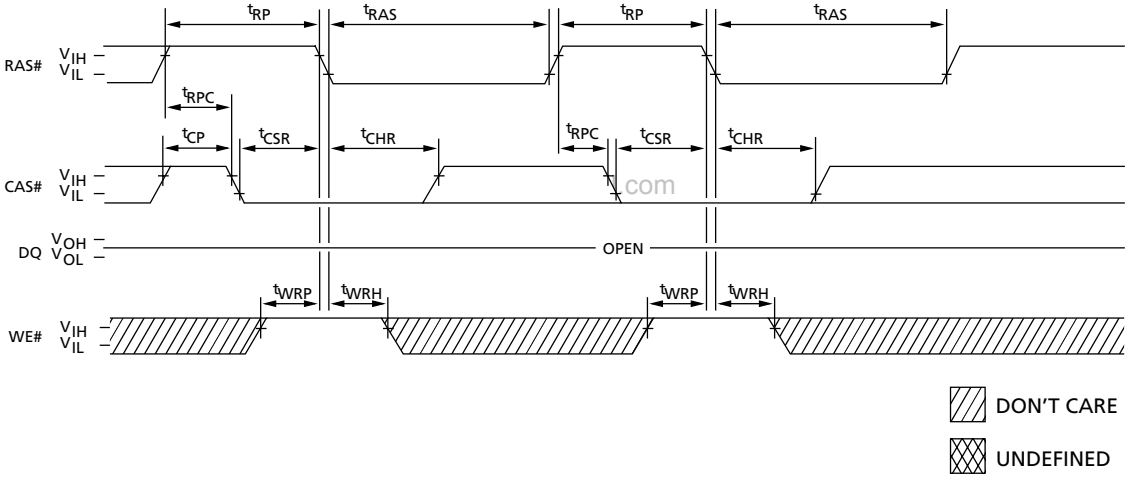
SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tASR	0		0		ns
tCRP	5		5		ns
tCSR	5		5		ns
tRAH (EDO)	9		10		ns
tRAH (FPM)	8		10		ns
tRAS	50	10,000	60	10,000	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tRC (FPM)	90		110		ns
tRC (EDO)	84		104		ns
tRP	30		40		ns
tRPC (FPM)	0		0		ns
tRPC (EDO)	5		5		ns

SELF REFRESH CYCLE [24, 25]
(Addresses = DON'T CARE)



CBR REFRESH CYCLE [24]
(Addresses = DON'T CARE)



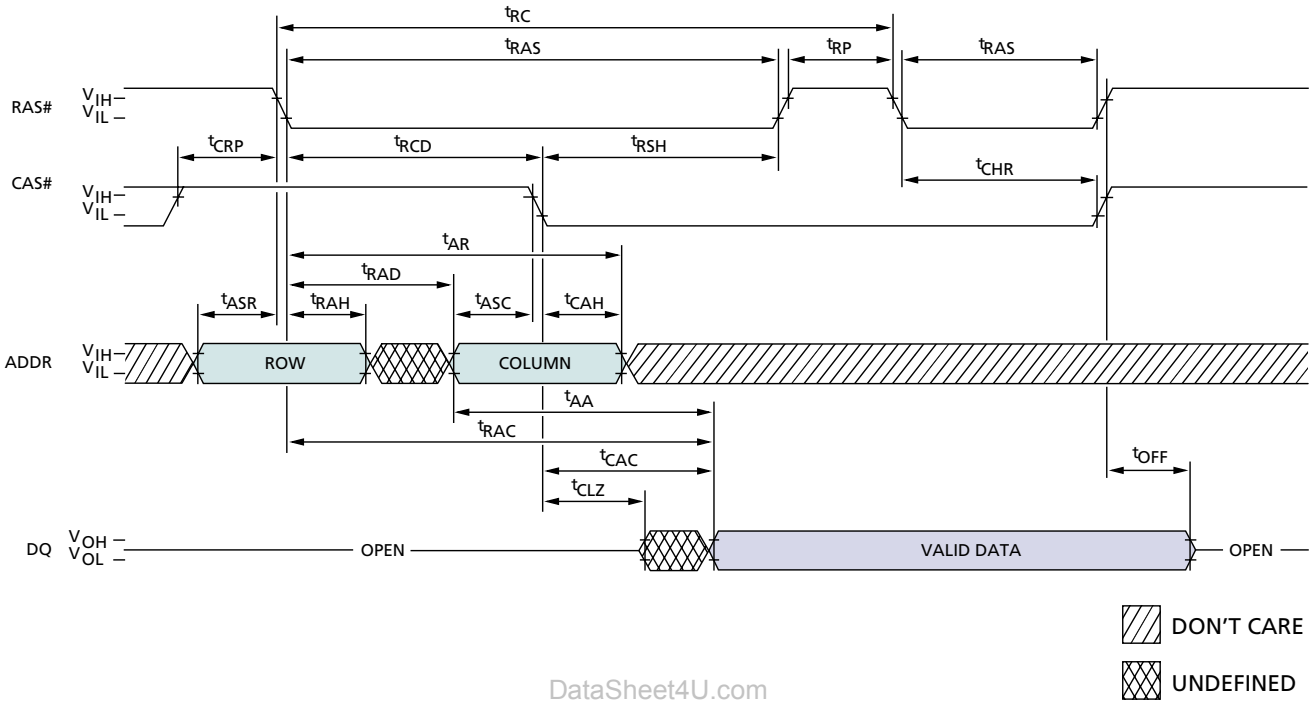
FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tCHD	15		15		ns
tCHR (FPM)	15		15		ns
tCHR (EDO)	8		10		ns
tCP	8		10		ns
tCSR	5		5		ns
tRAS	50	10,000	60	10,000	ns
tRASS	100		100		µs
tRP	30		40		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tRPC (FPM)	0		0		ns
tRPC (EDO)	5		5		ns
tRPS	90		105		ns
tWRH (FPM)	10		10		ns
tWRH (EDO)	8		10		ns
tWRP (FPM)	10		10		ns
tWRP (EDO)	8		10		ns

NOTE: 1. Once tRASS (MIN) is met and RAS# remains LOW, the DRAM will enter self refresh mode.
2. Once tRPS is satisfied, a complete burst of all rows should be executed.

HIDDEN REFRESH CYCLE [20, 24]
(WE# = HIGH)



FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

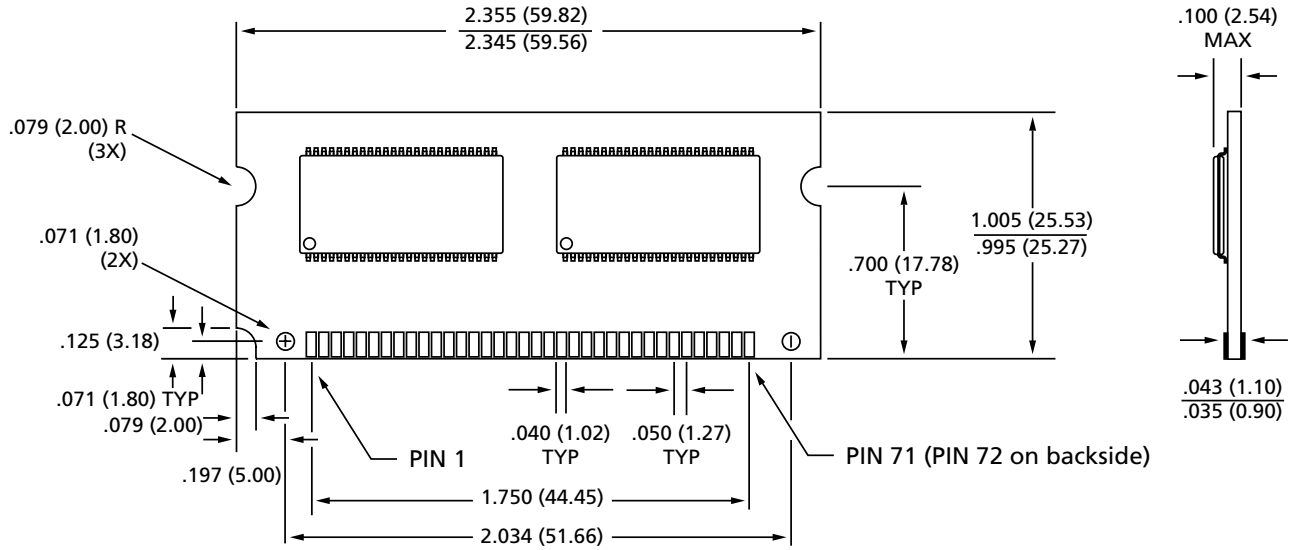
SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR (EDO)	38		45		ns
tAR (FPM)	40		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCHR (EDO)	8		10		ns
tCHR (FPM)	15		15		ns
tCLZ (EDO)	0		0		ns
tCLZ (FPM)	3		3		ns
tCRP	5		5		ns
tOFF (EDO)	0	12	0	15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOFF (FPM)	3	13	3	15	ns
tRAC		50		60	ns
tRAD (EDO)	9		12		ns
tRAD (FPM)	13		15		ns
tRAH (EDO)	9		10		ns
tRAH (FPM)	8		10		ns
tRAS	50	10,000	60	10,000	ns
tRC (EDO)	84		104		ns
tRC (FPM)	90		110		ns
tRCD (EDO)	11		14		ns
tRCD (FPM)	18		20		ns
tRP	30		40		ns
tRSH	13		15		ns

72-PIN SODIMM

(4 Meg x 32)

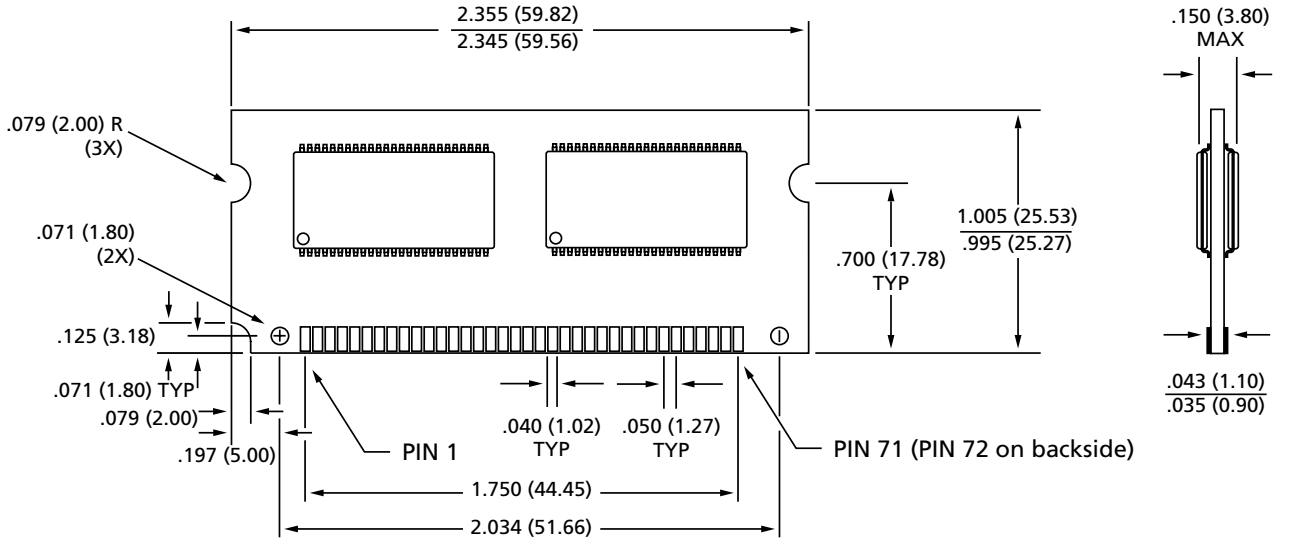
FRONT VIEW



72-PIN SODIMM

(8 Meg x 32)

FRONT VIEW



NOTE: All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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