NAND Flash Memory

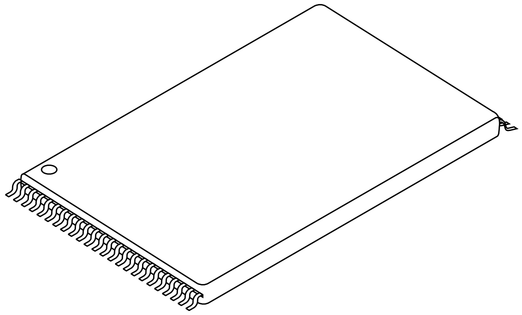
MT29F2G08AACWP, MT29F4G08BACWP, MT29F8G08FACWP

For the latest data sheet, please refer to the Micron Web site: www.micron.com/datasheets

Features

- Organization
  - Page size x8: 2,112 bytes (2,048 + 64 bytes)
  - Page size x16: 1,056 words (1,024 + 32 words)
  - Block size: 64 pages (128K + 4K bytes)
  - Device size: 2Gb: 2,048 blocks; 4Gb: 4,096 blocks; 8Gb: 8,192 blocks
- READ performance
  - RANDOM READ: 25µs
  - SEQUENTIAL READ: 30ns (3V x8 only)
- WRITE performance
  - PROGRAM PAGE: 300µs (TYP)
  - BLOCK ERASE: 2ms (TYP)
- Endurance: 100,000 PROGRAM/ERASE cycles
- First block (block address 00h) guaranteed to be valid without ECC (up to 1,000 PROGRAM/ERASE cycles)
- VCC: 1.70V–1.95V^1 or 2.7V–3.6V
- Automated PROGRAM and ERASE
- Basic NAND Flash command set:
  - PAGE READ, READ for INTERNAL DATA MOVE, RANDOM DATA READ, READ ID, READ STATUS, PROGRAM PAGE, RANDOM DATA INPUT, PROGRAM PAGE CACHE MODE, PROGRAM for INTERNAL DATA MOVE, BLOCK ERASE, RESET
- New commands:
  - PAGE READ CACHE MODE
  - One-time programmable (OTP), including: OTP DATA PROGRAM, OTP DATA PROTECT, OTP DATA READ
  - READ UNIQUE ID (contact factory)
  - READ ID2 (contact factory)
- Operation status byte provides a software method of detecting:
  - PROGRAM/ERASE operation completion
  - PROGRAM/ERASE pass/fail condition
  - Write-protect status
- READY/BUSY (R/B#) pin provides a hardware method of detecting PROGRAM or ERASE cycle completion
- PRE pin: prefetch on power up (3V device only)^2
- WP# pin: hardware write protect

Figure 1: 48-Pin TSOP Type 1



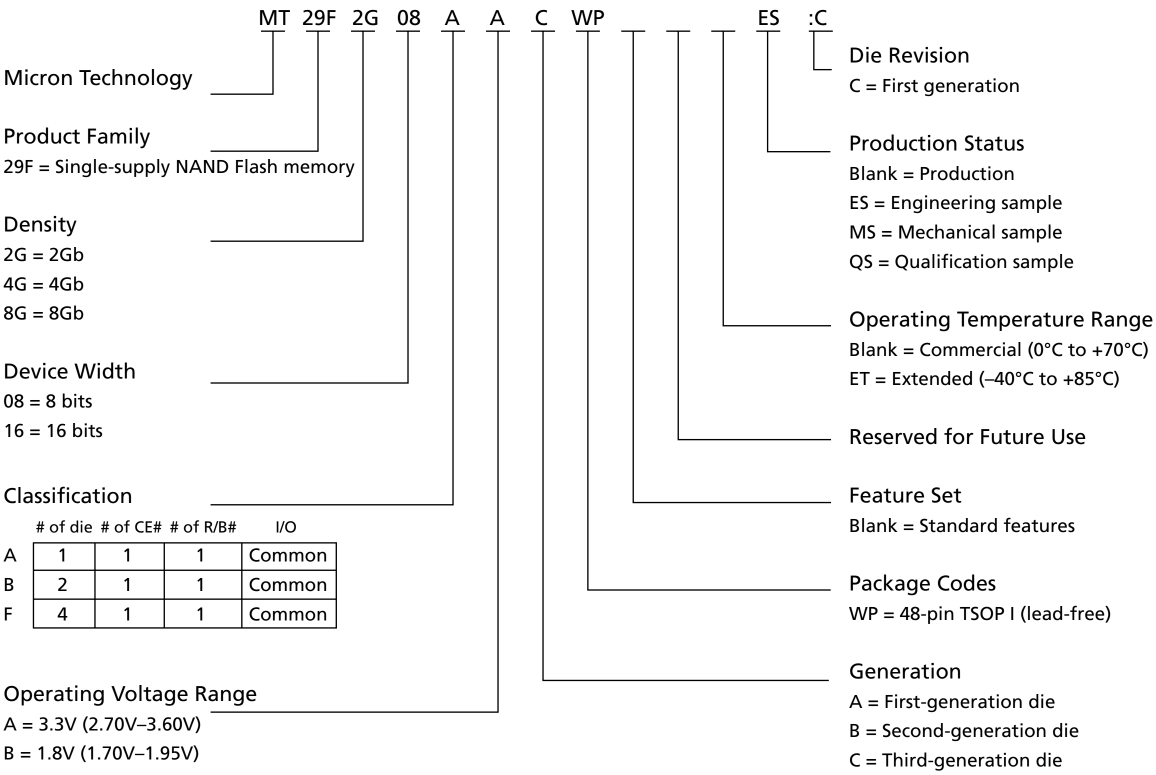
Options				Marking
Density:				
2Gb (single die)				MT29F2G
4Gb (dual-die stack)				MT29F4G
8Gb (quad-die stack)				MT29F8G
Device width:				
x8				MT29Fxx08x
x16^1				MT29Fxx16x
Configuration:				
	# of die	# of CE#	# of R/B#	
	1	1	1	A
	2	1	1	B
	4	2	2	F
VCC:				
2.7V–3.6V				A
1.70V–1.95V^1				B
Third generation die				C
Package:				
48-Pin TSOP type I (lead-free)				WP
Operating temperature:				
Commercial (0°C to 70°C)				None
Extended (–40°C to +85°C)^3				ET

Notes: 1. Packaged parts are only available for 3V x8 devices. For 1.8V or x16 devices, contact factory.
2. The PRE function is not supported on ET and 1.8V devices. Contact factory.
3. For ET devices, contact factory.

Part Numbering Information

Micron® NAND Flash devices are available in several different configurations and densities (see Figure 2).

Figure 2: Part Number Chart



	# of die	# of CE#	# of R/B#	I/O
A	1	1	1	Common
B	2	1	1	Common
F	4	1	1	Common

Valid Part Number Combinations

After building the part number from the part numbering chart above, verify that the part number is valid using the Micron Parametric Part Search at: http://www.micron.com/partsearch.

If the device required is not on this list, contact the factory.

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General Description

NAND Flash technology provides a cost-effective solution for applications requiring high-density solid-state storage. Micron MT29F2G08AxC and MT29F2G16AxC devices are 2Gb NAND Flash memory devices. The MT29F4G08BxC and MT29F4G16BxC are 4Gb devices. The MT29F8G08FAC is a four-die stack that operates as two independent 4Gb devices, providing a total storage capacity of 8Gb in a single, space-saving package. These devices include standard NAND features as well as new features designed to enhance system-level performance.

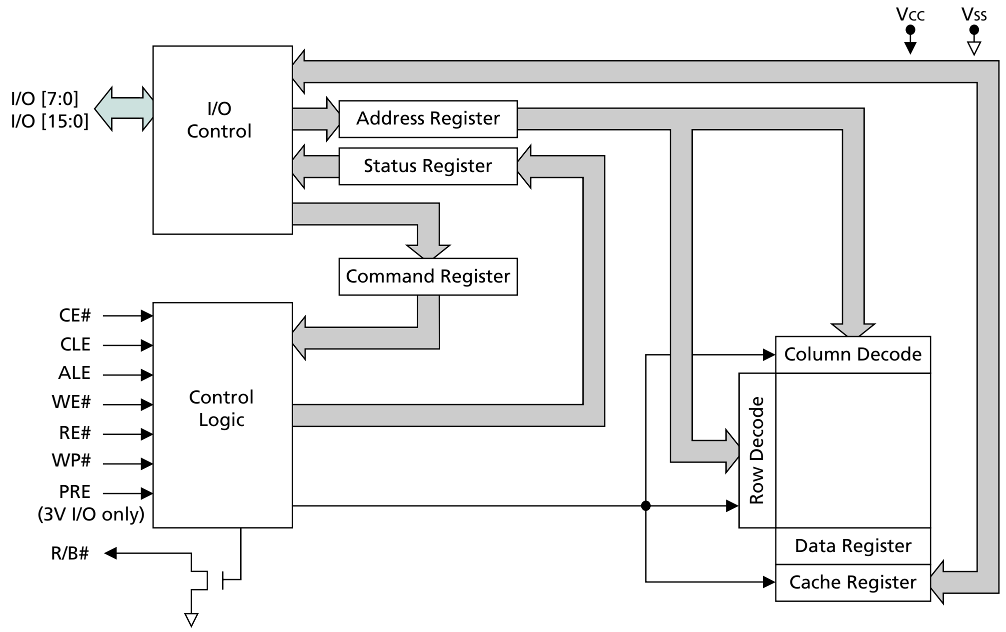
Micron NAND Flash devices use a highly multiplexed 8- or 16-bit bus (I/O[7:0] or I/O[15:0]) to transfer data, addresses, and instructions. The five command pins (CLE, ALE, CE#, RE#, WE#) implement the NAND command bus interface protocol. Three additional pins control hardware write protection (WP#), monitor device status (R/B#), and initiate the power-on AUTO-READ (PRE) feature. The PRE function is available on 3V commercial-temperature devices only.

This hardware interface creates a low-pin-count device with a standard pinout that is the same from one density to another, supporting future upgrades to higher densities without board redesign.

The MT29F2G and MT29F4G devices contain 2,048 and 4,096 erasable blocks respectively. Each block is subdivided into 64 programmable pages. Each page consists of 2,112 bytes (x8) or 1,056 words (x16). The pages are further divided into a 2,048-byte data storage region with a separate 64-byte area on the x8 device; and on the x16 device, separate 1,024-word and 32-word areas. The 64-byte and 32-word areas are typically used for error management functions.

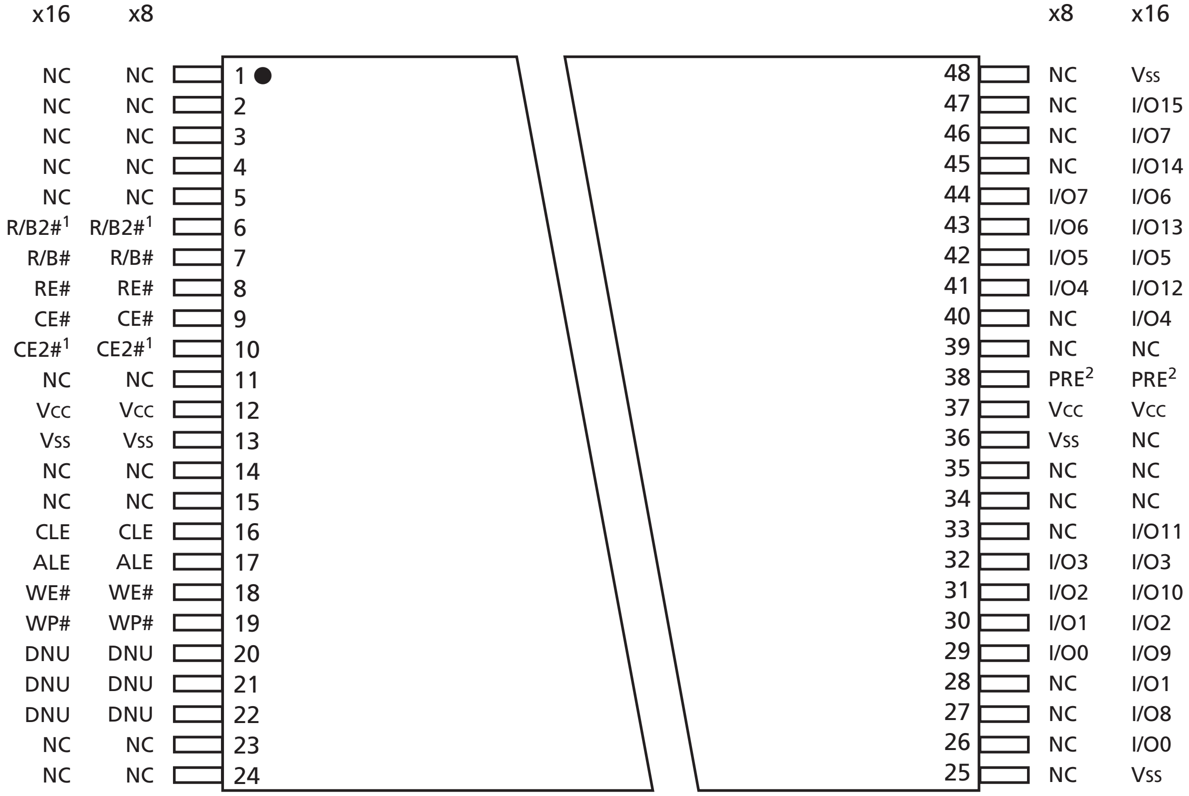
The contents of each 2,112-byte page can be programmed in 300µs, and an entire 132K-byte/66K-word block can be erased in 2ms. On-chip control logic automates PROGRAM and ERASE operations to maximize cycle endurance. ERASE/PROGRAM endurance is specified at 100K cycles when using appropriate error correcting code (ECC) and error management.

Figure 3: NAND Flash Functional Block Diagram



Note: The PRE function is not supported on extended-temperature devices.

Figure 4: 48-Pin TSOP Type 1 Pin Assignments (Top View)



Notes: 1. R/B2# and CE2# are only available on 8Gb devices. These pins are NC for other configurations.

2. The PRE function is available on 3V commercial-temperature devices. The PRE pin can be left unconnected if not in use, in which case, PRE functionality is disabled.

Table 1: Pin/Pad Descriptions

Symbol	Type	Description
ALE	Input	Address latch enable: During the time ALE is HIGH, address information is transferred from I/O[7:0] into the on-chip address register upon a LOW-to-HIGH transition on WE#. When address information is not being loaded, the ALE pin should be driven LOW.
CE#, CE2#	Input	Chip enable: Gates transfers between the host system and the NAND Flash device. Once the device starts a PROGRAM or ERASE operation, the chip enable pin can be de-asserted. For the 8Gb configuration, CE# controls the first 4Gb of memory; CE2# controls the second 4Gb. See “Bus Operation” on page 17 for additional operational details. In the 8Gb configuration, R/B# is for the 4Gb of memory enabled by CE#; R/B2# is for the 4Gb of memory enabled by the CE2#.
CLE	Input	Command latch enable: When CLE is HIGH, information is transferred from I/O[7:0] to the on-chip command register on the rising edge of WE#. When command information is not being loaded, CLE should be driven LOW.
PRE	Input	Power-on auto-read enable: When PRE is HIGH, the power-on AUTO-READ function is enabled. To disable this function, connect PRE to Vss, or leave it unconnected. The power-on AUTO-READ function is available on 3V commercial-temperature devices. On the MT29F8G08FAC, the PRE function is available only on the 4Gb of memory controlled by CE#. PRE is not available on the 4Gb of memory controlled by CE2#.
RE#	Input	Read enable: Gates transfers from the NAND Flash device to the host system.
WE#	Input	Write enable: Gates transfers from the host system to the NAND Flash device.
WP#	Input	Write protect: Pin protects against inadvertent PROGRAM and ERASE operations. All PROGRAM and ERASE operations are disabled when the WP# pin is LOW.
I/O[7:0] MT29FxG08 I/O[15:0] MT29FxG16	I/O	Data inputs/outputs: The bidirectional I/O pins transfer address, data, and instruction information. Data is output only during READ operations; at other times the I/O pins are inputs.
R/B#, R/B2#	Output	Ready/busy: An open-drain, active-LOW output that uses an external pull-up resistor, the pin is used to indicate when the chip is processing a PROGRAM or ERASE operation. The pin is also used during a READ operation to indicate when data is being transferred from the array into the serial data register. Once these operations have completed, the R/B# returns to the High-Z state.
Vcc	Supply	Vcc: Power supply.
Vss	Supply	Vss: Ground connection.
NC	–	No connect: NC pins are not internally connected. These pins can be driven or left unconnected.
DNU	–	Do not use: These pins must be left unconnected.

Architecture

These devices use NAND Flash electrical and command interfaces. Data, commands, and addresses are multiplexed onto the same pins to provide a memory device with a low pin count.

The internal memory array is accessed on a page basis. When doing reads, a page of data is copied from the memory array into the data register. Once copied to the data register, data is output sequentially, byte-by-byte on x8 devices, or word-by-word on x16 devices.

The memory array is programmed on a page basis. After the starting address is loaded into the internal address register, data is sequentially written to the internal data register up to the end of a page. After all of the page data has been loaded into the data register, array programming is started.

In order to increase programming bandwidth, this device incorporates a cache register. In the cache programming mode, data is first copied into the cache register and then into the data register. Once the data is copied into the data register, programming begins.

After the data register has been loaded and programming started, the cache register becomes available for loading additional data. Loading the next page of data into the cache register takes place while page programming is in process.

The INTERNAL DATA MOVE command also uses the internal cache register. Normally, moving data from one area of external memory to another uses a large number of external memory cycles. By using the internal cache register and data register, array data can be copied from one page and then programmed into another without using external memory cycles.

Addressing

NAND Flash devices do not contain dedicated address pins. Addresses are loaded using a five-cycle sequence as shown in Tables 4 and 5 on pages 13 and 14, respectively. See Figures 5 and 6 on pages 11 and 12 for additional memory mapping and addressing details.

Memory Mapping

Figure 5: Memory Map x8

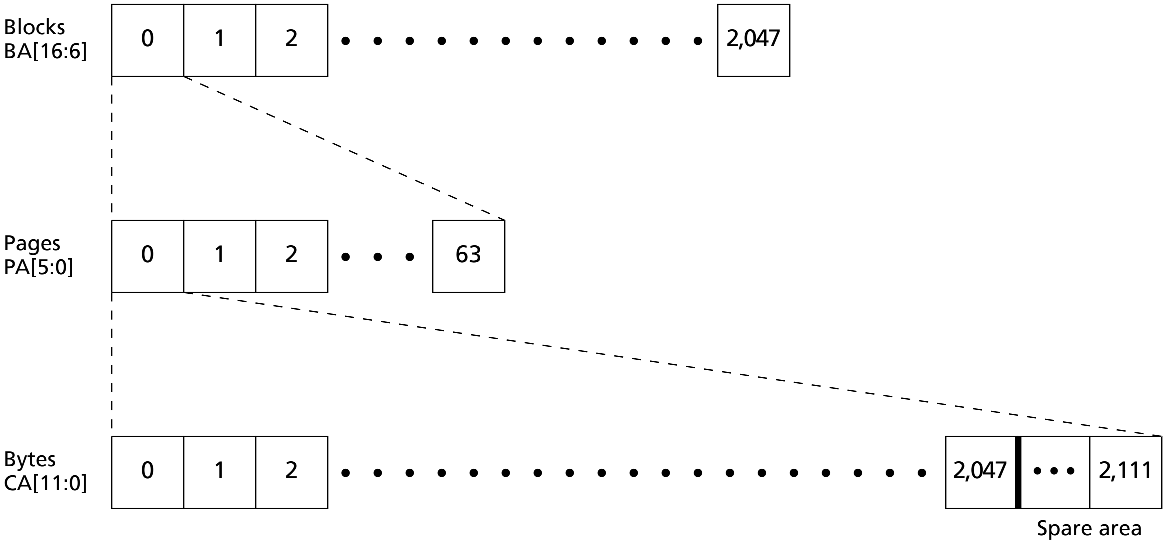


Table 2: Operational Example (x8)

Block	Page	Min Address in Page	Max Address in Page	Out of Bounds Addresses in Page
0	0	0x0000000000	0x000000083F	0x0000000840–0x0000000FFF
0	1	0x0000010000	0x000001083F	0x0000010840–0x0000010FFF
0	2	0x0000020000	0x000002083F	0x0000020840–0x0000020FFF
…	…	…	…	
2,046	62	0x01FFFE0000	0x01FFFE083F	0x01FFFE0840–0x01FFFE0FFF
2,047	63	0x01FFFF0000	0x01FFFF083F	0x01FFFF0840–0x01FFFF0FFF

Notes:
1. As shown in Table 4 on page 13, the high nibble of ADDRESS cycle 2 has no assigned address bits; however, these 4 bits must be held LOW during the ADDRESS cycle to ensure that the address is interpreted correctly by the NAND Flash device. These extra bits are accounted for in ADDRESS cycle 2 even though they do not have address bits assigned to them.
2. The 12-bit column address is capable of addressing from 0 to 4,095 bytes on x8 devices; however, only bytes 0 through 2,111 are valid. Bytes 2,112 through 4,095 of each page are “out of bounds,” do not exist in the device, and cannot be addressed.

Figure 6: Memory Map x16

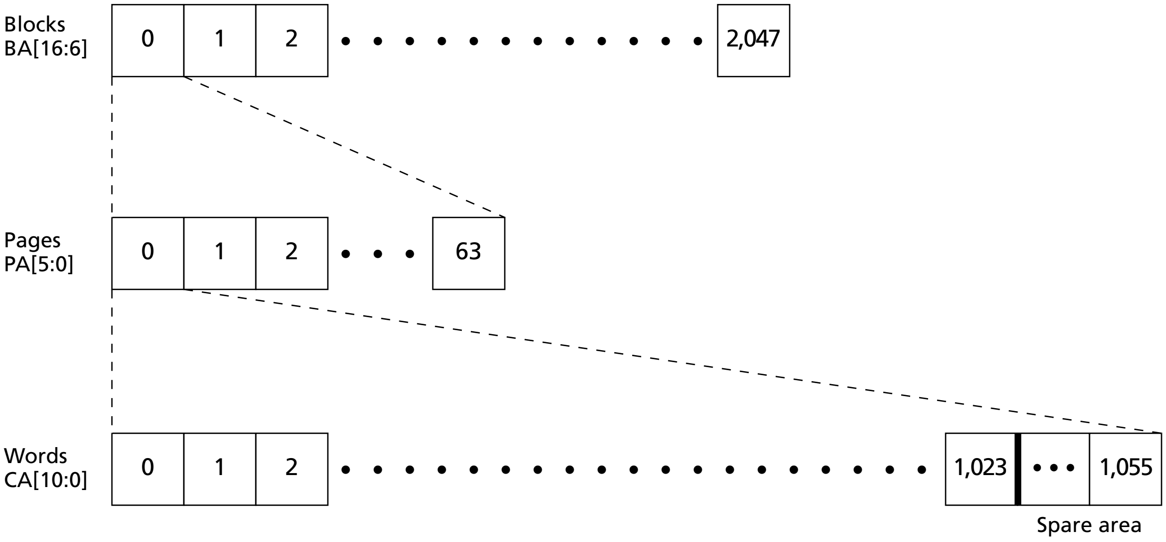


Table 3: Operational Example (x16)

Block	Page	Min Address in Page	Max Address in Page	Out of Bounds Addresses in Page
0	0	0x0000000000	0x000000041F	0x0000000420–0x0000000FFF
0	1	0x0000010000	0x000001041F	0x0000010420–0x0000010FFF
0	2	0x0000020000	0x000002041F	0x0000020420–0x0000020FFF
…	…	…	…	
2,046	62	0x01FFFE0000	0x01FFFE041F	0x01FFFE0420–0x01FFFE0FFF
2,047	63	0x01FFFF0000	0x01FFFF041F	0x01FFFF0420–0x01FFFF0FFF

Notes:
1. As shown in Table 5 on page 14, the upper 5 bits of ADDRESS cycle 2 have no assigned address bits; however, these 5 bits must be held LOW during the ADDRESS cycle to ensure that the address is interpreted correctly by the NAND Flash device. These extra bits are accounted for in ADDRESS cycle 2 even though they do not have address bits assigned to them.
2. The 11-bit column address is capable of addressing from 0 to 2,047 bytes on x16 devices; however, only bytes 0 through 1,055 are valid. Bytes 1,056 through 2,048 of each page are “out of bounds,” do not exist in the device, and cannot be addressed.

Figure 7: Array Organization for MT29F2G08AxC (x8)

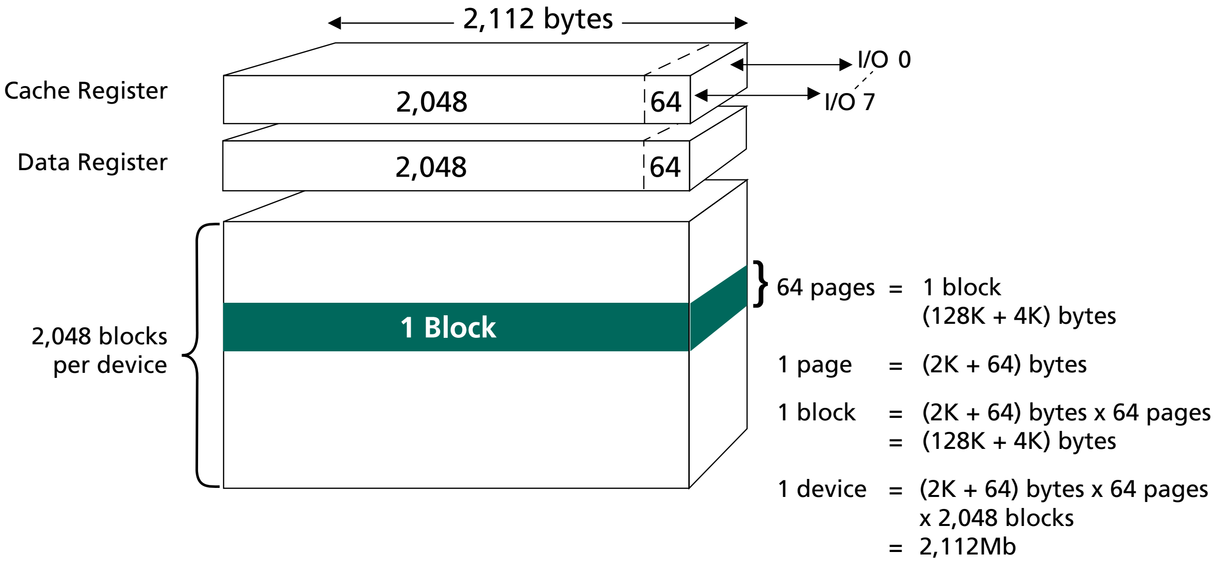
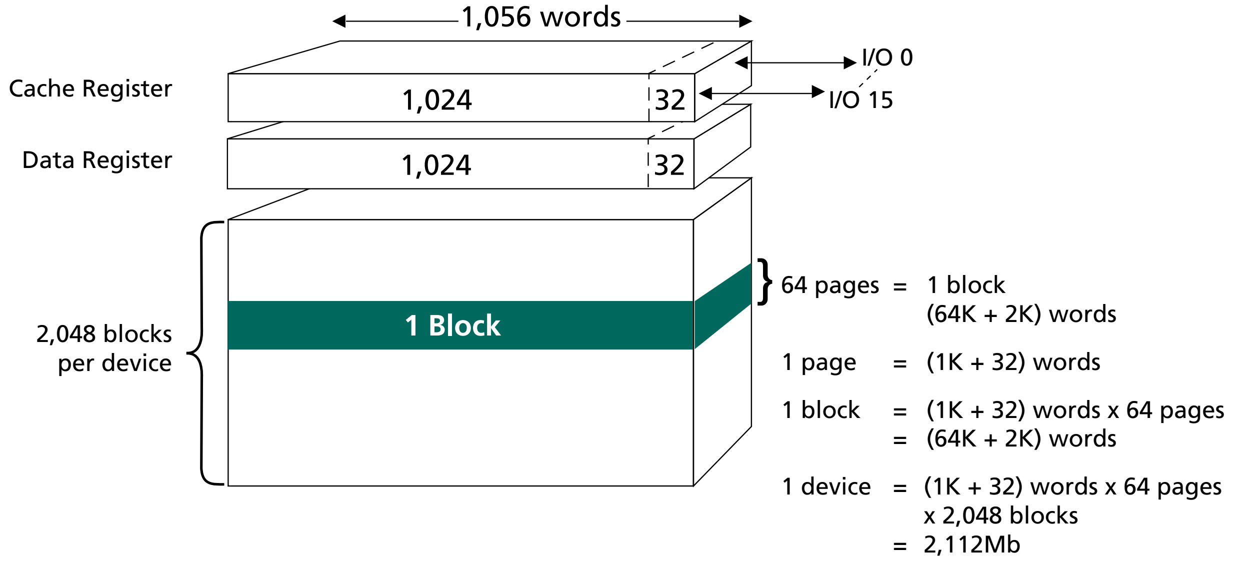


Table 4: Array Addressing: MT29F2G08AxC

Cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	LOW	CA11[1]	CA10	CA9	CA8
Third	BA7	BA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	LOW	LOW	LOW	LOW	LOW	LOW	LOW	BA16

Notes:
1. If CA11 = “1” then CA[10:6] must be “0.”
2. Block address concatenated with page address = actual page address; CAx = column address; PAx = page address, BAx = block address

Figure 8: Array Organization for MT29F2G16AxC (x16)



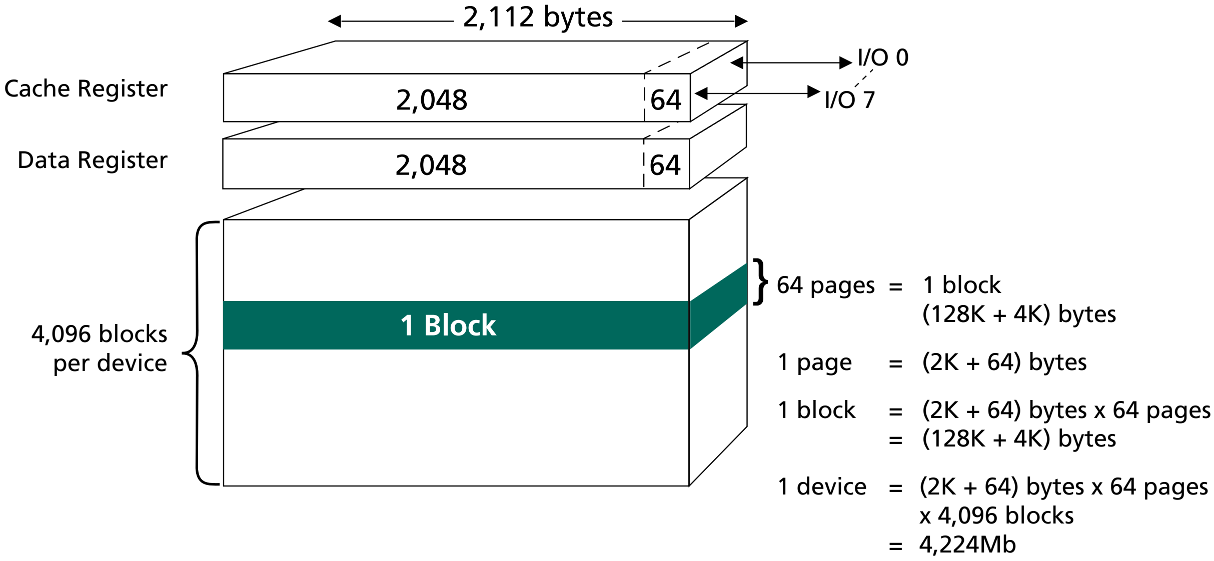
Note: For x16 devices, contact factory.

Table 5: Array Addressing: MT29F2G16AxC

Cycle	I/O[15:8]	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	LOW	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	LOW	LOW	LOW	CA10[1]	CA9	CA8
Third	LOW	BA7	BA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	LOW	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	BA16

Notes:
1. If CA10 = “1” then CA[9:5] must be “0.”
2. Block address concatenated with page address = actual page address. CAx = column address; PAx = page address, BAx = block address.
3. I/O[15:8] are not used during the addressing sequence and should be driven LOW.

Figure 9: Array Organization for MT29F4G08BxC and MT29F8G08FxC (x8)



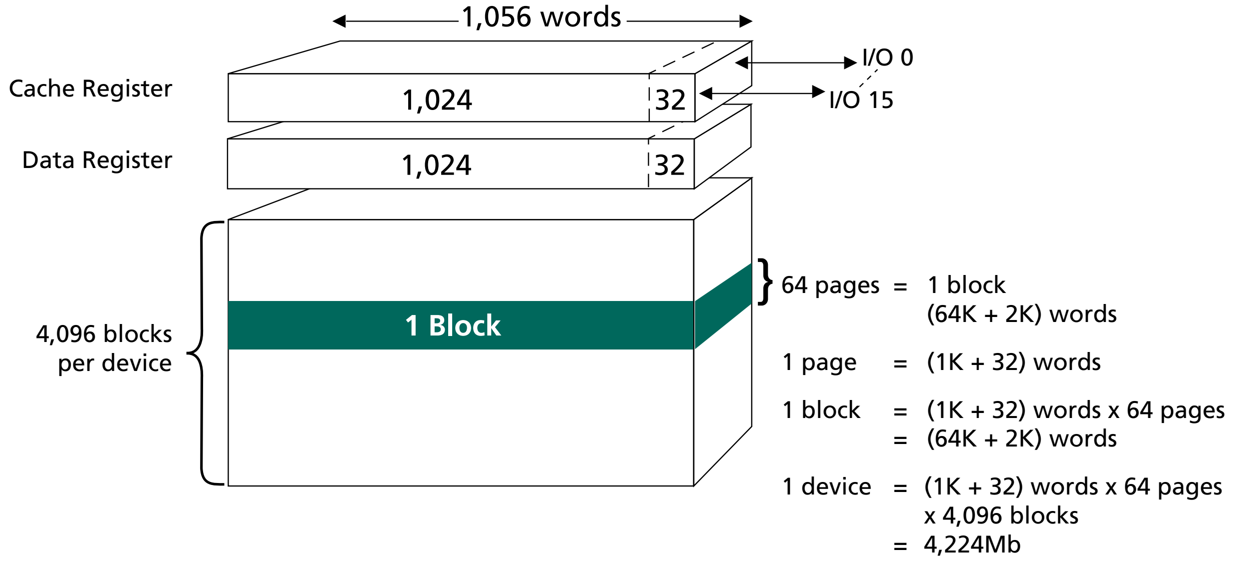
Note: For the 8Gb MT29F8G08F, the 4Gb array organization shown here applies to each chip enable (CE# and CE2#).

Table 6: Array Addressing for MT29F4G08BxC and MT29F8G08FxC (x8)

Cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	LOW	CA11[1]	CA10	CA9	CA8
Third	BA7	BA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	LOW	LOW	LOW	LOW	LOW	LOW	BA17[2]	BA16

Notes:
1. If CA11 = “1” then CA[10:6] must be “0.”
2. Die address boundary: “0” = 0Gb–2Gb devices, “1” = 2Gb–4Gb devices.
3. Block address concatenated with page address = actual page address. CAx = column address; PAx = page address, BAx = block address.

Figure 10: Array Organization for MT28F4G16BxC and MT29F8G16FxC (x16)



Notes: 1. For x16 devices, contact factory.
2. For the 8Gb MT29F8G16F, the 4Gb array organization shown here applies to each chip enable (CE# and CE2#).

Table 7: Array Addressing for MT28F4G16BxC and MT29F8G16FxC (x16)

Cycle	I/O[15:8]	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	LOW	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	LOW	LOW	LOW	CA10[1]	CA9	CA8
Third	LOW	BA7	BA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	LOW	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	LOW	LOW	LOW	LOW	LOW	LOW	LOW	BA17[2]	BA16

Notes: 1. If CA10 = “1” then CA[9:5] must be “0.”
2. Die address boundary: “0” = 0Gb–2Gb devices, “1” = 2Gb–4Gb devices.
3. Block address concatenated with page address = actual page address. CAx = column address; PAx = page address, BAx = block address.
4. I/O[15:8] are not used during the addressing sequence and should be driven LOW.

Bus Operation

The bus on the MT29Fxxx devices is multiplexed. Data I/O, addresses, and commands all share the same pins. I/O pins I/O[15:8] are used only for data in the x16 configuration. Addresses and commands are always supplied on I/O[7:0].

The command sequence normally consists of a command latch cycle, an ADDRESS LATCH cycle, and a DATA cycle—either READ or WRITE.

Control Signals

CE#, WE#, RE#, CLE, ALE and WP# control NAND Flash device READ and WRITE operations. On the 8Gb MT29F8G08FAC, CE# and CE2# each control independent 4Gb arrays. CE2# functions the same as CE# for its own array; all operations described for CE# also apply to CE2#.

CE# is used to enable the device. When CE# is LOW and the device is not in the busy state, the NAND Flash memory will accept command, data, and address information.

When the device is not performing an operation, CE# is typically driven HIGH and the device enters standby mode. The memory will enter standby if CE# goes HIGH while data is being transferred and the device is not busy. This helps reduce power consumption. See Figure 43 on page 49 and Figure 51 on page 55 for examples of CE# "Don't Care" operations.

The CE# "Don't Care" operation enables the NAND Flash to reside on the same asynchronous memory bus as other Flash or SRAM devices. Other devices on the memory bus can then be accessed while the NAND Flash is busy with internal operations. This capability is important for designs that require multiple NAND devices on the same bus. One device can be programmed while another is being read.

A HIGH CLE signal indicates that a command cycle is taking place. A HIGH ALE signal signifies that an address input cycle is occurring.

Commands

Commands are written to the command register on the rising edge of WE# when:

- CE# and ALE are LOW, and
- CLE is HIGH, and
- the device is not busy.

The exceptions to this are the READ STATUS and RESET commands when busy. See Figure 37 on page 46 for detailed timing requirements.

Commands are input on I/O[7:0] only. For devices with a x16 interface, I/O[15:8] must be written with zeros when issuing a command.

Address Input

Addresses are written to the address register on the rising edge of WE# when:

- CE# and CLE are LOW, and
- ALE is HIGH, and
- the device is not busy.

Addresses are input on I/O[7:0] only; bits not part of the address space must be LOW. For devices with a x16 interface, I/O[15:8] must be written with zeros when issuing an address.

The number of ADDRESS cycles required for each command varies. Refer to the command descriptions to determine addressing requirements. (See Table 9 on page 22.)

Data Input

Data is written to the data register on the rising edge of WE# when:

- CE#, CLE, and ALE are LOW, and
- the device is not busy.

Data is input on I/O[7:0] for x8 devices, and I/O[15:0] on x16 devices. See Figure 39 on page 47 for additional data input details.

READs

After a READ command is issued, data is transferred from the memory array to the data register on the rising edge of WE#. R/B# goes LOW for ^{t}R and transitions HIGH after the transfer is complete. When R/B# goes HIGH, data is available in the data register, and is clocked out of the part by toggling RE#. See Figure 42 on page 48 for detailed timing information.

The READ STATUS (70h) command or the R/B# signal can be used to determine when the device is ready. See the READ STATUS command section on page 28 for details.

Ready/Busy#

The R/B# output provides a hardware method of indicating the completion of PROGRAM, ERASE, and READ operations. The signal requires a pull-up resistor for proper operation. The signal is typically HIGH, and transitions to LOW after the appropriate command is written to the device. The signal pin's open-drain driver enables multiple R/B# outputs to be OR-tied. The READ STATUS command can be used in place of R/B#. Typically R/B# is connected to an interrupt pin on the system controller (see Figure 13 on page 19).

On the 8Gb MT29F8G08FAC, R/B# provides a status indication for the 4Gb section enabled by CE#, and R/B2# does the same for the 4Gb section enabled by CE2#. R/B# and R/B2# can be tied together, or they can be used separately to provide independent indications for each 4Gb section.

The combination of Rp and capacitive loading of the R/B# circuit determines the rise time of the R/B# pin. The actual value used for Rp depends on the system timing requirements. Large values of Rp cause R/B# to be delayed significantly. At the 10- to 90-percent points on the R/B# waveform, rise time is approximately two time constants (TC).

Figure 11: Time Constants

$TC = R \times C$

Where R = Rp (resistance of pull-up resistor), and C = total capacitive load.

The fall time of the R/B# signal is determined mainly by the output impedance of the R/B# pin and the total load capacitance.

Refer to Figure 14 on page 19, and Figure 15 on page 20, which depict approximate Rp values using a circuit load of 100pF.

The minimum value for Rp is determined by the output drive capability of the R/B# signal, the output voltage swing, and VCC.

Figure 12: Minimum Rp

$$\text{Rp (MIN, 1.8V part)} = \frac{V_{CC}\text{ (MAX)} - V_{OL}\text{ (MAX)}}{I_{OL} + \Sigma I_L} = \frac{1.85\text{V}}{3\text{mA} + \Sigma I_L}$$

$$\text{Rp (MIN, 3.3V part)} = \frac{V_{CC}\text{ (MAX)} - V_{OL}\text{ (MAX)}}{I_{OL} + \Sigma I_L} = \frac{3.2\text{V}}{8\text{mA} + \Sigma I_L}$$

Where ΣI_L is the sum of the input currents
of all devices tied to the R/B# pin.

Figure 13: READY/BUSY# Open Drain

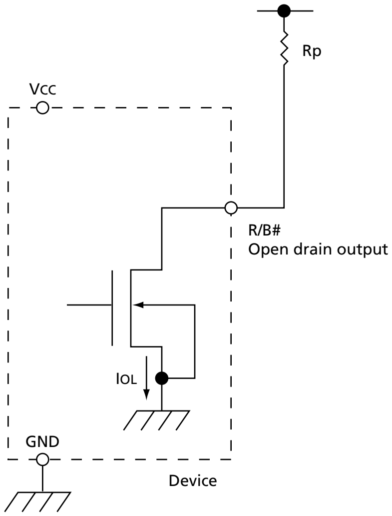
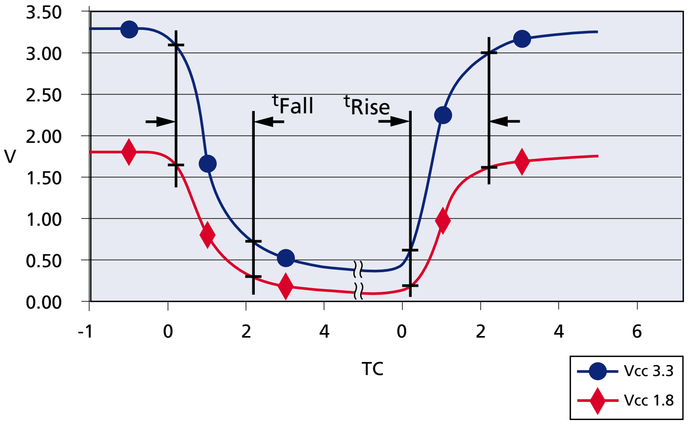


Figure 14: ^{t}Fall and ^{t}Rise



Notes:
1. ^{t}Fall and ^{t}Rise calculated at 10 percent and 90 percent points.
2. ^{t}Rise primarily dependent on external pull-up resistor and external capacitive loading.
3. ^{t}Fall ≈ 10ns at 3.3V; ^{t}Fall ≈ 7ns at 1.8V.

Figure 15: I_{OL} vs. Rp

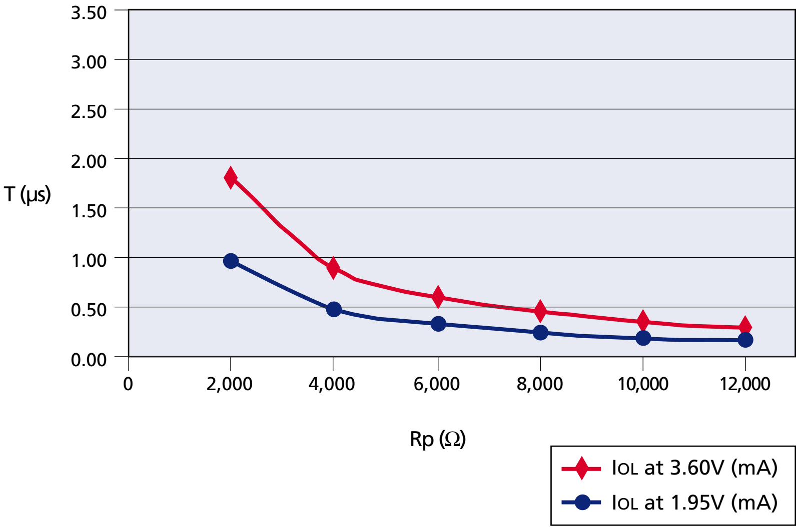


Table 8: Mode Selection

CLE	ALE	CE#	WE#	RE#	WP#[1]	PRE[2]	Mode	
H	L	L	↑	H	X	X	Read mode	Command input
L	H	L	↑	H	X	X		Address input
H	L	L	↑	H	H	X	Write mode	Command input
L	H	L	↑	H	H	X		Address input
L	L	L	↑	H	H	X	Data input	
L	L	L	H	↓	X	X	Sequential read and data output	
L	L	L	H	H	X	X	During read (busy)	
X	X	X	X	X	H	X	During program (busy)	
X	X	X	X	X	H	X	During erase (busy)	
X	X	X	X	X	L	X	Write protect	
X	X	H	X	X	0V/Vcc	0V/Vcc	Standby	

Notes:
1. WP# should be biased to CMOS HIGH or LOW for standby.
2. Do not transition PRE during device operations. PRE is only supported on 3V devices and can be left unconnected if not used. PRE is not supported on extended-temperature devices.
3. H = Logic level HIGH; L = Logic level LOW; X = V_{IH} or V_{IL}

Power-On AUTO-READ

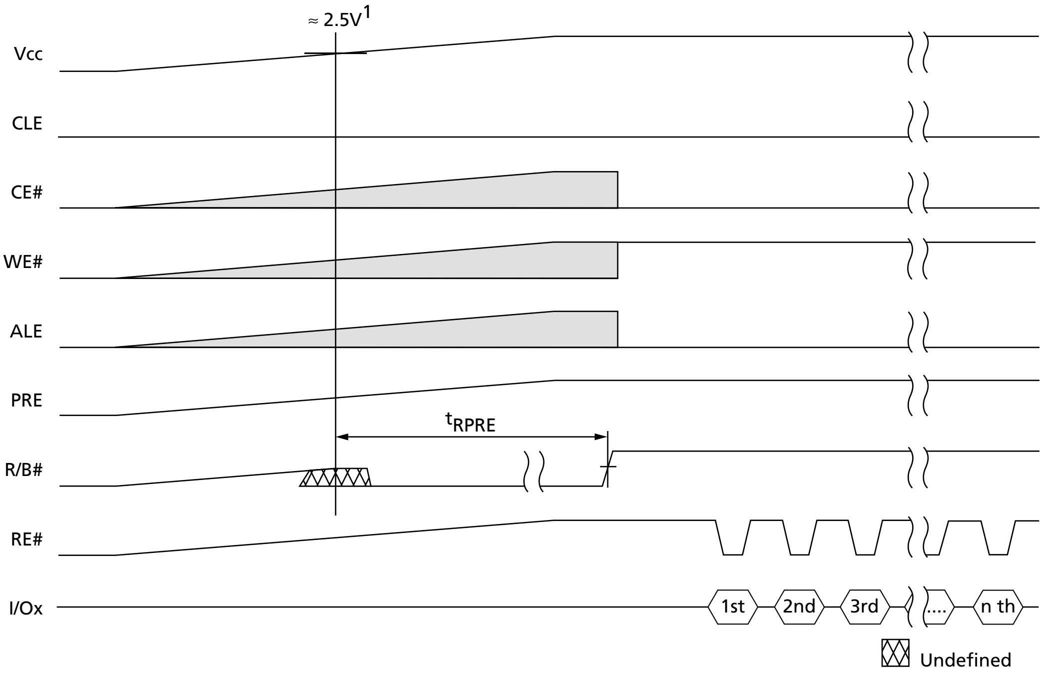
During power-on, with the PRE pin at VCC, 3V devices automatically transfer the first page of the memory array to the data register without requiring a command or address-input sequence. After VCC reaches approximately 2.5V, the internal voltage detector initiates the power-on AUTO-READ function.

R/B# will stay LOW (^{t}RPRE) while the first page of data is copied into the data register. See Table 21 on page 45 for ^{t}RPRE values. Once the READ is complete and R/B# goes HIGH, RE# can be toggled repeatedly to output the first page of data.

If connected, PRE must be set to 0V or VCC at power-on, and must not be toggled during device operations. PRE can be left unconnected if not used, in which case, PRE functionality is disabled.

The power-on AUTO-READ function is available only on 3V commercial-temperature devices.

Figure 16: First Page Power-On AUTO-READ (3V devices only)



Notes: 1. Verified per device characterization; not 100 percent tested on all devices.

Command Definitions

Table 9: Command Set

Operation	Command Cycle 1	Number of Address Cycles	Data Cycles Required[1]	Command Cycle 2	Valid During Busy	Notes
PAGE READ	00h	5	No	30h	No	
PAGE READ CACHE MODE START	31h	–	No	–	No	
PAGE READ CACHE MODE START LAST	3Fh	–	No	–	No	
READ for INTERNAL DATA MOVE	00h	5	No	35h	No	2
RANDOM DATA READ	05h	2	No	E0h	No	3
READ ID	90h	1	No	–	No	
READ STATUS	70h	–	No	–	Yes	
PROGRAM PAGE	80h	5	Yes	10h	No	
PROGRAM PAGE CACHE MODE	80h	5	Yes	15h	No	
PROGRAM for INTERNAL DATA MOVE	85h	5	Optional	10h	No	2
RANDOM DATA INPUT	85h	2	Yes	–	No	4
BLOCK ERASE	60h	3	No	D0h	No	
RESET	FFh	–	No	–	Yes	
OTP DATA PROGRAM	A0h	5	Yes	10h	No	
OTP DATA PROTECT	A5h	5	No	10h	No	
OTP DATA READ	AFh	5	No	30h	No	

Notes:
1. Indicates required data cycles between command cycle 1 and command cycle 2.
2. Do not cross die boundaries when using READ for INTERNAL DATA MOVE and PROGRAM for INTERNAL DATA MOVE.
3. RANDOM DATA READ command limited to use within a single page.
4. RANDOM DATA INPUT command limited to use within a single page.

READ Operations

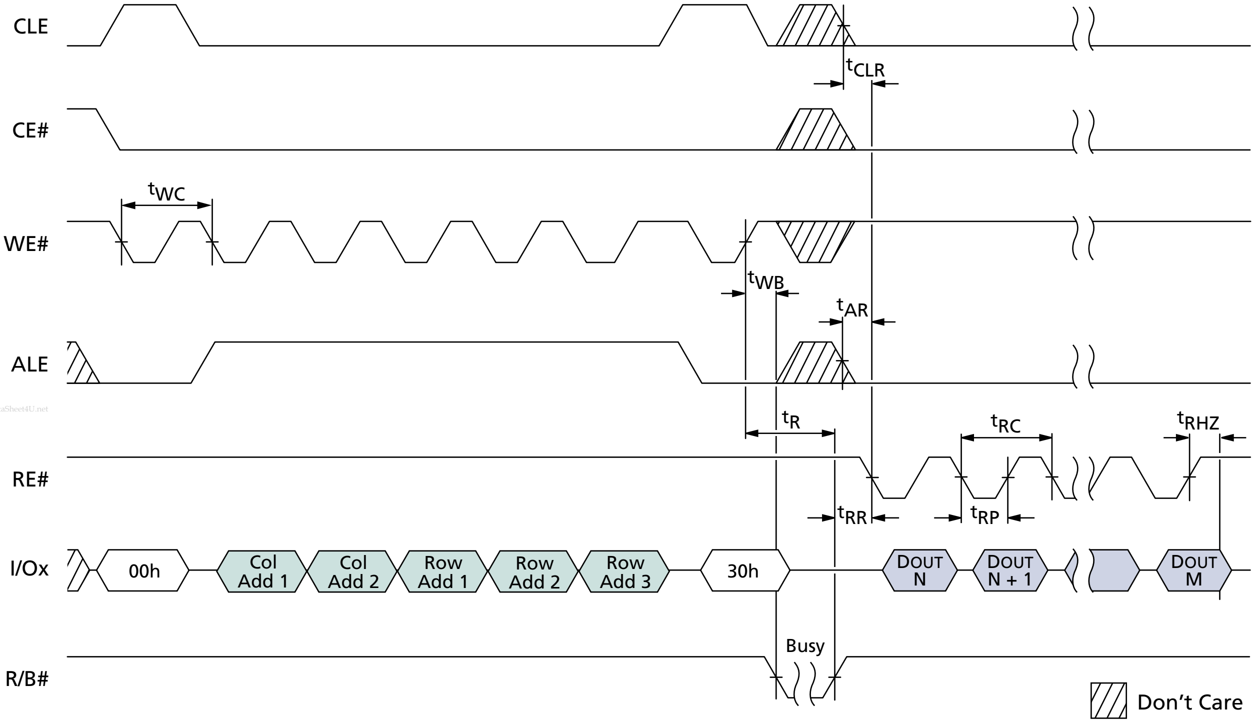
PAGE READ 00h-30h

On initial power up, the device defaults to read mode. To enter the read mode while in operation, write the 00h command to the command register, then write five ADDRESS cycles followed by the 30h command.

To determine the progress of the data transfer from the NAND Flash array to the data register (^{t}R), monitor the R/B# signal; or alternately, issue a READ STATUS (70h) command. If the READ STATUS command is used to monitor the data transfer, the user must re-issue the READ (00h) command to receive data output from the data register. See Figure 47 on page 52 and Figure 48 on page 53 for examples. After the READ command has been re-issued, pulsing the RE# line will result in outputting data, starting from the initial column address.

A serial page read sequence outputs a complete page of data. After 30h is written, the page data is transferred to the data register, and R/B# goes LOW during the transfer. When the transfer to the data register is complete, R/B# returns HIGH. At this point, data can be read from the device. Starting from the initial column address to the end of the page, read the data by repeatedly pulsing RE# at the maximum ^{t}RC rate (see Figure 17).

Figure 17: PAGE READ Operation



RANDOM DATA READ 05h-E0h

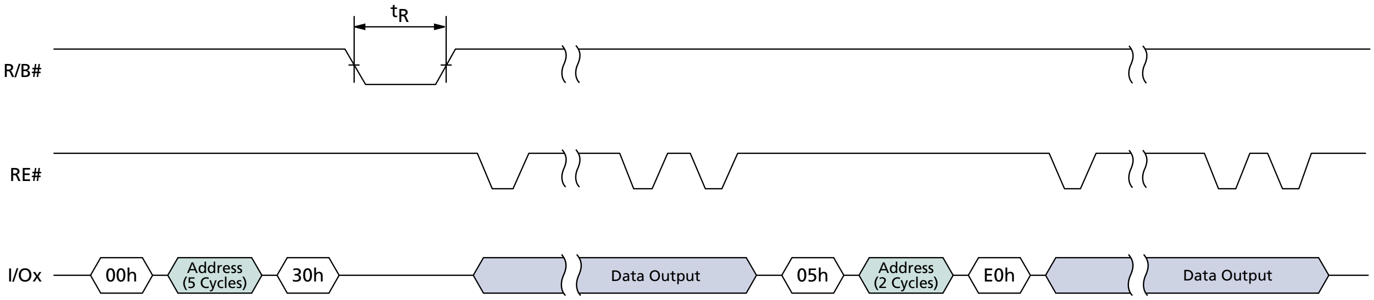
The RANDOM DATA READ command enables the user to specify a new column address so the data at single or multiple addresses can be read. The random read mode is enabled after a normal PAGE READ (00h-30h) sequence.

Random data can be output after the initial page read by writing an 05h-E0h command sequence along with the new column address (two cycles).

The RANDOM DATA READ command can be issued without limit within the page.

Only data on the current page can be read. Pulsing the RE# pin outputs data sequentially (see Figure 18).

Figure 18: RANDOM DATA READ Operation



PAGE READ CACHE MODE Start 31h; PAGE READ CACHE MODE Start Last 3Fh

Micron NAND Flash devices have a cache register that can be used to increase the READ operation speed when accessing sequential pages in a block.

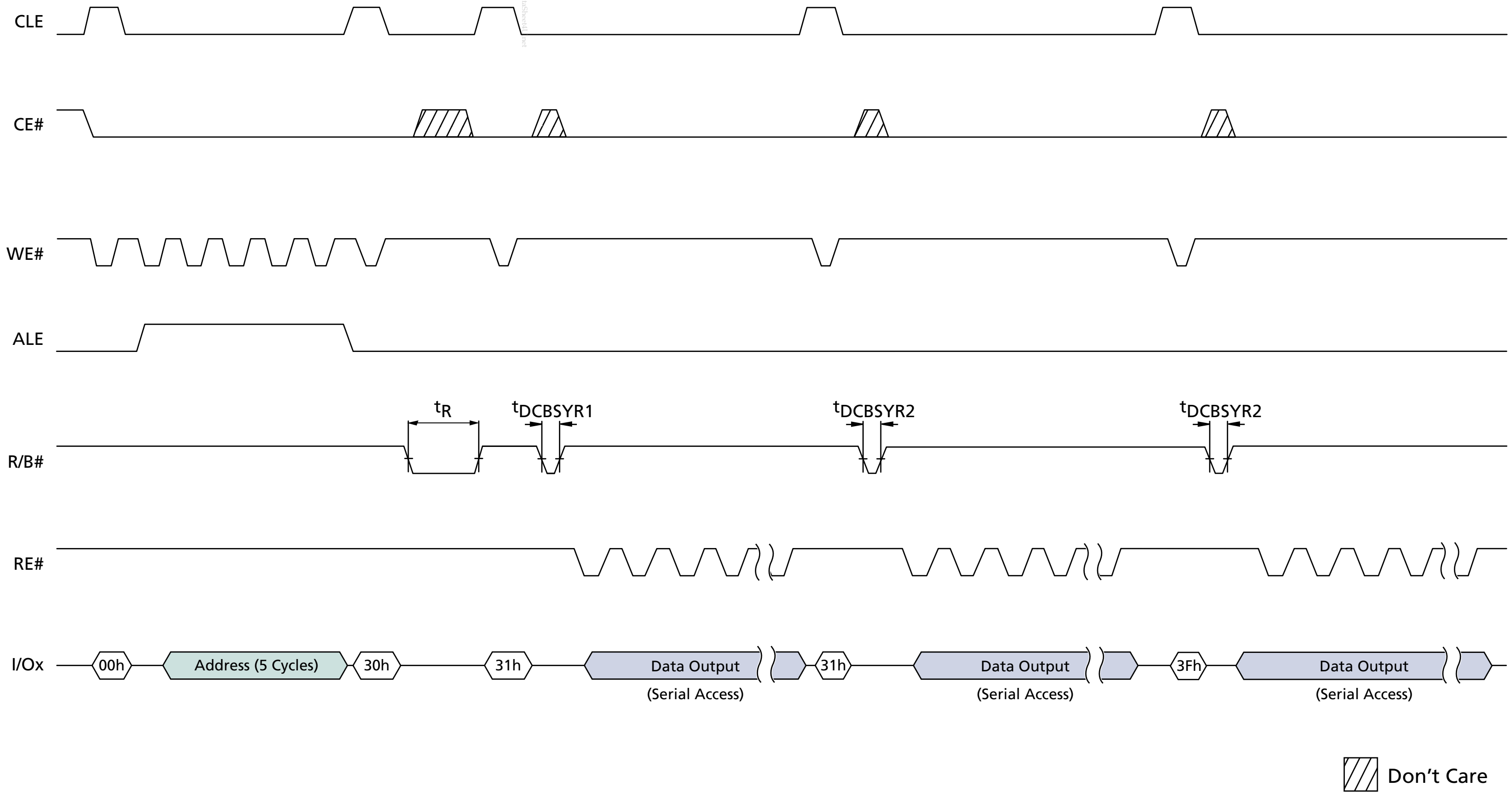
First, a normal PAGE READ (00h-30h) command sequence is issued. See Figure 19 on page 25 for operation details. The R/B# signal goes LOW for ^tR during the time it takes to transfer the first page of data from the memory to the data register. After R/B# returns to HIGH, the PAGE READ CACHE MODE START (31h) command is latched into the command register. R/B# goes LOW for $^tDCBSYR1$ while data is being transferred from the data register to the cache register. Once the data register contents are transferred to the cache register, another PAGE READ is automatically started as part of the 31h command. Data is transferred from the next sequential page of the memory array to the data register during the same time data is being read serially (pulsing of RE#) from the cache register. If the total time to output data exceeds ^tR, then the PAGE READ is hidden.

The second and subsequent pages of data are transferred to the cache register by issuing additional 31h commands. R/B# will stay LOW up to $^tDCBSYR2$. This time can vary, depending on whether the previous memory-to-data-register transfer was completed prior to issuing the next 31h command. See Table 21 on page 45 for timing parameters. If the data transfer from memory to the data register is not completed before the 31h command is issued, R/B# stays LOW until the transfer is complete.

It is not necessary to output a whole page of data before issuing another 31h command. R/B# will stay LOW until the previous PAGE READ is complete and the data has been transferred to the cache register.

To read out the last page of data, the PAGE READ CACHE MODE START LAST (3Fh) command is issued. This command transfers data from the data register to the cache register without issuing another PAGE READ (see Figure 19 on page 25).

Figure 19: PAGE READ CACHE MODE

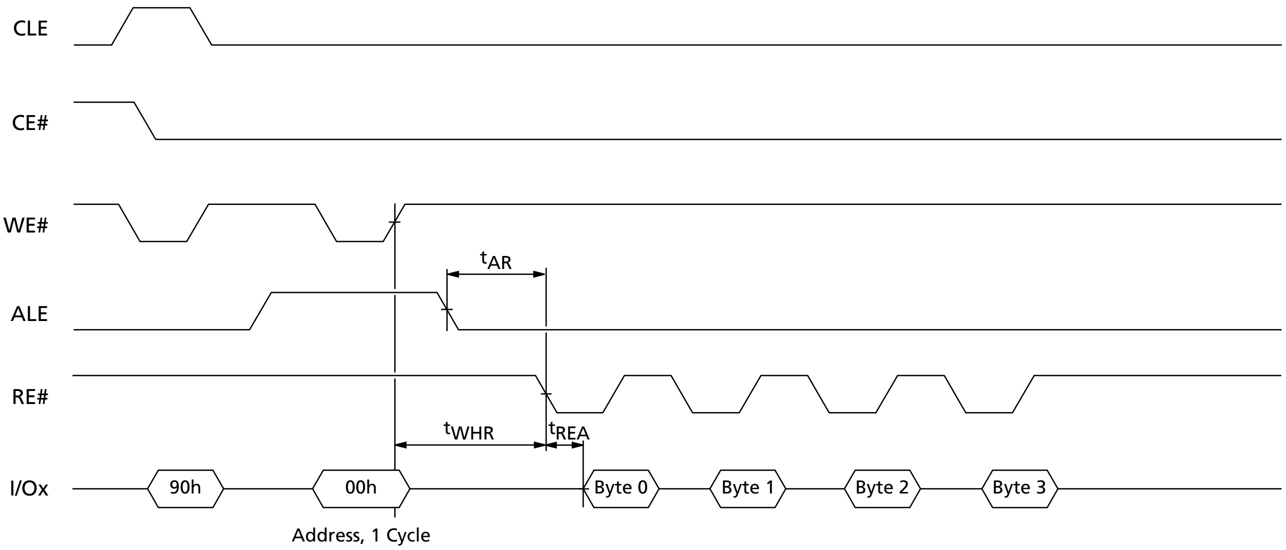


READ ID 90h

The READ ID (90h) command is used to read the 4 bytes of identifier codes programmed into the devices. The READ ID command reads a 4-byte table that includes manufacturer ID, device configuration, and part-specific information. (See Table 10 on page 27.)

Writing 90h to the command register puts the device into the read ID mode. The command register stays in this mode until another valid command is issued (see Figure 20)**.**

Figure 20: READ ID Operation



Notes: 1. See Table 10 on page 27 for byte definitions.

Table 10: Device ID and Configuration Codes

	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value[1]	Notes
Byte 0	Manufacturer ID										
	Micron	0	0	1	0	1	1	0	0	2Ch	
Byte 1	Device ID										
MT29F2G08AAC	2Gb, x8, 3V	1	1	0	1	1	0	1	0	DAh	
MT29F2G08ABC	2Gb, x8, 1.8V	1	0	1	0	1	0	1	0	AAh	2
MT29F2G16AAC	2Gb, x16, 3V	1	1	0	0	1	0	1	0	CAh	2
MT29F2G16ABC	2Gb, x16, 1.8V	1	0	1	1	1	0	1	0	BAh	2
MT29F4G08BAC	4Gb, x8, 3V	1	1	0	1	1	1	0	0	DCh	
MT29F8G08FAC	8Gb, x8, 3V	1	1	0	1	1	1	0	0	DCh	3
Byte 2											
Byte value	Don't Care	x	x	x	x	x	x	x	x	XXh	
Byte 3											
Page size	2KB							0	1	01b	
Spare area size (bytes)	64					0	1			01b	
Block size (w/o spare)	128KB			0	1					01b	
Organization	x8		0							0b	
	x16		1							1b	
Reserved		0								0b	
Byte value	x8	0	0	0	1	0	1	0	1	15h	
	x16	0	1	0	1	0	1	0	1	55h	

Notes:
1. b = binary; h = hex.
2. Device IDs for these configurations are provided for reference only.
3. The MT29F8G08FAC device ID code reflects the configuration of each 4Gb section.

READ STATUS 70h

NAND Flash devices have an 8-bit status register that the software can read during device operation. On the x16 device, I/O[15:8] are “0” when reading the status register. Table 11 describes the status register.

After a READ STATUS command, all READ cycles will be from the status register until a new command is issued. Changes in the status register will be seen on I/O[7:0] as long as CE# and RE# are LOW; it is not necessary to start a new READ STATUS cycle to see these changes.

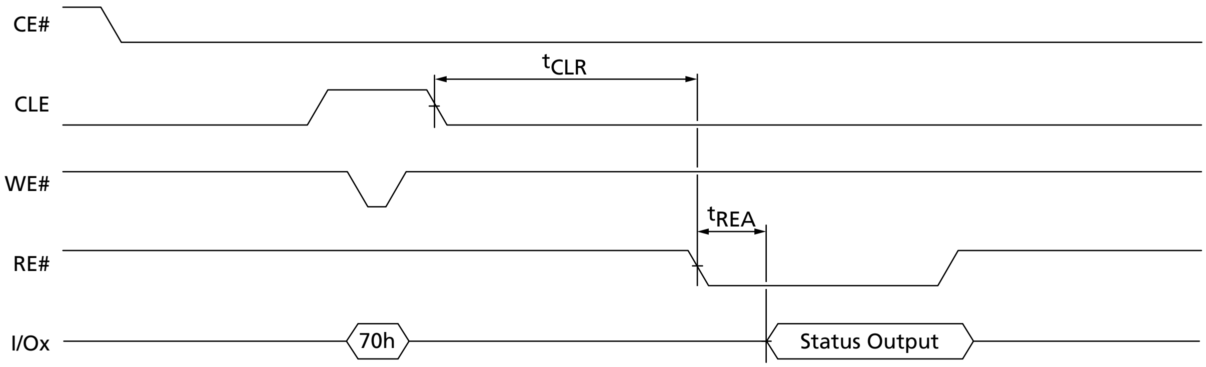
While monitoring the read status to determine when the ^{t}R (transfer from NAND Flash array to data register) is complete, the user must re-issue the READ (00h) command to make the change from status mode to read mode. After the READ command has been re-issued, pulsing the RE# line will result in outputting data, starting from the initial column address.

Table 11: Status Register Bit Definition

SR Bit	Page Program	Program Page Cache Mode	Page Read	Page Read Cache Mode	Block Erase	Definition
0	Pass/fail	Pass/fail (N)	–	–	Pass/fail	“0” = Successful PROGRAM/ERASE “1” = Error in PROGRAM/ERASE
1	–	Pass/fail (N-1)	–	–	–	“0” = Successful PROGRAM/ERASE “1” = Error in PROGRAM/ERASE
2	–	–	–	–	–	“0”
3	–	–	–	–	–	“0”
4	–	–	–	–	–	“0”
5	Ready/busy	Ready/busy[1]	Ready/busy	Ready/busy[1]	Ready/busy	“0” = Busy “1” = Ready
6	Ready/busy	Ready/busy cache[2]	Ready/busy	Ready/busy cache[2]	Ready/busy	“0” = Busy “1” = Ready
7	Write protect	Write protect	Write protect	Write protect	Write protect	“0” = Protected “1” = Not protected
[15:8]	–	–	–	–	–	“0”

Notes: 1. Status register bit 5 is “0” during the actual programming operation. If cache mode is used, this bit will be “1” when all internal operations are complete.
2. Status register bit 6 is “1” when the cache is ready to accept new data. R/B# follows bit 6. See Figure 19 on page 25, and Figure 24 on page 30.

Figure 21: Status Register Operation



PROGRAM Operations

PROGRAM PAGE 80h-10h

Micron NAND Flash devices are inherently page-programmed devices. Pages must be programmed consecutively within a block, from the least significant page address to the most significant page address (i.e., 0, 1, 2, …, 63). Random page address programming is prohibited.

Micron NAND flash devices also support partial-page programming operations. This means that any single bit can only be programmed one time before an erase is required; however, the page can be partitioned such that a maximum of eight programming operations are allowed before an erase is required.

SERIAL DATA INPUT 80h

PROGRAM PAGE operations require loading the SERIAL DATA INPUT (80h) command into the command register, followed by five ADDRESS cycles, then the data. Serial data is loaded on consecutive WE# cycles starting at the given address. The PROGRAM (10h) command is written after the data input is complete. The control logic automatically executes the proper algorithm and controls all the necessary timing to program and verify the operation. Write verification only detects "1s" that are not successfully written to "0s."

R/B# goes LOW for the duration of array programming time, ^{t}PROG. The READ STATUS (70h) command and the RESET (FFh) command are the only commands valid during the programming operation. Bit 6 of the status register will reflect the state of R/B#. When the device reaches ready, read bit 0 of the status register to determine if the program operation passed or failed (see Figure 22). The command register stays in read status register mode until another valid command is written to it.

RANDOM DATA INPUT 85h

After the initial data set is input, additional data can be written to a new column address with the RANDOM DATA INPUT (85h) command. The RANDOM DATA INPUT command can be used any number of times in the same page prior to issuing the PAGE WRITE (10h) command. See Figure 23 for the proper command sequence.

Figure 22: PROGRAM and READ STATUS Operation

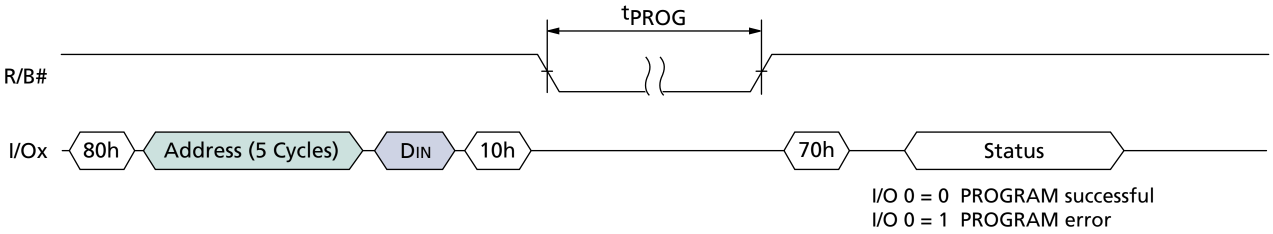
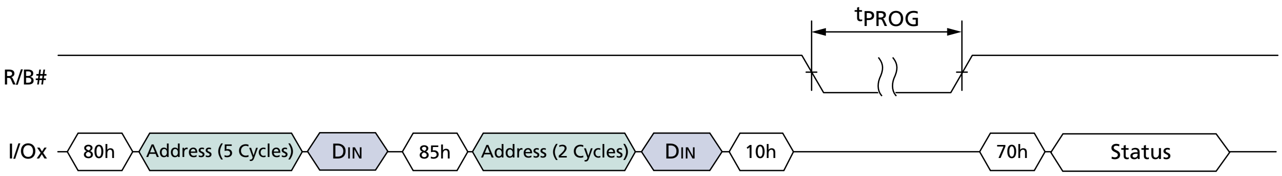


Figure 23: RANDOM DATA INPUT



PROGRAM PAGE CACHE MODE 80h-15h

Cache programming is actually a buffered programming mode of the standard PROGRAM PAGE command. Programming is started by loading the SERIAL DATA INPUT (80h) command to the command register, followed by five address cycles, and a full or partial page of data. The data is initially copied into the cache register, and the CACHE WRITE (15h) command is then latched to the command register. Data is transferred from the cache register to the data register on the rising edge of WE#. R/B# goes LOW during this transfer time. After the data has been copied into the data register and R/B# returns to HIGH, memory array programming begins.

When R/B# returns to HIGH, new data can be written to the cache register by issuing another CACHE PROGRAM command sequence. The time that R/B# stays LOW will be controlled by the actual programming time. The first time through equals the time it takes to transfer the cache register contents to the data register. On the second and subsequent programming passes, transfer from the cache register to the data register is held off until current data register content has been programmed into the array.

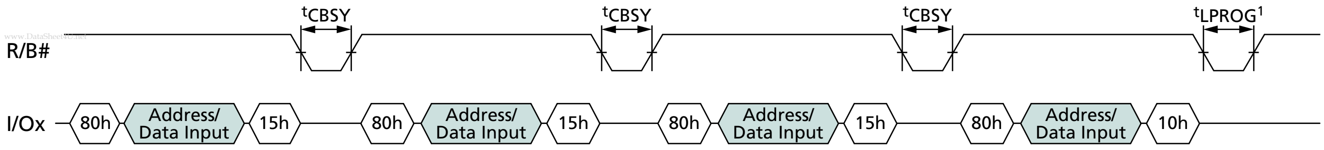
Bit 6 (cache R/B#) of the status register can be read by issuing the READ STATUS (70h) command to determine when the cache register is ready to accept new data. The R/B# pin always follows bit 6.

Bit 5 (R/B#) of the status register can be polled to determine when the actual programming of the array is complete for the current programming cycle.

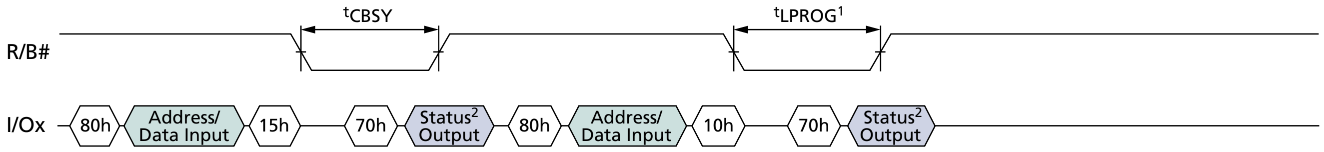
If just the R/B# pin is used to determine programming completion, the last page of the program sequence must use the PROGRAM PAGE (10h) command instead of the CACHE PROGRAM (15h) command. If the CACHE PROGRAM (15h) command is used every time, including the last page of the programming sequence, status register bit 5 must be used to determine when programming is complete (see Figure 24).

Bit 0 of the status register returns the pass/fail for the previous page when bit 6 of the status register is a “1” (ready state). The pass/fail status of the current PROGRAM operation is returned with bit 0 of the status register when bit 5 of the status register is a “1” (ready state) (see Figure 24).

Figure 24: PROGRAM PAGE CACHE MODE Example



A: Without status reads



B: With status reads

Notes: 1. See Note 3, Table 22 on page 45.
2. Check I/O[6:5] for internal ready/busy. Check I/O[1:0] for pass fail. RE# can stay LOW or pulse multiple times after a 70h command.

Internal Data Move

An internal data move requires two command sequences. Issue a READ for INTERNAL DATA MOVE (00h-35h) command first, then the PROGRAM for INTERNAL DATA MOVE (85h-10h) command. Data moves are only supported within the die from which data is read.

READ FOR INTERNAL DATA MOVE 00h-35h

The READ for INTERNAL DATA MOVE (00h-35h)command is used in conjunction with the PROGRAM for INTERNAL DATA MOVE (85h-10h) command. First (00h) is written to the command register, then the internal source address is written (five cycles). After the address is input, the READ for INTERNAL DATA MOVE (35h) command writes to the command register. This transfers a page from memory into the cache register.

The written column addresses are ignored even though all five ADDRESS cycles are required.

The memory device is now ready to accept the PROGRAM for INTERNAL DATA MOVE command. Refer to the command description in the following section for details.

PROGRAM for INTERNAL DATA MOVE 85h-10h

After the READ for INTERNAL DATA MOVE (00h-35h) command has been issued and R/B# goes HIGH, the PROGRAM for INTERNAL DATA MOVE (85h-10h) command can be written to the command register. This command transfers the data from the cache register to the data register and programming of the new destination page begins. The sequence: 85h, destination address (five cycles), then 10h, is written to the device. After 10h is written, R/B# goes LOW while the control logic automatically programs the new page. The READ STATUS command can be used instead of the R/B# line to determine when the write is complete. When status register bit 6 = “1,” bit 0 indicates if the operation was successful.

The RANDOM DATA INPUT (85h) command can be used during the PROGRAM for INTERNAL DATA MOVE command sequence to modify a word or multiple words of the original data. First, data is copied into the cache register using the 00h-35h command sequence, then the RANDOM DATA INPUT (85h) command is written along with the address of the data to be modified next. New data is input on the external data pins. This copies the new data into the cache register.

When 10h is written to the command register, the original data plus the modified data are transferred to the data register, and programming of the new page is started. The RANDOM DATA INPUT command can be issued as many times as necessary before starting the programming sequence with 10h (see Figures 25 and 26 on page 32).

Because INTERNAL DATA MOVE operations do not use external memory, ECC cannot be used to check for errors before programming the data to a new page. This can lead to a data error if the source page contains a bit error due to charge loss or charge gain. In the case that multiple INTERNAL DATA MOVE operations are performed, these bit errors may accumulate without correction. For this reason, it is highly recommended that systems using INTERNAL DATA MOVE operations also use a robust ECC scheme that can correct two or more bits per sector.

Figure 25: INTERNAL DATA MOVE

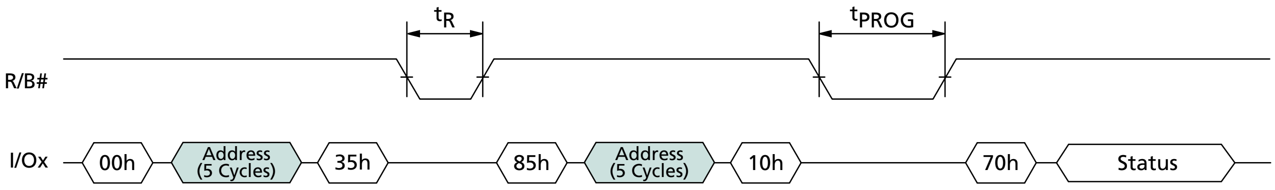
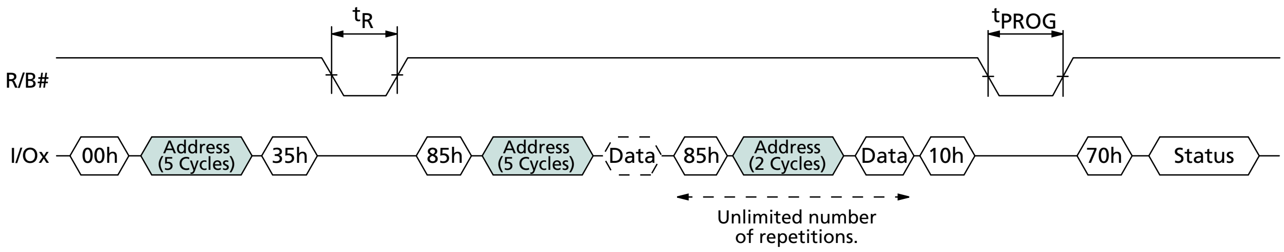


Figure 26: INTERNAL DATA MOVE with RANDOM DATA INPUT



BLOCK ERASE Operation

BLOCK ERASE 60h-D0h

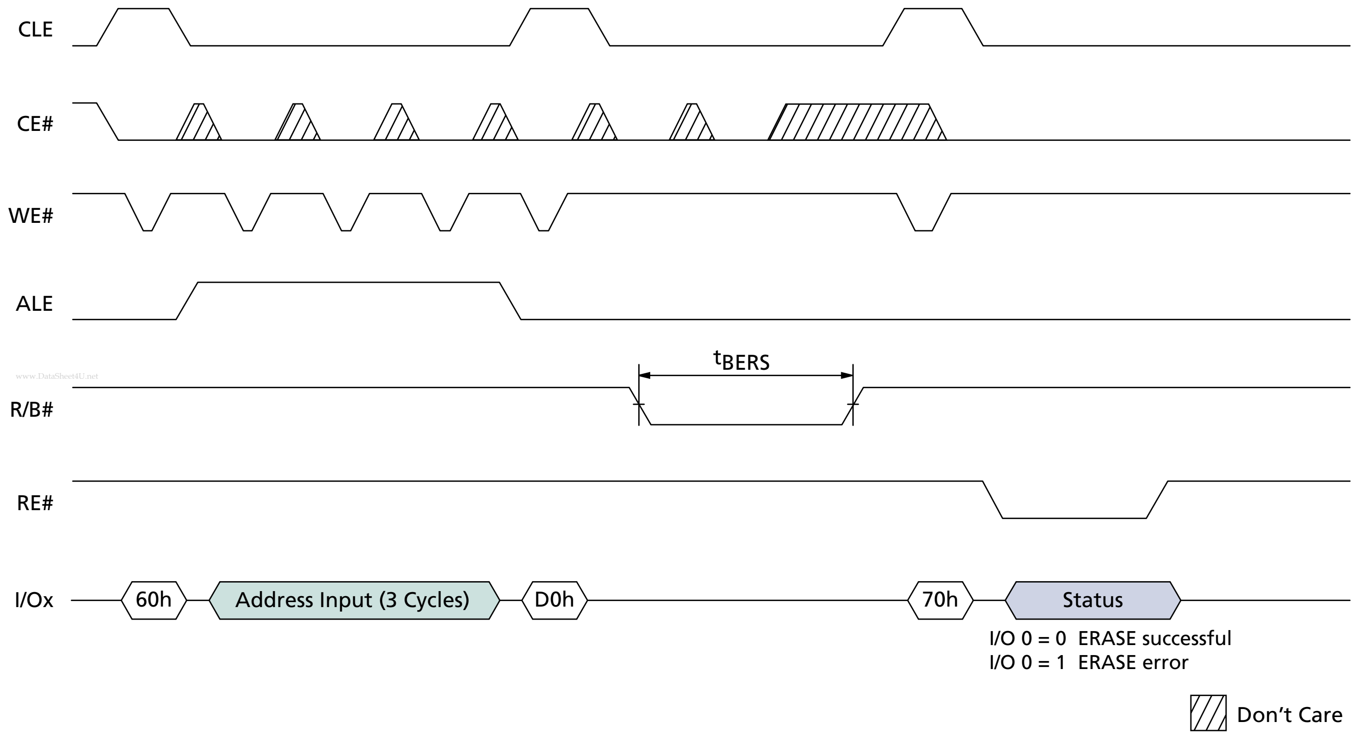
Erasing occurs at the block level. For example, the MT29F2G08xxC device has 2,048 erase blocks organized into 64 pages per block, 2,112 bytes per page (2,048 + 64 bytes). Each block is 132K bytes (128K + 4K bytes). The BLOCK ERASE command operates on one block at a time (see Figure 27).

Three cycles of addresses BA[17:6] and PA[5:0] are required. Although page addresses PA[5:0] are loaded, they are “Don’t Care” and are ignored for BLOCK ERASE operations. See Table 4 on page 13 for addressing details.

The actual command sequence is a two-step process. The ERASE SETUP (60h) command is first written to the command register. Then three cycles of addresses are written to the device. Next, the ERASE CONFIRM (D0h) command is written to the command register. At the rising edge of WE#, R/B# goes LOW and the control logic automatically controls the timing and erase-verify operations. R/B# stays LOW for the entire ^{t}BERS erase time.

The READ STATUS (70h) command can be used to check the status of the BLOCK ERASE operation. When bit 6 = “1” the ERASE operation is complete. Bit 0 indicates a pass/fail condition where “0” = pass (see Figure 27, and Table 11 on page 28).

Figure 27: BLOCK ERASE Operation



One Time Programmable (OTP) Area

This Micron NAND Flash device offers a protected, one-time programmable NAND Flash memory area. Ten full pages (2,112 bytes or 1,056 words per page) of OTP data is available on the device, and the entire range is guaranteed to be good from the factory. The OTP area is accessible only through the OTP commands. Customers can use the OTP area any way they desire; typical uses include programming serial numbers or other data for permanent storage.

In Micron NAND Flash devices, the OTP area leaves the factory in a non-written state (all bits are “1s”). Programming or partial-page programming enables the user to program only “0” bits in the OTP area. The OTP area cannot be erased, even if it is not protected. Protecting the OTP area simply prevents further programming of the OTP area.

While the OTP area is referred to as “one-time programmable,” Micron provides a unique way to program and verify data—before permanently protecting it and preventing future changes.

OTP programming and protection are accomplished in two discrete operations. First, using the OTP DATA PROGRAM (A0h-10h) command, an OTP page is programmed entirely in one operation, or in up to four partial-page programming sequences. Second, the OTP area is permanently protected from further programming using the OTP DATA PROTECT (A5h-10h) command. The pages within the OTP area can always be read using the OTP DATA READ (AFh-30h) command, whether or not it is protected.

OTP DATA PROGRAM A0h-10h

The OTP DATA PROGRAM (A0h-10h) command is used to write data to the pages within the OTP area. An entire page can be programmed at one time, or the page can be partially programmed up to four times. There is no ERASE operation for the OTP pages.

The OTP DATA PROGRAM enables programming into an offset of an OTP page, using the two bytes of column address (CA[11:0]). The command is not compatible with the RANDOM DATA INPUT (85h) command. The OTP DATA PROGRAM command will not execute if the OTP area has been protected.

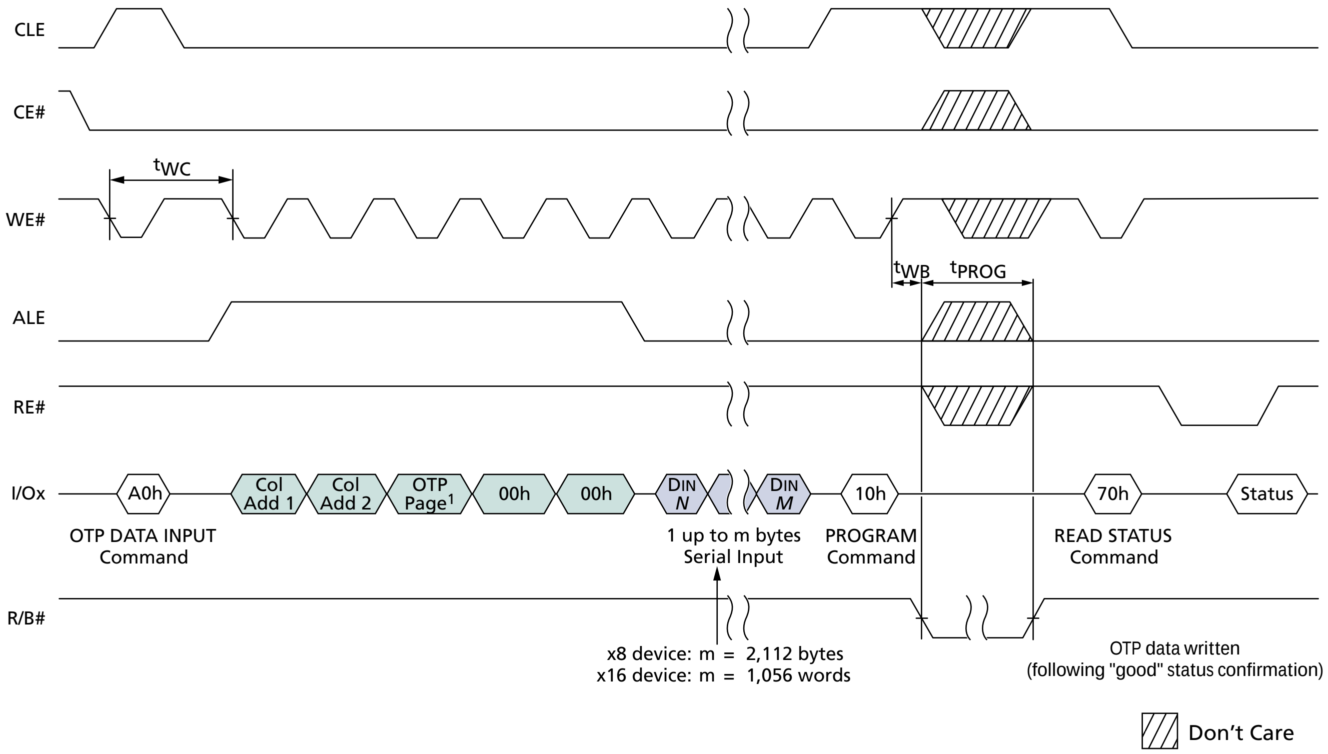
To use the OTP DATA PROGRAM command, issue the A0h command. Then issue five ADDRESS cycles: the first two ADDRESS cycles are the column address, and for the remaining three cycles, select a page in the range of 02h-00h-00h through 0Bh-00h-00h. Next, write the data: from 1 to 2,112 bytes (x8 device), or from 1 to 1,056 words (x16 device). After data input is complete, issue the 10h command. The internal control logic automatically executes the proper programming algorithm and controls the necessary timing for programming and verification. Program verification only detects “1s” that are not successfully written to “0s.”

R/B# goes LOW during the duration of the array programming time (^{t}PROG). The READ STATUS (70h) command is the only command valid during the OTP DATA PROGRAM operation. Bit 5 of the status register will reflect the state of R/B#. If bit 7 is “0,” the OTP area has been protected; otherwise, it is not protected.

When the device is ready, read bit 0 of the status register to determine if the operation passed or failed (see Table 11 on page 28).

It is possible to program each OTP page a maximum of four times.

Figure 28: OTP DATA PROGRAM



Notes: 1. The OTP page must be within the 02h–0Bh range.

OTP DATA PROTECT A5h-10h

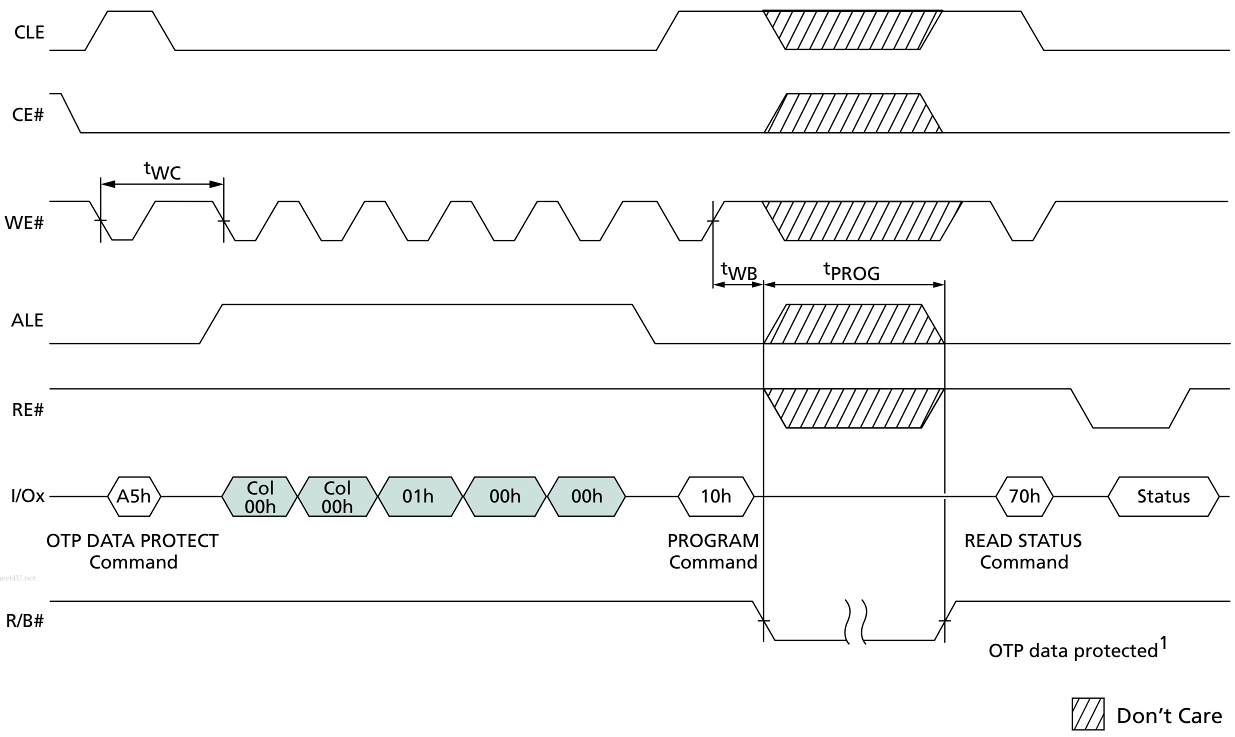
The OTP DATA PROTECT (A5h-10h) command is used to protect the data in the OTP area. After the data is protected it cannot be programmed further. When the OTP area is protected, the pages within the area are no longer programmable and cannot be unprotected.

To use the OTP DATA PROTECT command, issue the A5h command. Next, issue the following five address cycles: 00h-00h-01h-00h-00h. Finally, issue the 10h command.

R/B# goes LOW while the OTP area is being protected. The protect command duration is similar to a normal page programming operation, ^{t}PROG. The READ STATUS (70h) command is the only command valid during the OTP DATA PROTECT operation. Bit 5 of the status register will reflect the state of R/B#.

When the device is ready, read bit 0 of the status register to determine if the operation passed or failed (see Table 11 on page 28).

Figure 29: OTP DATA PROTECT



Notes: 1. OTP data is protected following "good" status confirmation.

OTP DATA READ AFh-30h

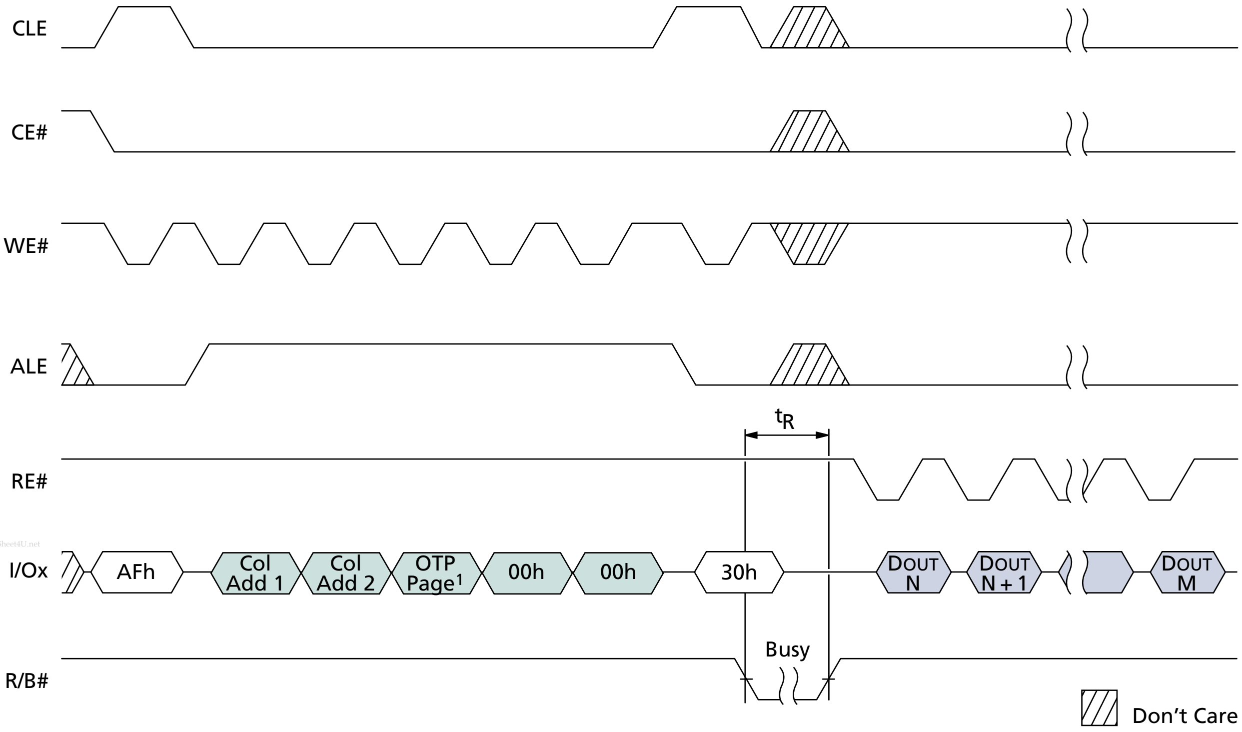
The OTP DATA READ (AFh-30h) command is used to read data from a page within the OTP area. An OTP page within the OTP area is available for reading data whether or not the area is protected.

To use the OTP DATA READ command, issue the AFh command. Then issue five ADDRESS cycles: the first two ADDRESS cycles are the column address, and for the remaining three cycles select a page in the range of 02h-00h-00h through 0Bh-00h-00h. Finally, issue the 30h command.

R/B# goes LOW (^{t}R) while the data is moved from the OTP page to the data register. The READ STATUS (70h) command and the RESET (FFh) command are the only commands valid during the OTP DATA READ operation. Bit 5 of the status register will reflect the state of R/B#. For details, refer to Table 11 on page 28.

Normal READ operation timings apply to OTP read accesses (see Figure 30). Additional pages within the OTP area can be selected by repeating the OTP DATA READ command.

Figure 30: OTP DATA READ



Notes: 1. The OTP page must be within the 02h–0Bh range.

RESET Operation

RESET FFh

The RESET command is used to put the memory device into a known condition and to abort a command sequence in progress.

READ, PROGRAM, and ERASE commands can be aborted while the device is in the busy state. The contents of the memory location being programmed or the block being erased are no longer valid. The data may be partially erased or programmed, and is invalid. The command register is cleared and is ready for the next command. The data register and cache register contents are invalid.

The status register contains the value E0h when WP# is HIGH; otherwise it is written with a 60h value. R/B# goes low for ^{t}RST after the RESET command is written to the command register (see Figure 31 and Table 12).

Figure 31: RESET Operation

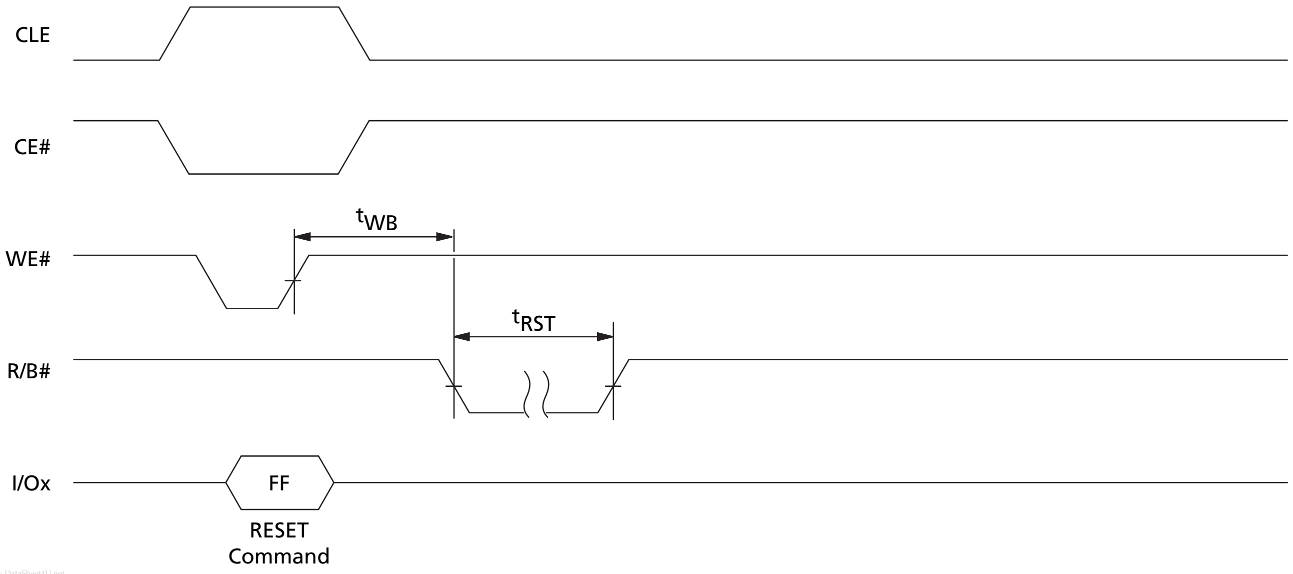


Table 12: Status Register Contents After RESET Operation

Condition	Status	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
WP# HIGH	Ready	1	1	1	0	0	0	0	0	E0h
WP# LOW	Ready and write protected	0	1	1	0	0	0	0	0	60h

WRITE PROTECT Operation

It is possible to enable and disable PROGRAM and ERASE commands using the WP# pin. The following figures illustrate the setup time (^tWW) required from WP# toggling until a PROGRAM or ERASE command is latched into the command register. After command cycle 1 is latched, WP# must not be toggled until the command is complete and the device is ready (status register bit 5 is "1").

Figure 32: ERASE Enable

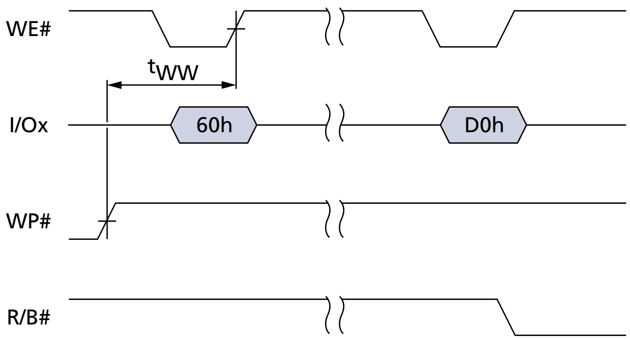


Figure 33: ERASE Disable

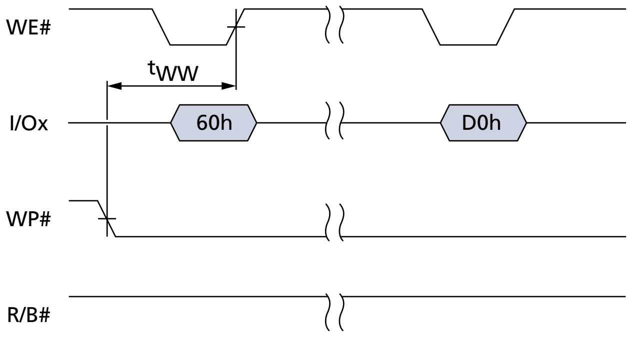


Figure 34: PROGRAM Enable

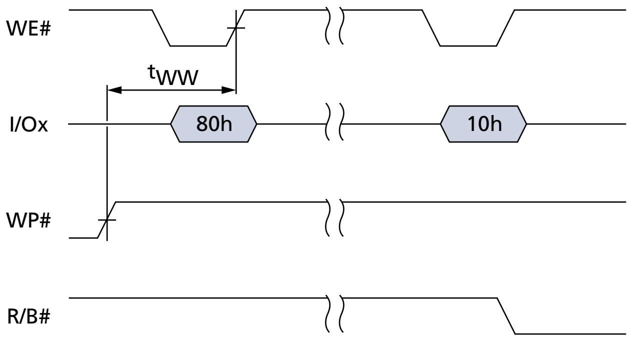
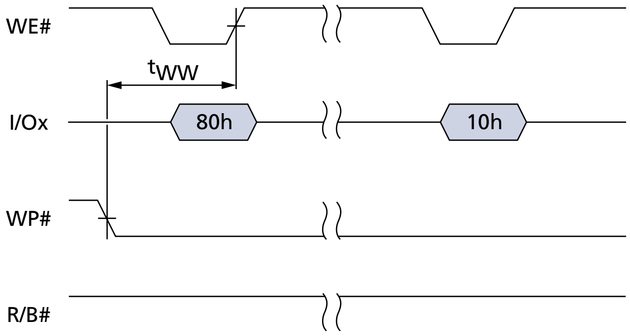


Figure 35: PROGRAM Disable



Error Management

Micron NAND Flash devices are specified to have a minimum of 2,008 (NVB) valid blocks out of every 2,048 total available blocks. This means the devices may have blocks that are invalid when they are shipped. An invalid block is one that contains one or more bad bits. Additional bad blocks may develop with use. However, the total number of available blocks will not fall below NVB during the endurance life of the product.

Although NAND Flash memory devices may contain bad blocks, they can be used quite reliably in systems that provide bad-block mapping, bad-block replacement, and error correction algorithms. This type of software environment ensures data integrity.

Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the Flash device.

The first block (physical block address 00h) for each CE#is guaranteed to be free of defects (up to 1,000 PROGRAM/ERASE cycles) when shipped from the factory. This provides a reliable location for storing boot code and critical boot information.

Before NAND Flash devices are shipped from Micron, they are erased. The factory identifies invalid blocks before shipping by programming data other than FFh (x8) or FFFFh (x16) into the first spare location (column address 2,048 for x8 devices, or column address 1,024 for x16 devices) of the first or second page of each bad block.

System software should check the first spare address on the first two pages of each block prior to performing any erase or programming operations on the NAND Flash device. A bad block table can then be created, allowing system software to map around these areas. Factory testing is performed under worst-case conditions. Because blocks marked "bad" may be marginal, it may not be possible to recover this information if the block is erased.

Over time, some memory locations may fail to program or erase properly. In order to ensure that data is stored properly over the life of the NAND Flash device, certain precautions must be taken, such as:

- Always check status after a PROGRAM, ERASE, or DATA MOVE operation.
- Use some type of error detection and correction algorithm to recover from single-bit errors per 528 bytes of data.
- Use a bad-block replacement algorithm.

Electrical Characteristics

Stresses greater than those listed under “Absolute Maximum Ratings” (see Table 13) may cause permanent damage to the device. This is a stress rating *only,* and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 13: Absolute Maximum Ratings by Device
Voltage on any pin relative to VSS

Parameter/Condition		Symbol	Min	Max	Unit
Voltage input	MT29FxGxxxAC	VIN	–0.6	+4.6	V
	MT29FxGxxxBC		–0.6	+2.4	V
VCC supply voltage	MT29FxGxxxAC	VCC	–0.6	+4.6	V
	MT29FxGxxxBC		–0.6	+2.4	V
Storage temperature		TSTG	–65	+150	°C
Short circuit output current, I/Os			–	5	mA

Table 14: Recommended Operating Conditions

Parameter/Condition		Symbol	Min	Typ	Max	Unit
Operating temperature	Commercial	TA	0	–	+70	°C
	Extended		–40	–	+85	°C
VCC supply voltage	MT29FxGxxxAC	Vcc	2.7	3.3	3.6	V
	MT29FxGxxxBC		1.70	1.8	1.95	V
Ground supply voltage		Vss	0	0	0	V

Vcc Power Cycling

Micron NAND Flash devices are designed to prevent data corruption during power transitions. VCC is internally monitored. When VCC goes below approximately 1.1V (1.8V device), or 2.0V (3V device), PROGRAM and ERASE functions are disabled. WP# provides additional hardware protection. WP# should be kept at VIL during power cycling. When VCC reaches approximately 1.5V (1.8V device) or 2.5V (3V device), a minimum of 10µs should be allowed for the NAND Flash to initialize before executing any commands (see Figure 36).

Figure 36: AC Waveforms During Power Transitions

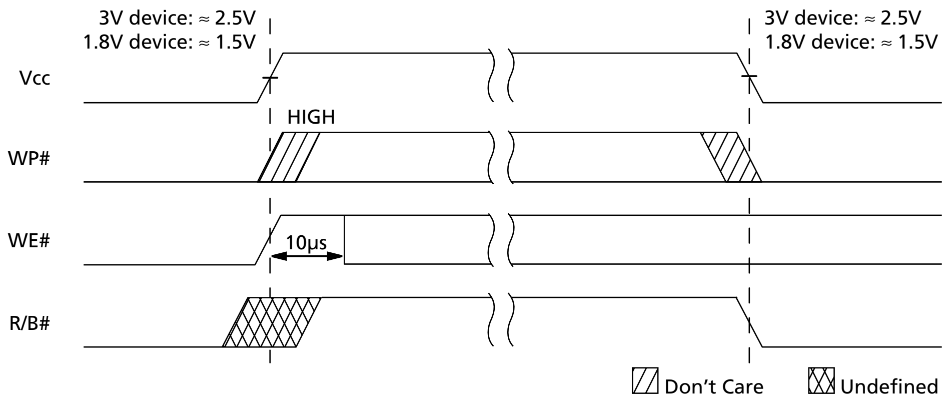


Table 15: M29FxGxxxAC 3V Device DC and Operating Characteristics

Parameter		Conditions	Symbol	Min	Typ	Max	Unit
Sequential read current		$^tRC = 30ns$, CE# = V_{IL}, $I_{OUT} = 0mA$	$I_{CC}1$	–	15	30	mA
Program current		–	$I_{CC}2$	–	15	30	mA
Erase current		–	$I_{CC}3$	–	15	30	mA
Standby current (TTL)		CE# = V_{IH}, PRE = WP# = 0V/V_{CC}	$I_{SB}1$	–	–	1	mA
Standby current (CMOS)							
	MT29F2GxxAAC	CE# = V_{CC} – 0.2V, PRE = WP# = 0V/V_{CC}	$I_{SB}2$	–	10	50	µA
	MT29F4GxxBAC			–	20	100	µA
	MT29F8GxxFAC			–	40	200	µA
Input leakage current							
	MT29F2GxxAAC	V_{IN} = 0V to V_{CC}	I_{LI}	–	–	±10	µA
	MT29F4GxxBAC			–	–	±20	µA
	MT29F8GxxFAC			–	–	±40	µA
Input leakage current (PRE)		V_{IN} = 0V/V_{CC}	I_{LIPRE}	–	–	±10	µA
Output leakage current							
	MT29F2GxxAAC	V_{OUT} = 0V to V_{CC}	I_{LO}	–	–	±10	µA
	MT29F4GxxBAC			–	–	±20	µA
	MT29F8GxxFAC			–	–	±40	µA
Input high voltage		I/O[7:0], I/O[15:0] CE#, CLE, ALE, WE#, RE#, WP#, PRE, R/B#	V_{IH}	0.8 x V_{CC}	–	V_{CC} + 0.3	V
Input low voltage (all inputs)		–	V_{IL}	–0.3	–	0.2 x V_{CC}	V
Output high voltage		I_{OH} = –400µA	V_{OH}	2.4	–	–	V
Output low voltage		I_{OL} = 2.1mA	V_{OL}	–	–	0.4	V
Output low current (R/B#)		V_{OL} = 0.4V	I_{OL} (R/B#)	8	10	–	mA

Note: The PRE function is available only on commercial-temperature devices.

Table 16: M29FxGxxxBC 1.8V Device DC and Operating Characteristics

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Sequential read current	^tRC = 50ns, CE# = V_{IL}, I_{OUT} = 0mA	$I_{CC}1$	–	8	15	mA
Program current	–	$I_{CC}2$	–	8	15	mA
Erase current	–	$I_{CC}3$	–	8	15	mA
Standby current (TTL)	CE# = V_{IH}, PRE = WP# = 0V/V_{CC}	$I_{SB}1$	–	–	1	mA
Standby current (CMOS)						
MT29F2GxxAAC	CE# = V_{CC} – 0.2V, PRE = WP# = 0V/V_{CC}	$I_{SB}2$	–	10	50	µA
MT29F4GxxBAC			–	20	100	µA
MT29F8GxxFAC			–	40	200	µA
Input leakage current						
MT29F2GxxAAC	V_{IN} = 0V to V_{CC}	I_{LI}	–	–	±10	µA
MT29F4GxxBAC			–	–	±20	µA
MT29F8GxxFAC			–	–	±40	µA
Output leakage current						
MT29F2GxxAAC	V_{OUT} = 0V to V_{CC}	I_{LO}	–	–	±10	µA
MT29F4GxxBAC			–	–	±20	µA
MT29F8GxxFAC			–	–	±40	µA
Input high voltage	I/O [7:0], I/O [15:0] CE#, CLE, ALE, WE#, RE#, WP#, PRE, R/B#	V_{IH}	0.8 x V_{CC}	–	V_{CC} + 0.3	V
Input low voltage (all inputs)	–	V_{IL}	–0.3	–	0.2 x V_{CC}	V
Output high voltage	I_{OH} = –100µA	V_{OH}	V_{CC} – 0.1	–	–	V
Output low voltage	I_{OL} = 100µA	V_{OL}	–	–	0.1	V
Output low current	V_{OL} = 0.1V	I_{OL} (R/B#)	3	4	–	mA

Note: The PRE function is not available on 1.8V devices.

Table 17: Valid Blocks

Parameter	Symbol	Device	Min	Max	Unit	Notes
Valid block number	N_{VB}	MT29F2GxxAxC	2,008	2,048	Blocks	1, 2
		MT29F4GxxBxC	4,016	4,096		
		MT29F8GxxFxC	8,032	8,192		3

Notes:
1. Invalid blocks are blocks that contain one or more bad bits. The device may contain bad blocks upon shipment. Additional bad blocks may develop over time; however, the total number of available blocks will not drop below N_{VB} during the endurance life of the device. Do not erase or program blocks marked invalid by the factory.
2. Block 00h (the first block) is guaranteed to be valid and does not require error correction up to 1K PROGRAM/ERASE cycles.
3. The number of invalid blocks in each 4Gb section will not exceed 80.

Table 18: Capacitance

Description	Symbol	Device	Max	Unit	Notes
Input capacitance	CIN	MT29F2GxxAxC	10	pF	1, 2
		MT29F4GxxBxC	20		
		MT29F8GxxFxC	40		
Input/output capacitance (I/O)	CIO	MT29F2GxxAxC	10	pF	1, 2
		MT29F4GxxBxC	20		
		MT29F8GxxFxC	40		

Notes: 1. These parameters are verified in device characterization and are not 100 percent tested.
2. Test conditions: T_C = 25°C; f = 1 MHz; VIN = 0V.

Table 19: Test Conditions

Parameter		Value	Notes
Input pulse levels	MT29FxGxxxAC	0.0V to VCC (2.7V–3.6V)	
	MT29FxGxxxBC	0.0V to VCC (1.70V–1.95V)	
Input rise and fall times		5ns	
Input and output timing levels		VCC/2	
Output load	MT29FxGxxxAC (VCC = 3.0V ± 10%)	1 TTL GATE and CL = 50pF	1
	MT29FxGxxxAC (VCC = 3.3V ± 10%)	1 TTL GATE and CL = 100pF	1
	MT29FxGxxxBC (VCC = 1.70–1.95V)	1 TTL GATE and CL = 30pF	1

Notes: 1. Verified in device characterization; not 100 percent tested.

Table 20: AC Characteristics: Command, Data, and Address Input

		3V x16 and 1.8V		3V x8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
ALE to data start	^{t}ADL	100	–	100	–	ns	1
ALE hold time	^{t}ALH	10	–	5	–	ns	2
ALE setup time	^{t}ALS	25	–	10	–	ns	2
CE# hold time	^{t}CH	10	–	5	–	ns	2
CLE hold time	^{t}CLH	10	–	5	–	ns	2
CLE setup time	^{t}CLS	25	–	10	–	ns	2
CE# setup time	^{t}CS	35	–	15	–	ns	2
Data hold time	^{t}DH	10	–	5	–	ns	2
Data setup time	^{t}DS	20	–	10	–	ns	2
Write cycle time	^{t}WC	45	–	30	–	ns	2, 3
WE# pulse width HIGH	^{t}WH	15	–	10	–	ns	2
WE# pulse width	^{t}WP	25	–	15	–	ns	2
WP# setup time	^{t}WW	30	–	30	–	ns	

Notes: 1. Timing for ^{t}ADL begins in the ADDRESS cycle, on the final rising edge of WE#, and ends with the first rising edge of WE# for data input.
2. For PAGE READ CACHE MODE and PROGRAM PAGE CACHE MODE operations, the 3V x16 AC characteristics apply for 3V x8 devices.
3. For 1.8V devices: During PROGRAM PAGE CACHE MODE and PAGE READ CACHE MODE operations, when VCC = 1.70V, ^{t}WC = 55ns MIN.

Table 21: AC Characteristics: Normal Operation

Parameter	Symbol	3V x16 and 1.8V		3V x8		Unit	Notes
		Min	Max	Min	Max		
ALE to RE# delay	^{t}AR	10	–	10		ns	
CE# access time	^{t}CEA	–	45	–	23	ns	1
CE# HIGH to output High-Z	^{t}CHZ	–	20	–	20	ns	2
CLE to RE# delay	^{t}CLR	10	–	10	–	ns	
Cache busy in page read cache mode (first 31h)	^{t}DCBSYR1	–	3	–	3	µs	
Cache busy in page read cache mode (next 31h and 3Fh)	^{t}DCBSYR2	^{t}DCBSYR1	25	^{t}DCBSYR1	25	µs	
Output High-Z to RE# LOW	^{t}IR	0	–	0	–	ns	1
Data output hold time	^{t}OH	15	–	15	–	ns	
Data transfer from NAND Flash array to data register	^{t}R	–	25	–	25	µs	
READ cycle time	^{t}RC	50	–	30	–	ns	1
RE# access time	^{t}REA	–	30	–	18	ns	1
RE# HIGH hold time	^{t}REH	15	–	10	–	ns	1
RE# HIGH to output High-Z	^{t}RHZ	–	30	–	30	ns	2
RE# pulse width	^{t}RP	25	–	15	–	ns	1
Data transfer from NAND Flash array to data register at power-up with PRE enabled at 3.3V Vcc	^{t}RPRE	–	25	–	25	µs	3
Ready to RE# LOW	^{t}RR	20	–	20	–	ns	
Reset time (READ/PROGRAM/ERASE)	^{t}RST	–	5/10/500	–	5/10/500	µs	4
WE# HIGH to busy	^{t}WB	–	100	–	100	ns	4, 5
WE# HIGH to RE# LOW	^{t}WHR	60	–	60	–	ns	

Notes:
1. For PAGE READ CACHE MODE and PROGRAM PAGE CACHE MODE operations, the 3V x16 AC characteristics apply for 3V x8 devices.
2. Transition is measured ±200mV from steady-state voltage with load. This parameter is sampled and not 100 percent tested.
3. The PRE function is available only on 3V commercial-temperature devices.
4. If RESET (FFh) command is loaded at ready state, the device goes busy for maximum 5µs.
5. Do not issue a new command during ^{t}WB, even if R/B# is ready.

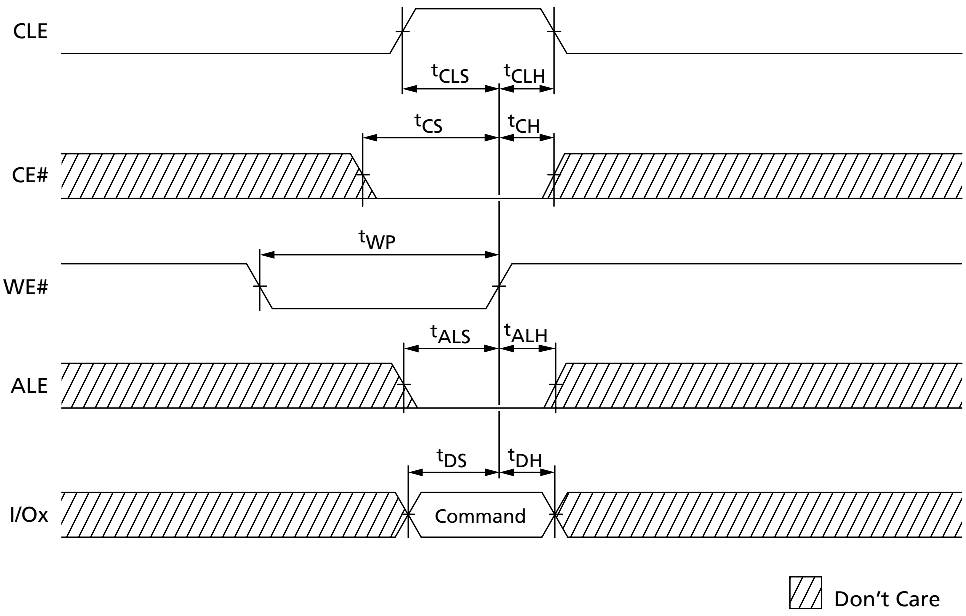
Table 22: PROGRAM/ERASE Characteristics

Parameter	Description	Typ	Max	Unit	Notes
NOP	Number of partial page programs	–	8	Cycles	1
^{t}BERS	Block erase time	2	3	ms	
^{t}CBSY	Busy time for cache program	3	700	µs	2
^{t}LPROG	Last page program time	–	–	–	3
^{t}PROG	Page program time	300	700	µs	

Notes:
1. Eight cycles total to the same page.
2. ^{t}CBSY MAX time depends on timing between internal program completion and data in.
3. ^{t}LPROG = ^{t}PROG (last page) + ^{t}PROG (last – 1 page) – command load time (last page) – address load time (last page) – data load time (last page).

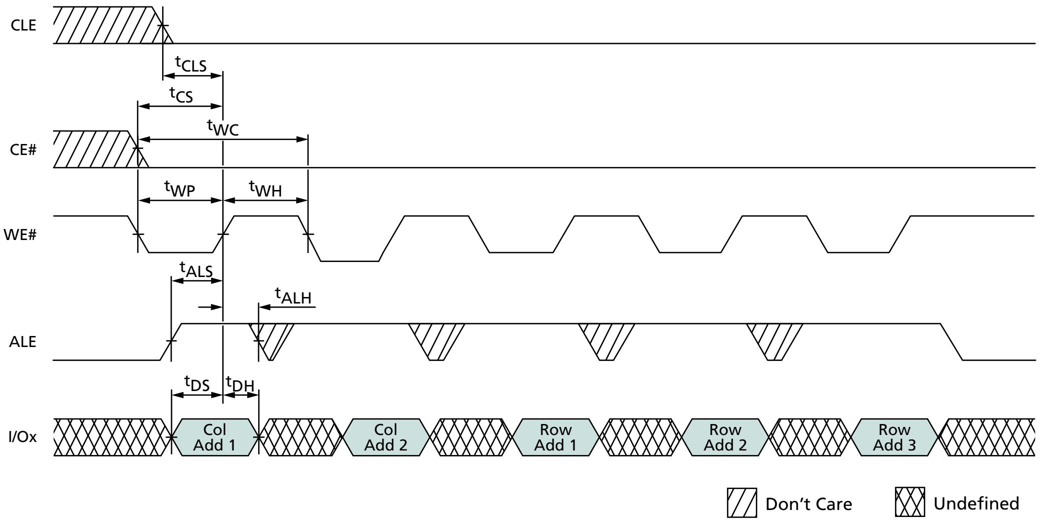
Timing Diagrams

Figure 37: COMMAND LATCH Cycle



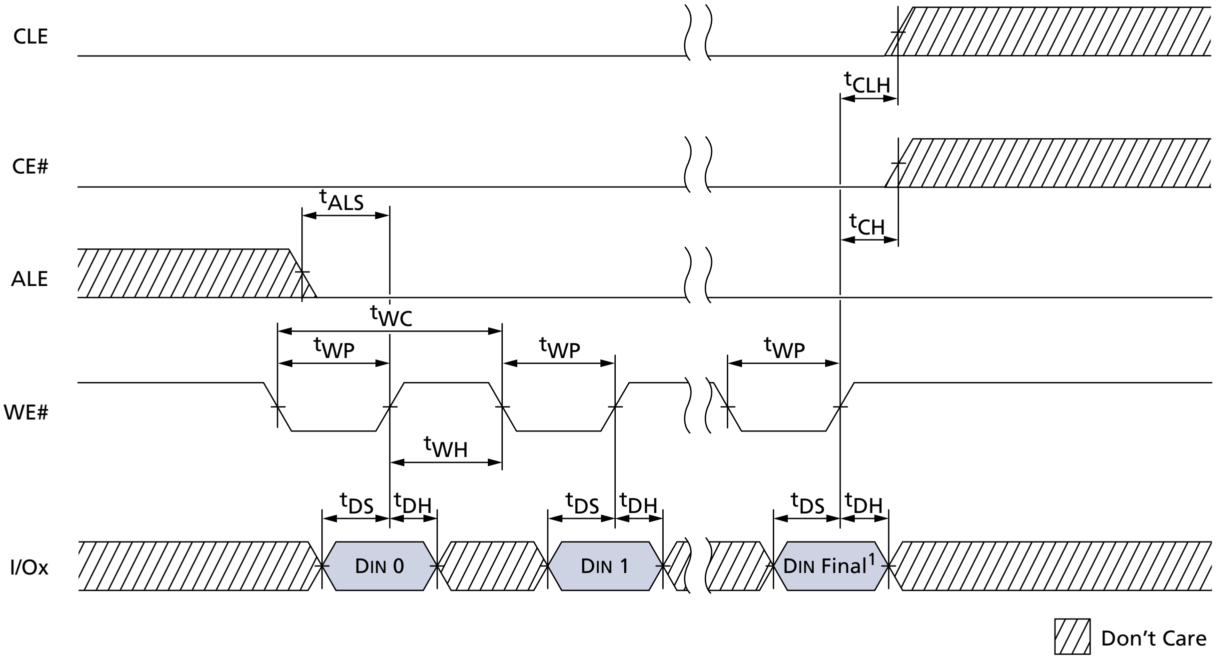
Note: x16: I/O[15:8] must be set to "0."

Figure 38: ADDRESS LATCH Cycle



Note: x16: I/O [15:8] must be set to "0."

Figure 39: INPUT DATA LATCH Cycle



Notes: 1. DIN Final = 2,111 (x8) or 1,055 (x16).

Figure 40: SERIAL ACCESS Cycle After READ

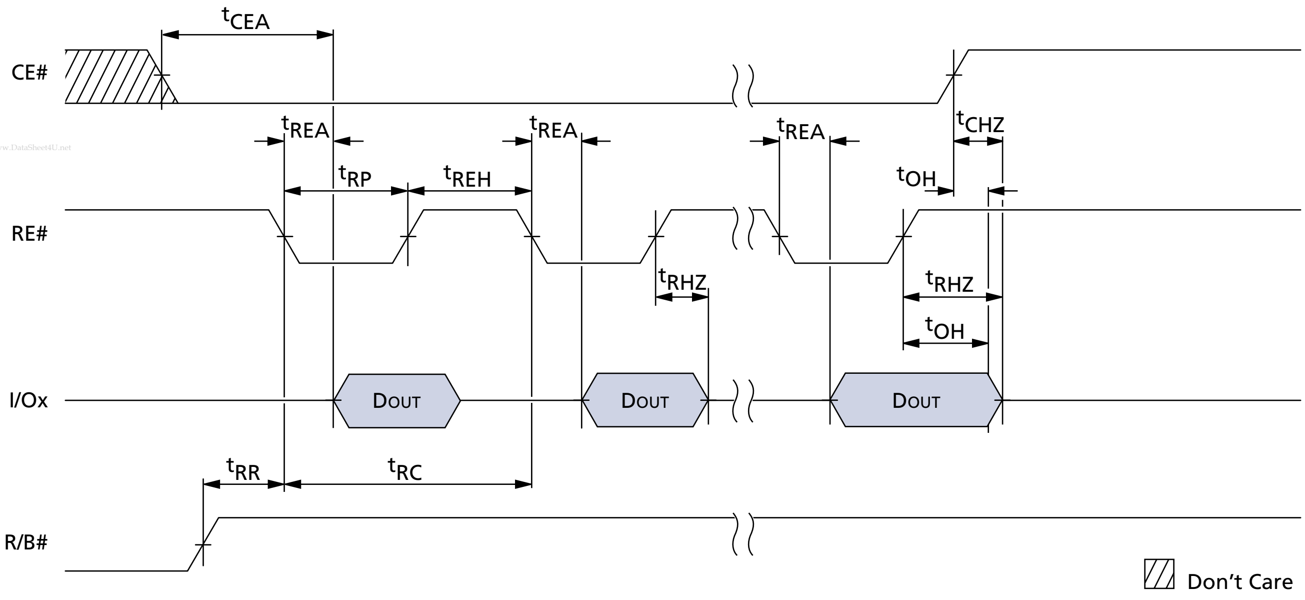


Figure 41: READ STATUS Cycle

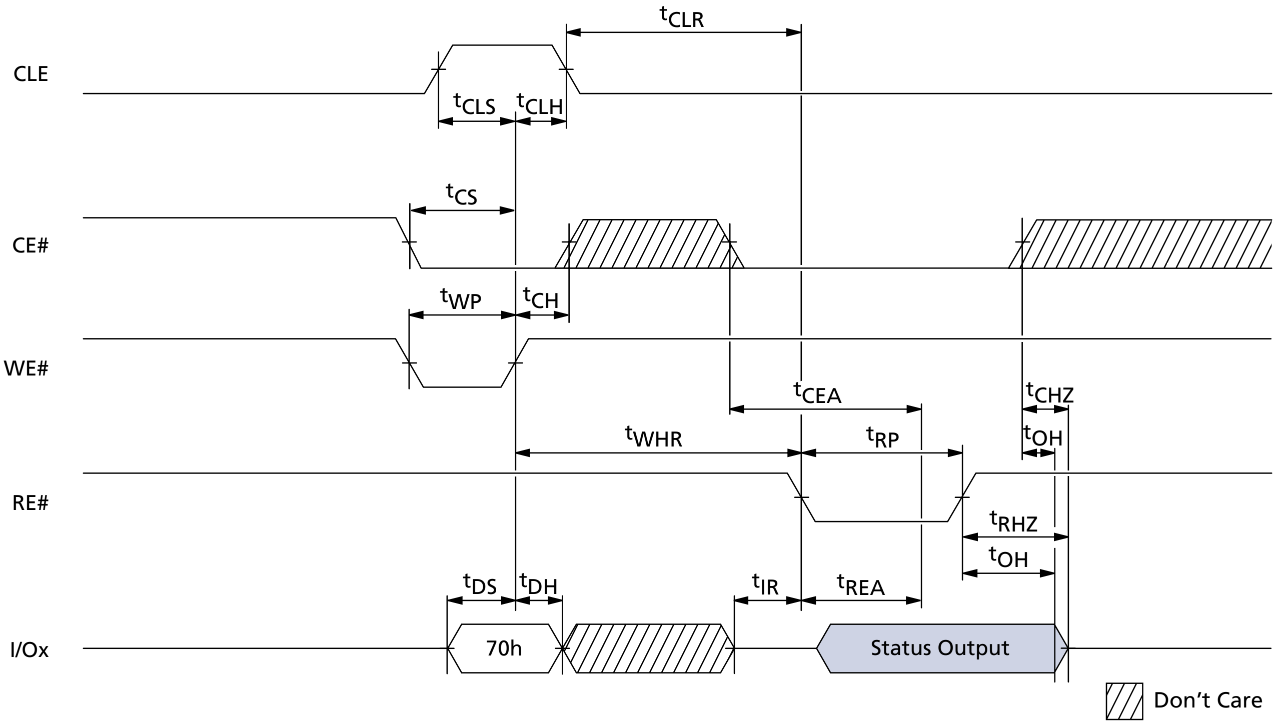


Figure 42: PAGE READ

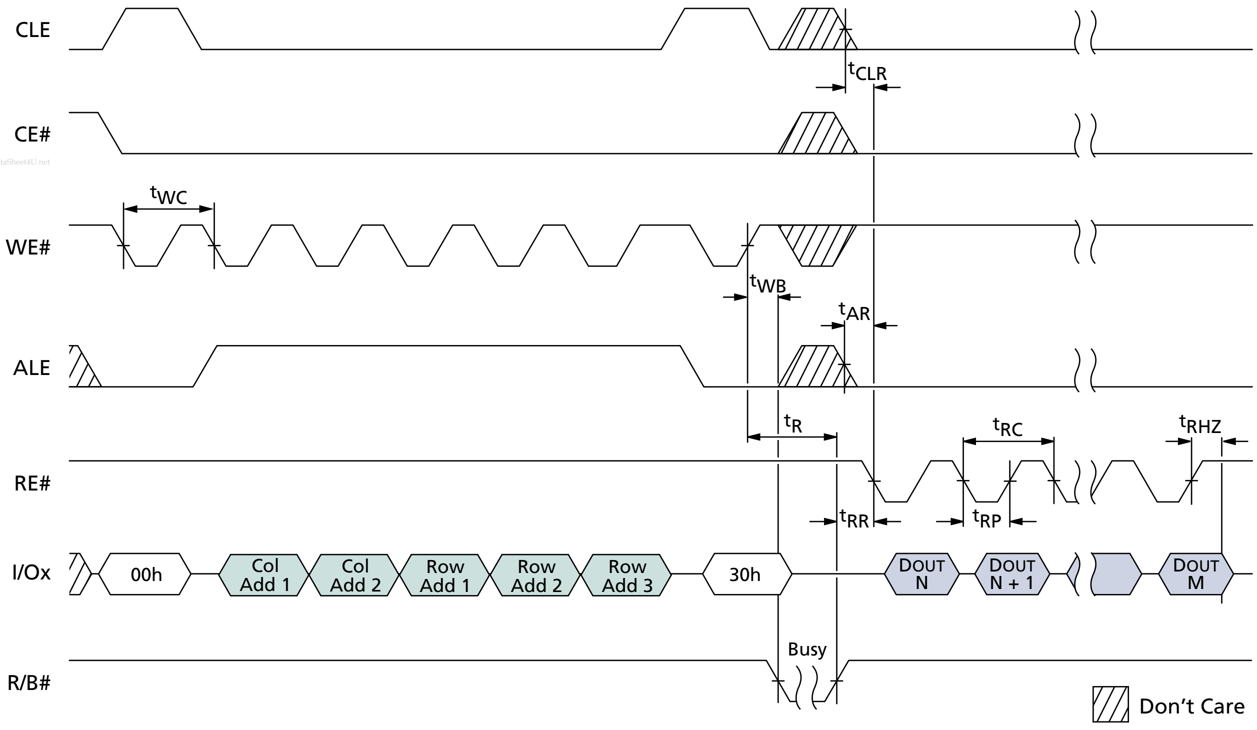


Figure 43: PAGE READ Operation with CE# “Don’t Care”

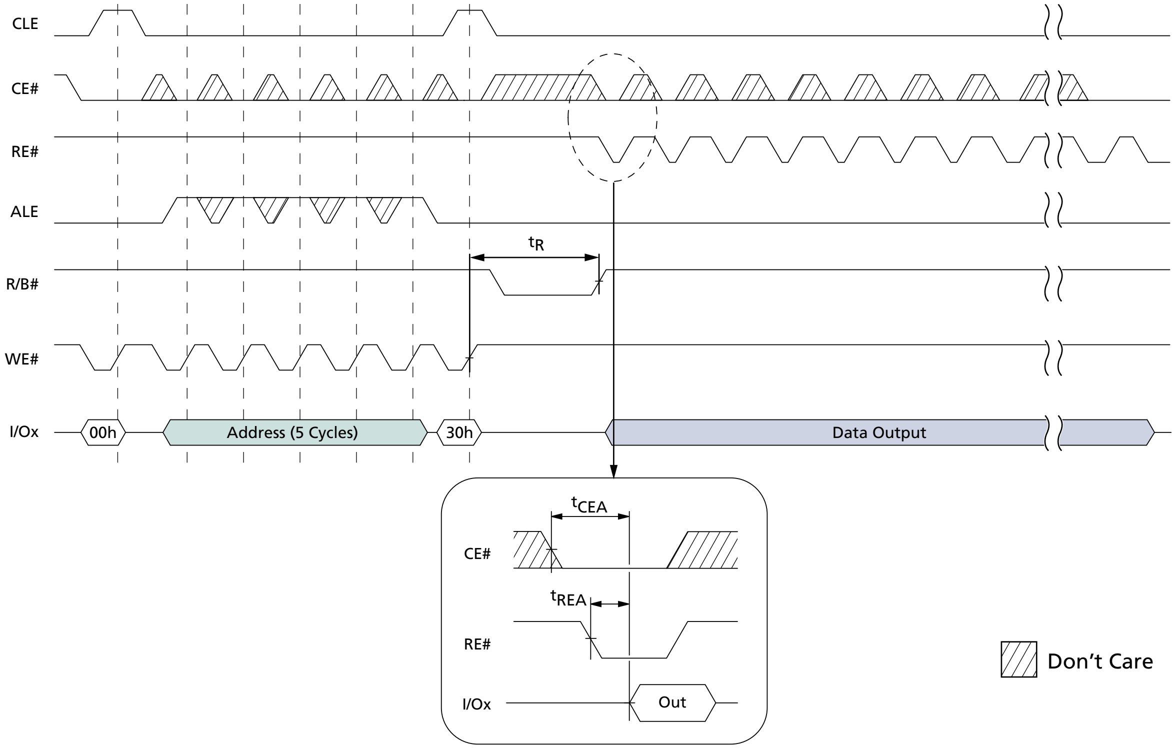


Figure 44: RANDOM DATA READ

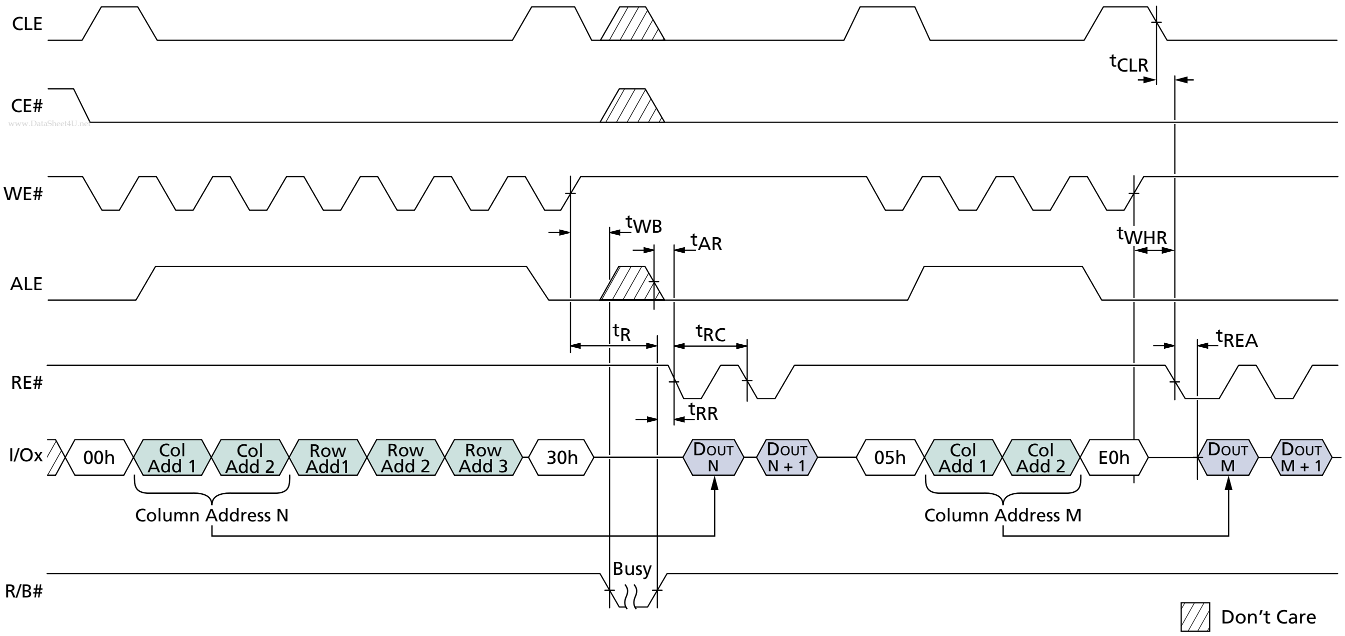


Figure 45: PAGE READ CACHE MODE Timing Diagram, Part 1 of 2

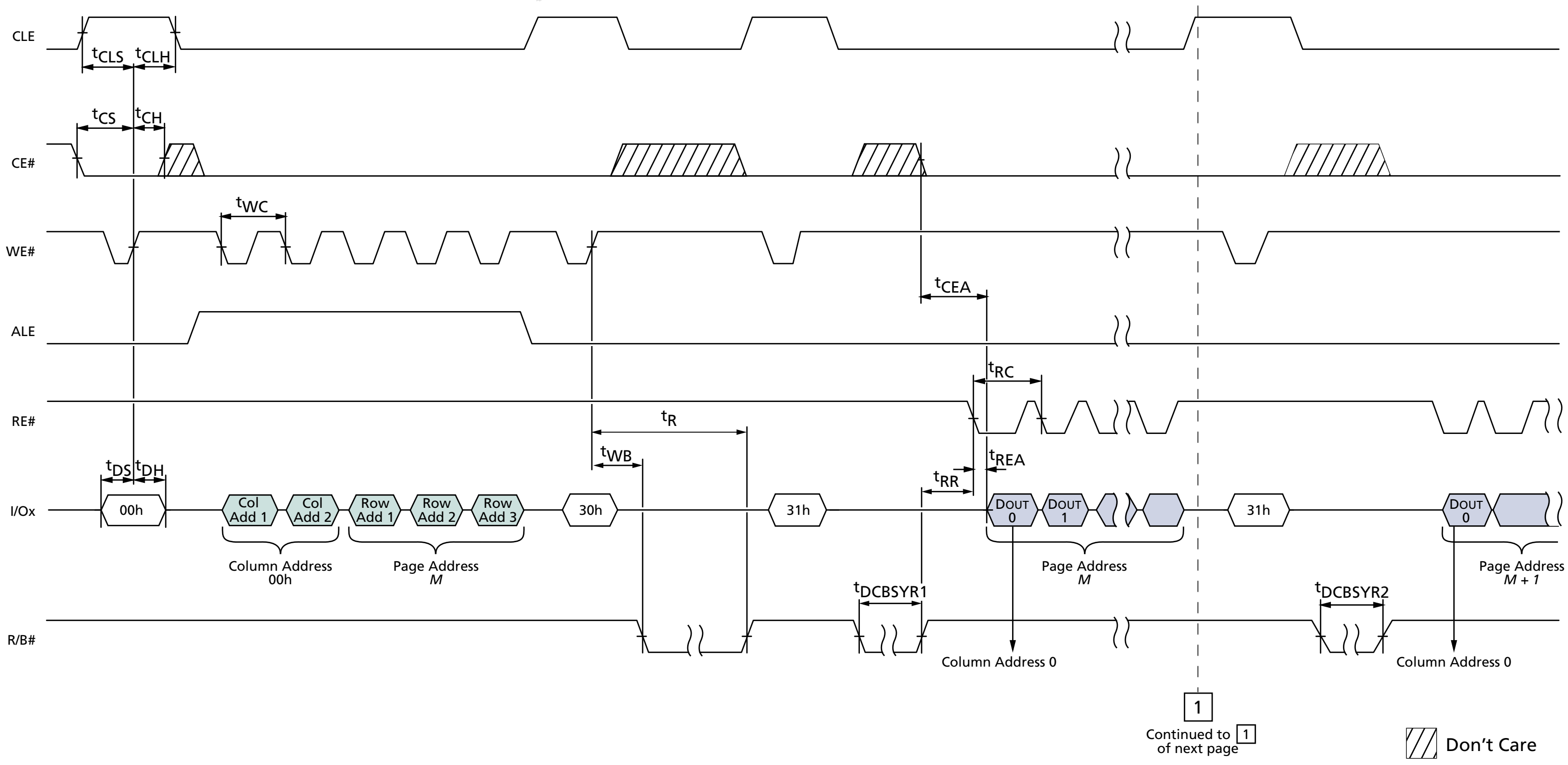


Figure 46: PAGE READ CACHE MODE Timing Diagram, Part 2 of 2

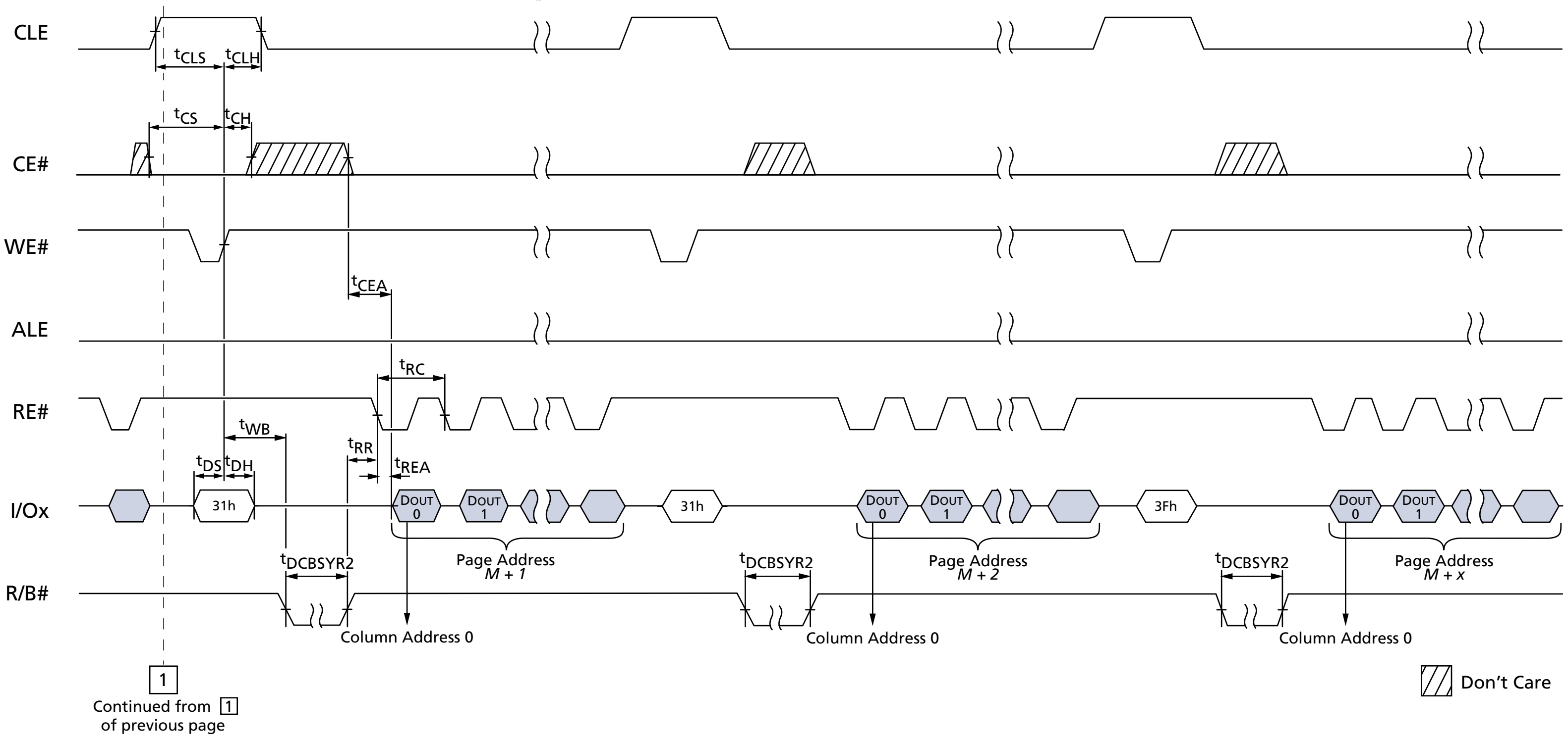


Figure 47: PAGE READ CACHE MODE Timing without R/B#, Part 1 of 2

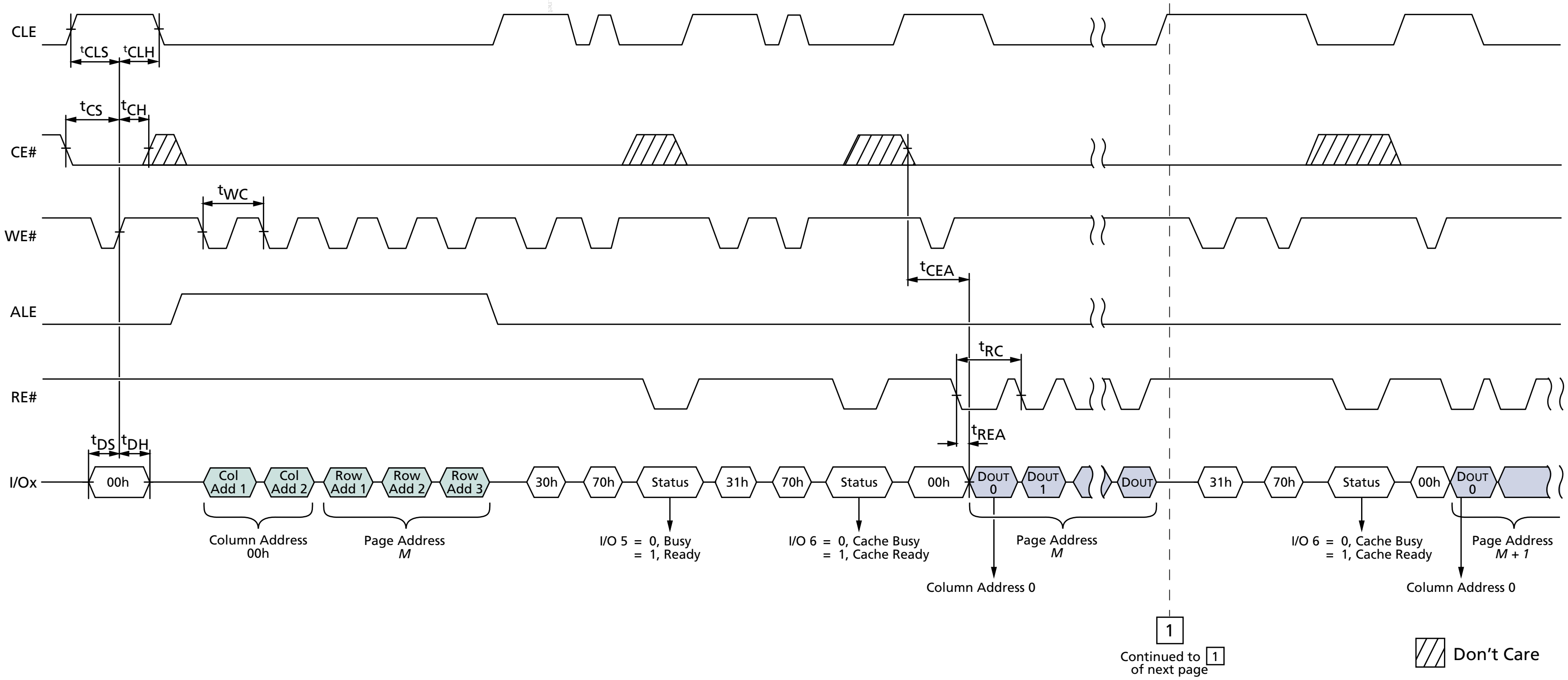


Figure 48: PAGE READ CACHE MODE Timing without R/B#, Part 2 of 2

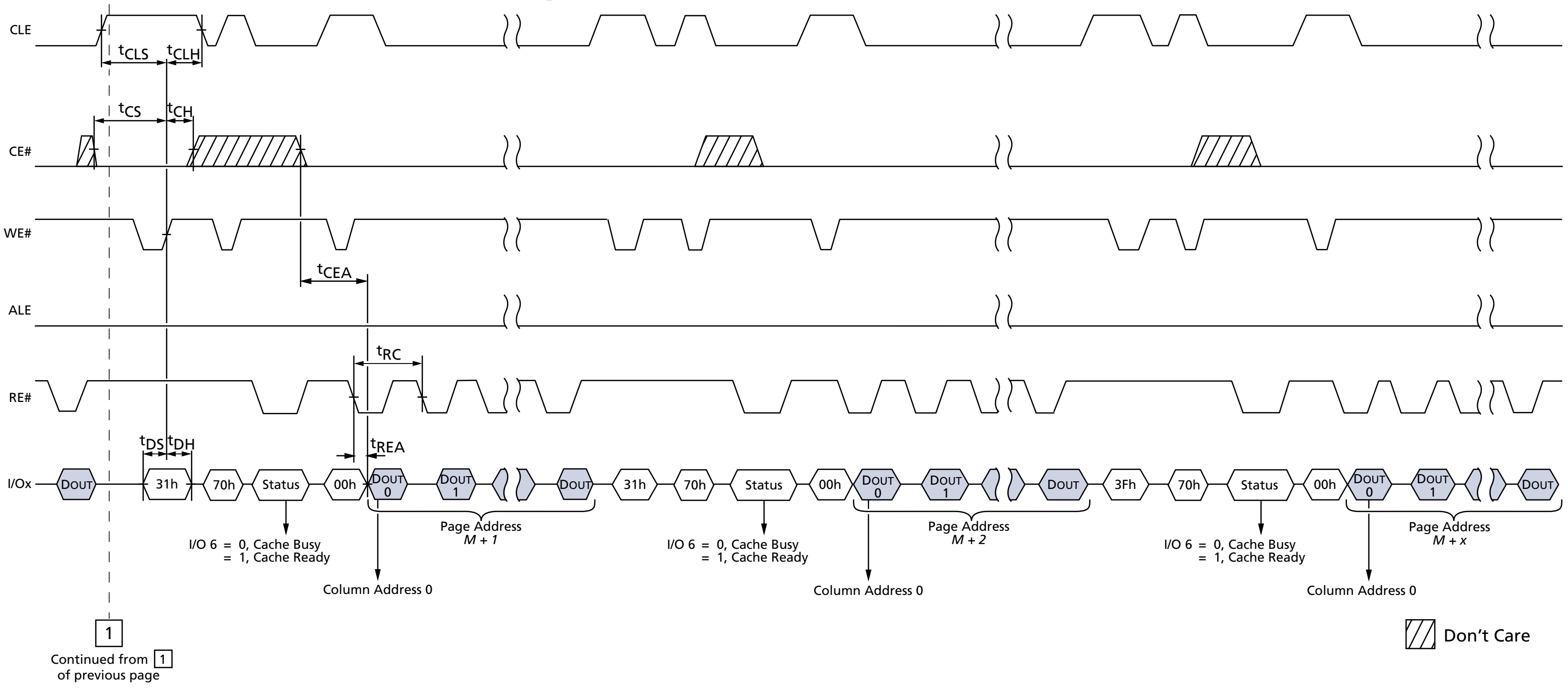
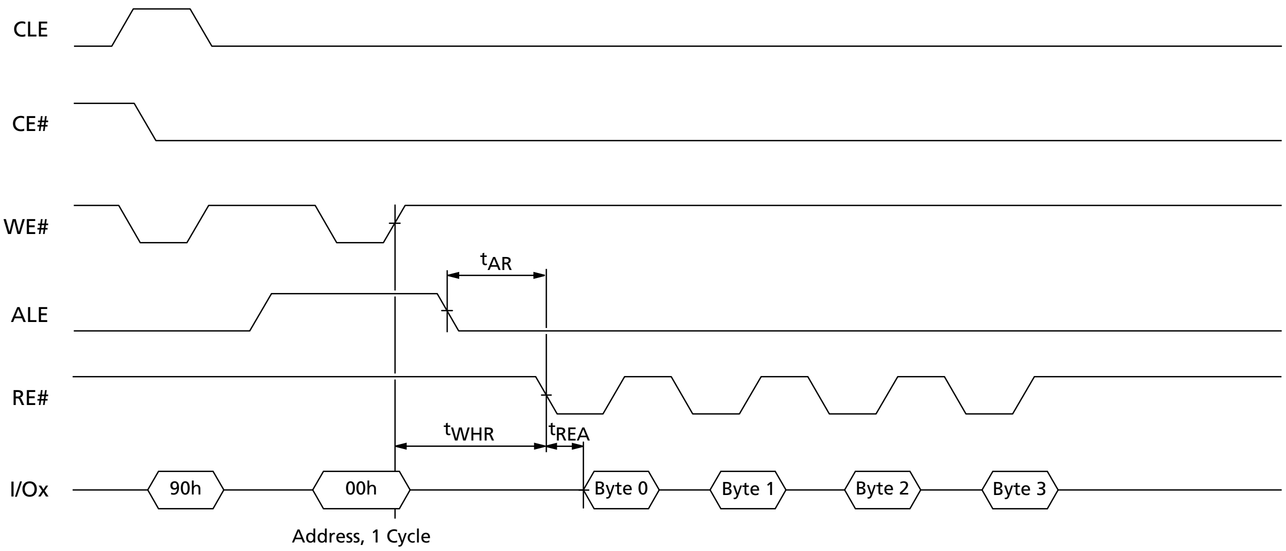


Figure 49: READ ID Operation



Note: See Table 10 on page 27 for byte definitions.

Figure 50: PROGRAM PAGE Operation

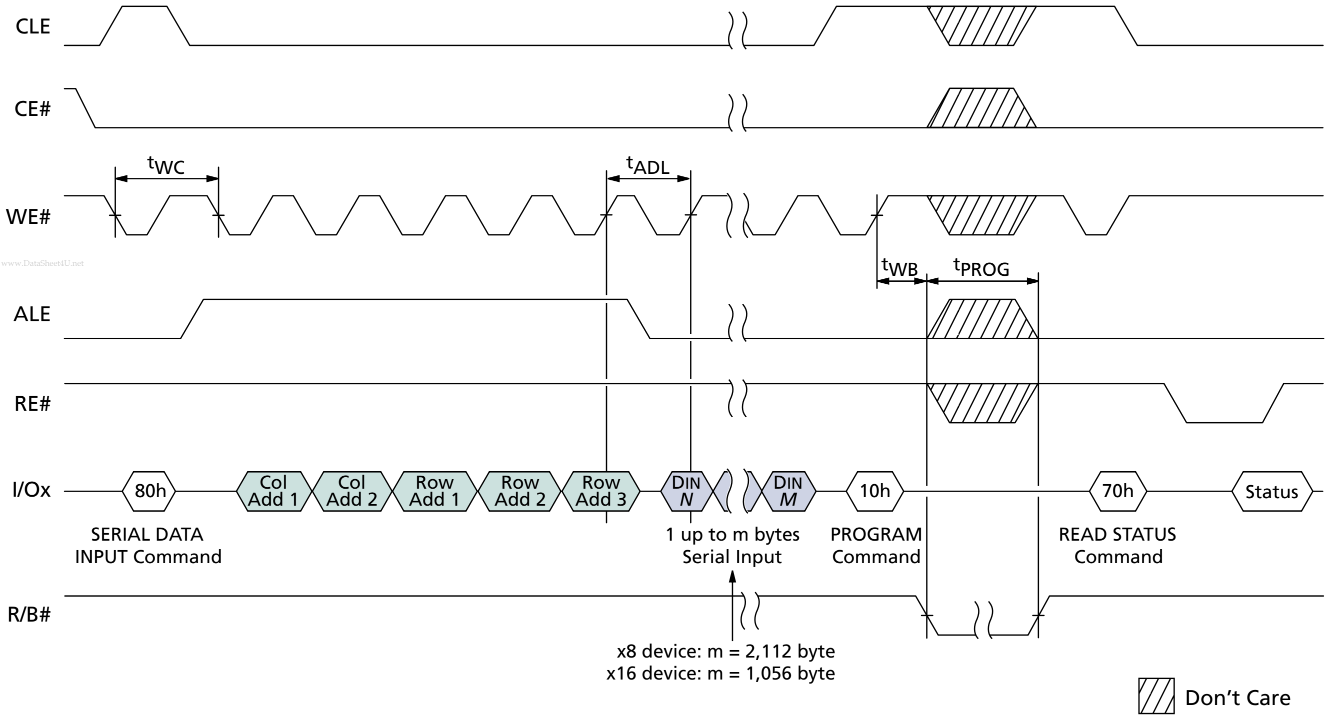


Figure 51: PROGRAM PAGE Operation with CE# "Don't Care"

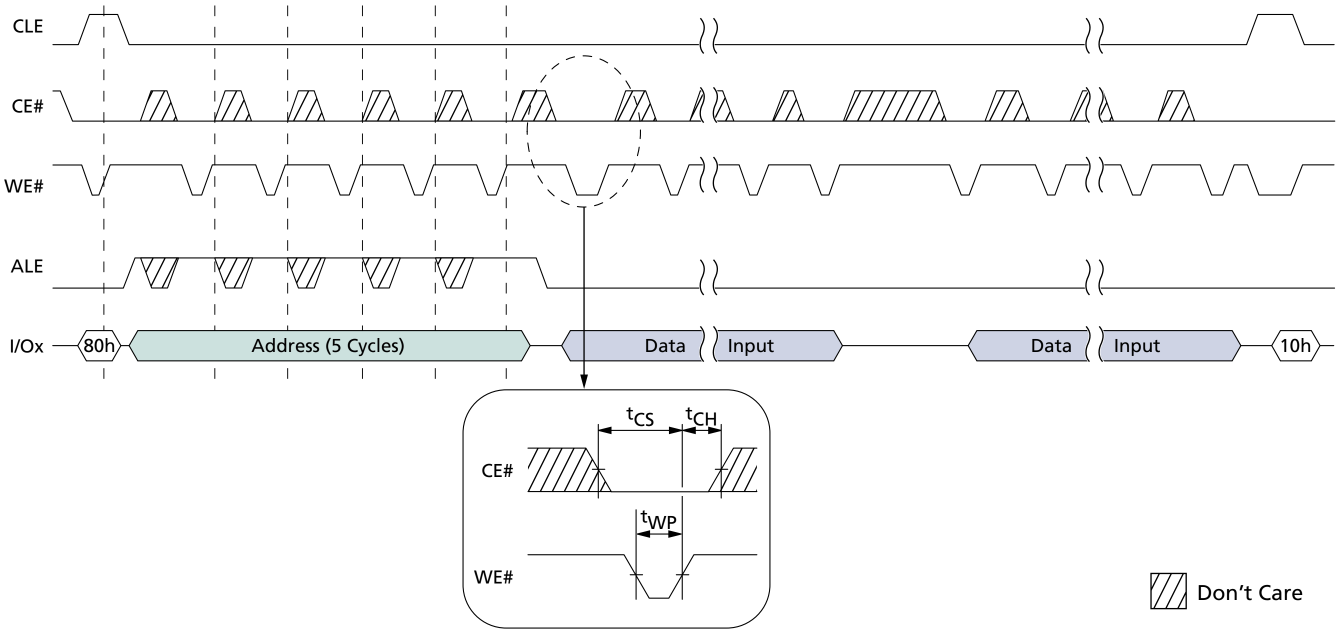


Figure 52: PROGRAM PAGE Operation with RANDOM DATA INPUT

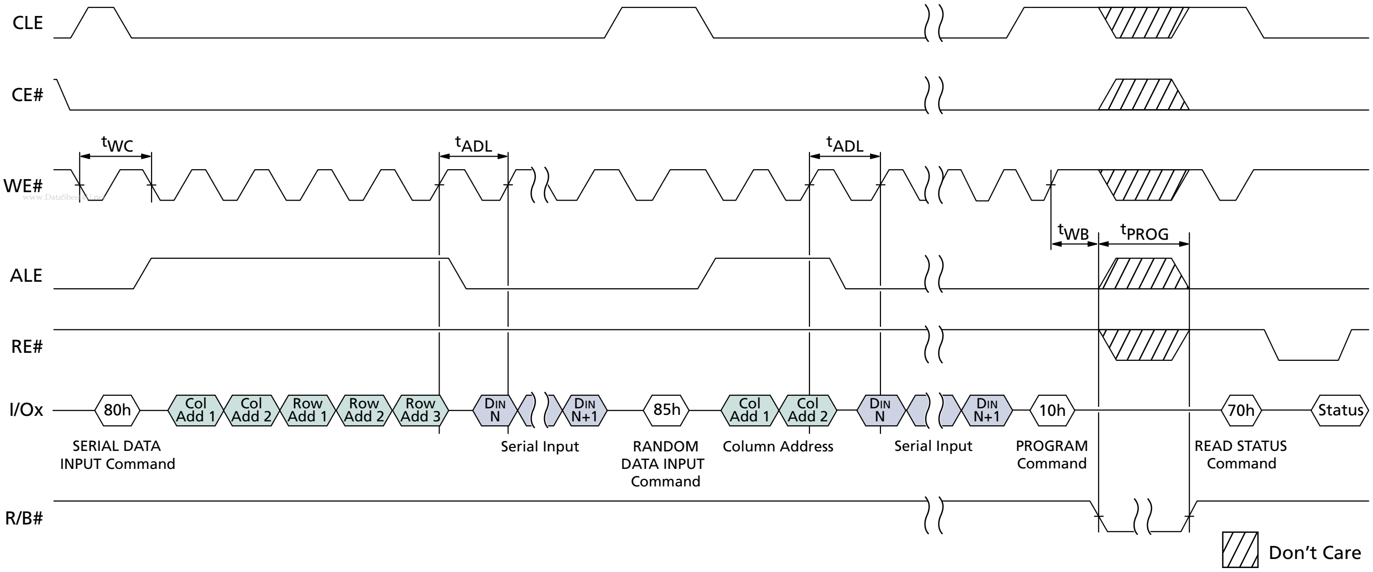


Figure 53: INTERNAL DATA MOVE

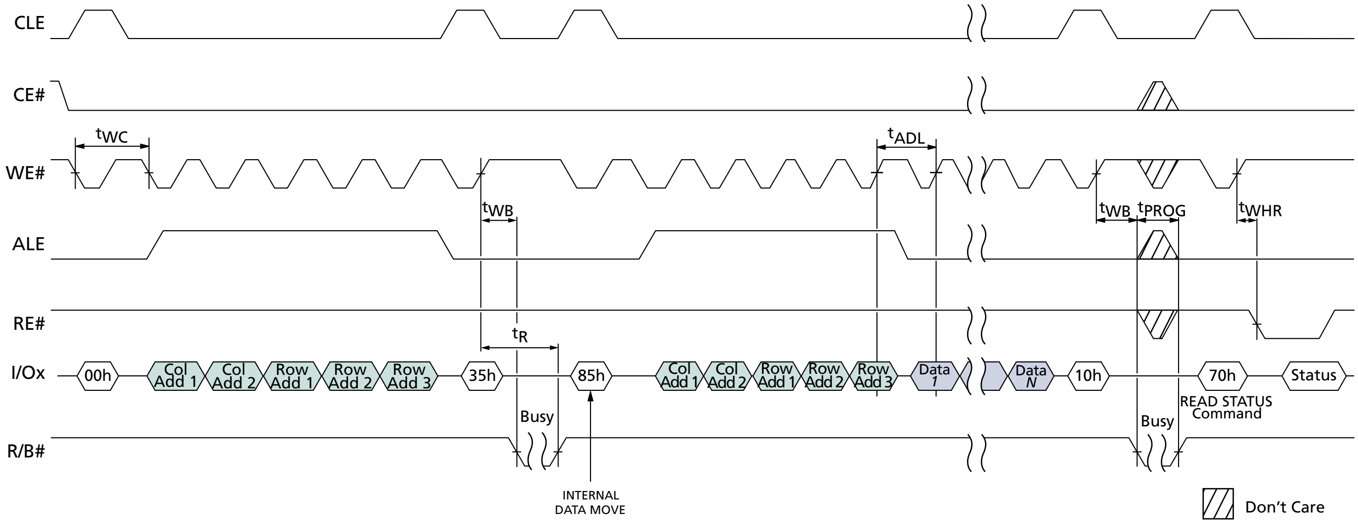


Figure 54: PROGRAM PAGE CACHE MODE

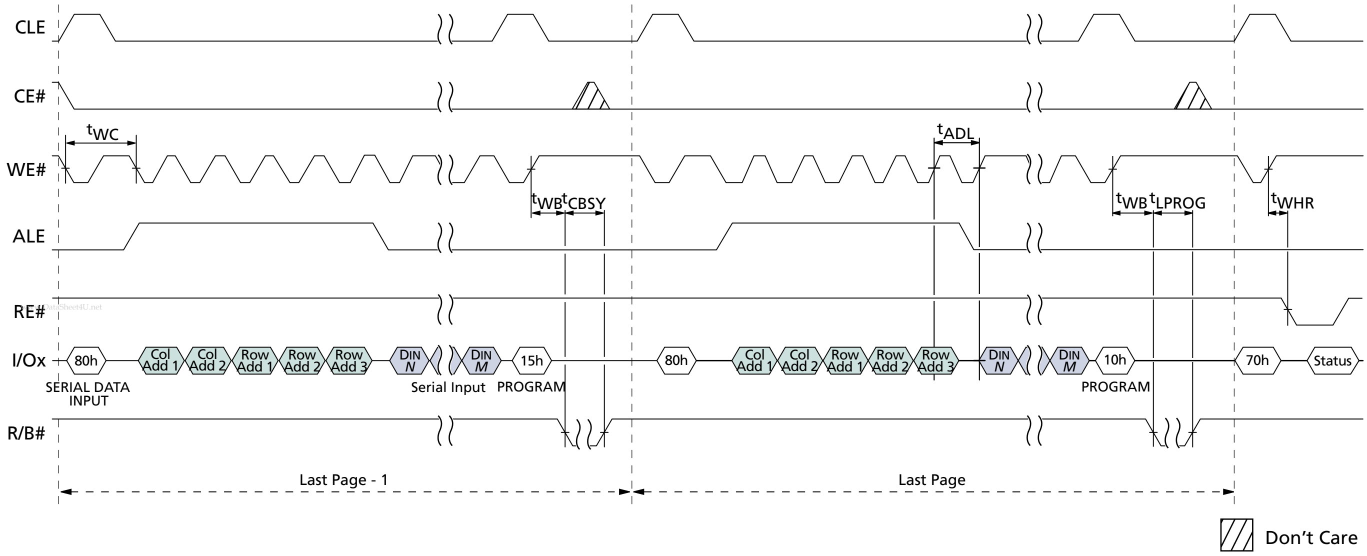
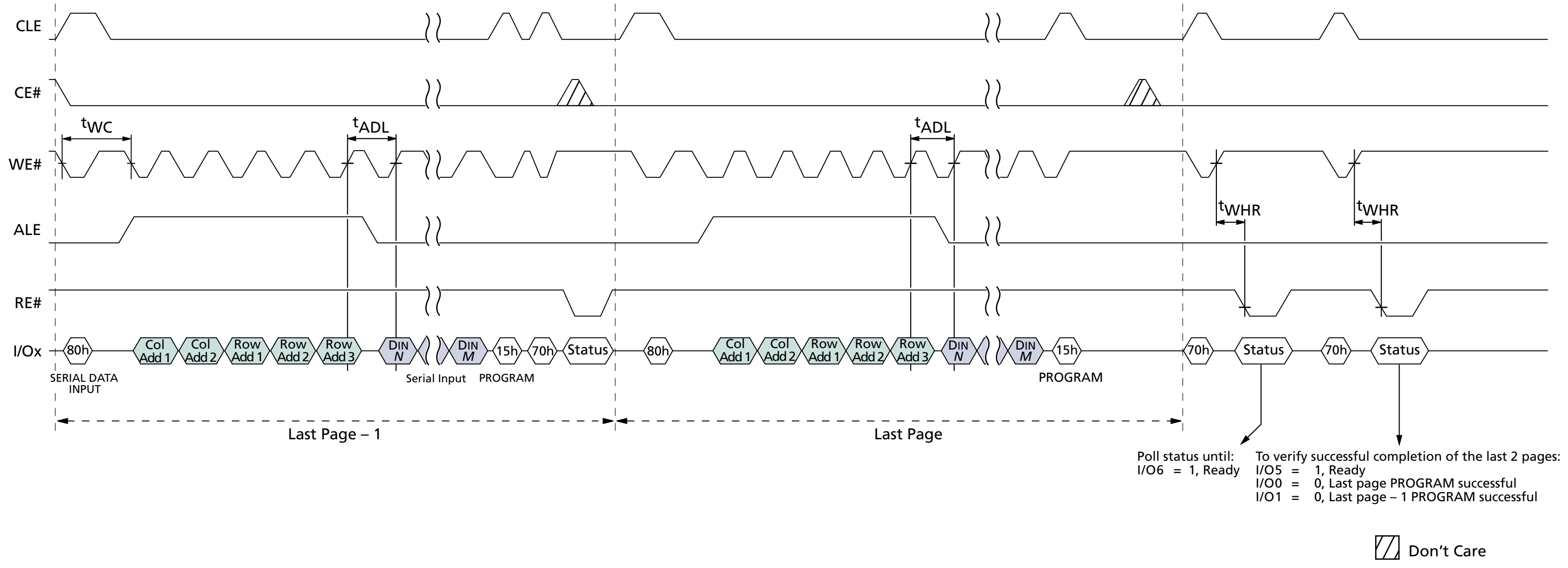


Figure 55: PROGRAM PAGE CACHE MODE Ending on 15h

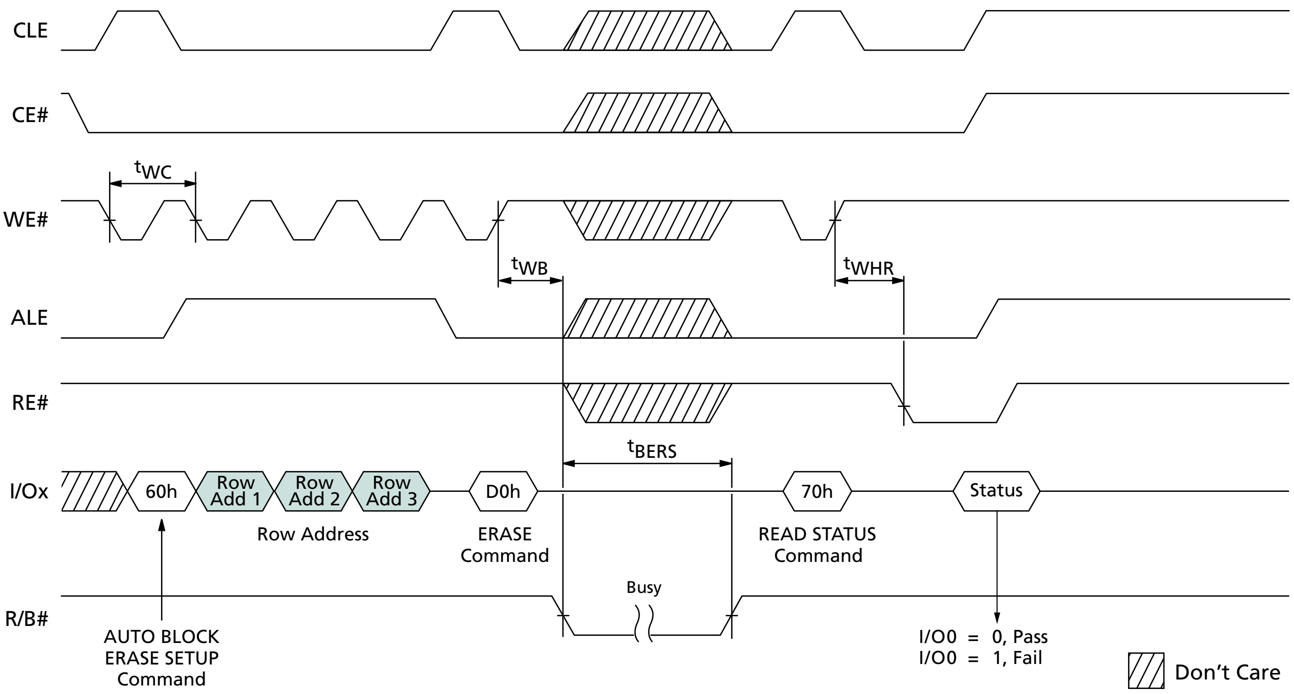


Poll status until:
I/O6 = 1, Ready

To verify successful completion of the last 2 pages:
I/O5 = 1, Ready
I/O0 = 0, Last page PROGRAM successful
I/O1 = 0, Last page – 1 PROGRAM successful

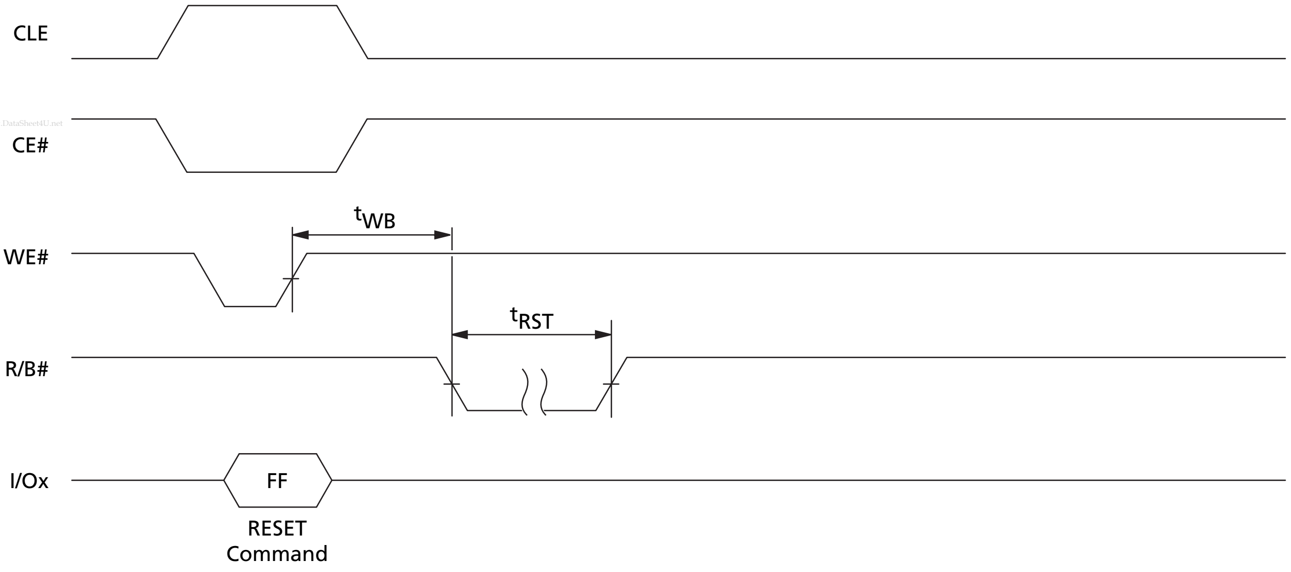
▨ Don't Care

Figure 56: BLOCK ERASE Operation



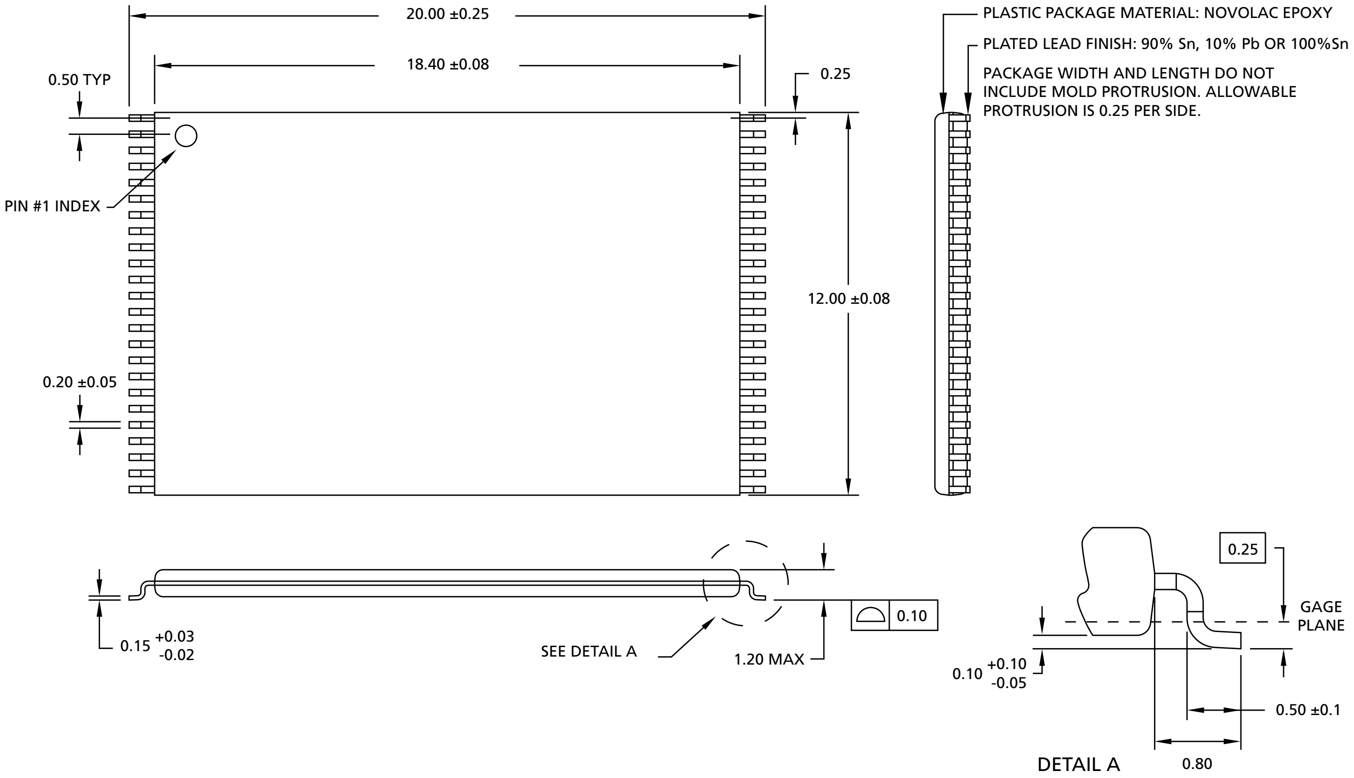
Notes: 1. See Table 10 on page 27 for actual values.

Figure 57: RESET Operation



Package Dimensions

Figure 58: TSOP Type I



Note: All dimensions in millimeters.

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Revision History

Rev. A 3/06

- Initial release.