FLASH MEMORY

MT28F320A18

Low Voltage, Extended Temperature
0.15µm Process Technology

FEATURES

32Mb block architecture
- Seventy-one erasable blocks:
- Eight 4K-word parameter blocks
- Sixty-three 32K-word main memory blocks

VCC, VCCQ, VPP voltages*
- 1.65V (MIN), 1.95V (MAX) VCC, VCCQ
- 0.9V (MIN), 1.95V (MAX) VPP (in-system
- PROGRAM/ERASE)
- 12V ±5% (HV) VPP tolerant (factory programming compatibility)

Random access time: 70ns @ 1.65V VCC

Low power consumption (VCC = 1.8V)
- Asynchronous Read < 18mA
- Write/Erase < 40mA (MAX)
- Standby < 50µA (MAX)
- Automatic power saving feature (APS)

Enhanced write and erase suspend options
- ERASE-SUSPEND-to-READ
- PROGRAM-SUSPEND-to-READ
- ERASE-SUSPEND-to-PROGRAM

Dual 64-bit chip protection registers for security purposes

Cross-compatible command support

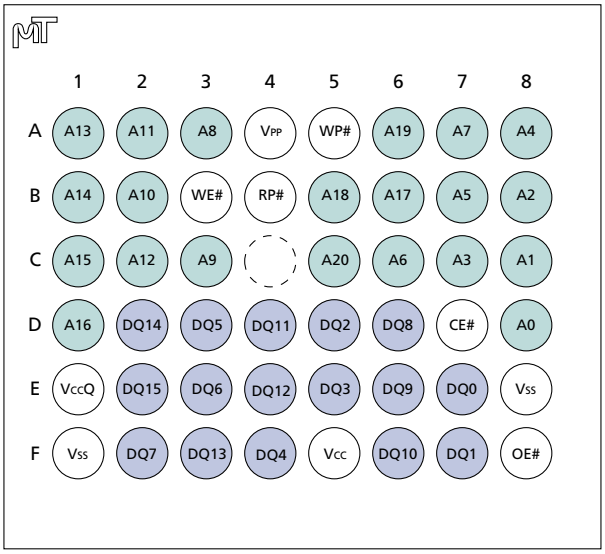
Extended command set

Common flash interface

PROGRAM/ERASE cycle
- 100,000 WRITE/ERASE cycles per block
- (VPP = VPP1)

*An extended voltage range of 1.65V–2.20V for Vcc and VccQ, and 0.9V–2.20V for Vpp is available upon request. A voltage range of 1.42V–1.60V for VccQ is also available upon request.

Ball Assignment
47-Ball FBGA



Top View
(Ball Down)

Note: See page 6 for Ball Description table.
See page 36 for mechanical drawing.

OPTIONS / MARKING

OPTIONS	MARKING
• Timing	
70ns access	-70
• Configurations	
2 Meg x 16	MT28F320A18
• Boot Block Configuration	
Top	T
Bottom	B
• Package	
47-ball FBGA (6 x 8 ball grid)	FF
• Temperature Range	
Extended (-40ºC to +85ºC)	ET

Part Number Example:
MT28F320A18FF-70 TET

GENERAL DESCRIPTION

The MT28F320A18 is a nonvolatile electrically block-erasable (Flash) memory containing eight 4K-word parameter blocks and sixty-three 32K-word main blocks.

The MT28F320A18 allows soft protection for blocks, as read only, by configuring soft protection registers with dedicated command sequences. For security purposes, a 128-bit chip protection register is provided.

The embedded WORD WRITE and BLOCK ERASE functions are fully automated by an on-chip write state machine (WSM). An on-chip status register can be used to monitor the WSM status and to determine the progress of the PROGRAM/ERASE task.

The ERASE/PROGRAM SUSPEND functionality allows compatibility with existing EEPROM emulation software packages.

The device is manufactured using 0.15µm process technology.

Please refer to Micron's Web site (www.micron.com/flash) for the latest data sheet.

ARCHITECTURE AND MEMORY ORGANIZATION

The MT28F320A18 contains eight 4K-word parameter blocks and sixty-three 32K-word main blocks.

Figure 2 and Figure 3 show the bottom and top memory organizations for the 32Mb device.

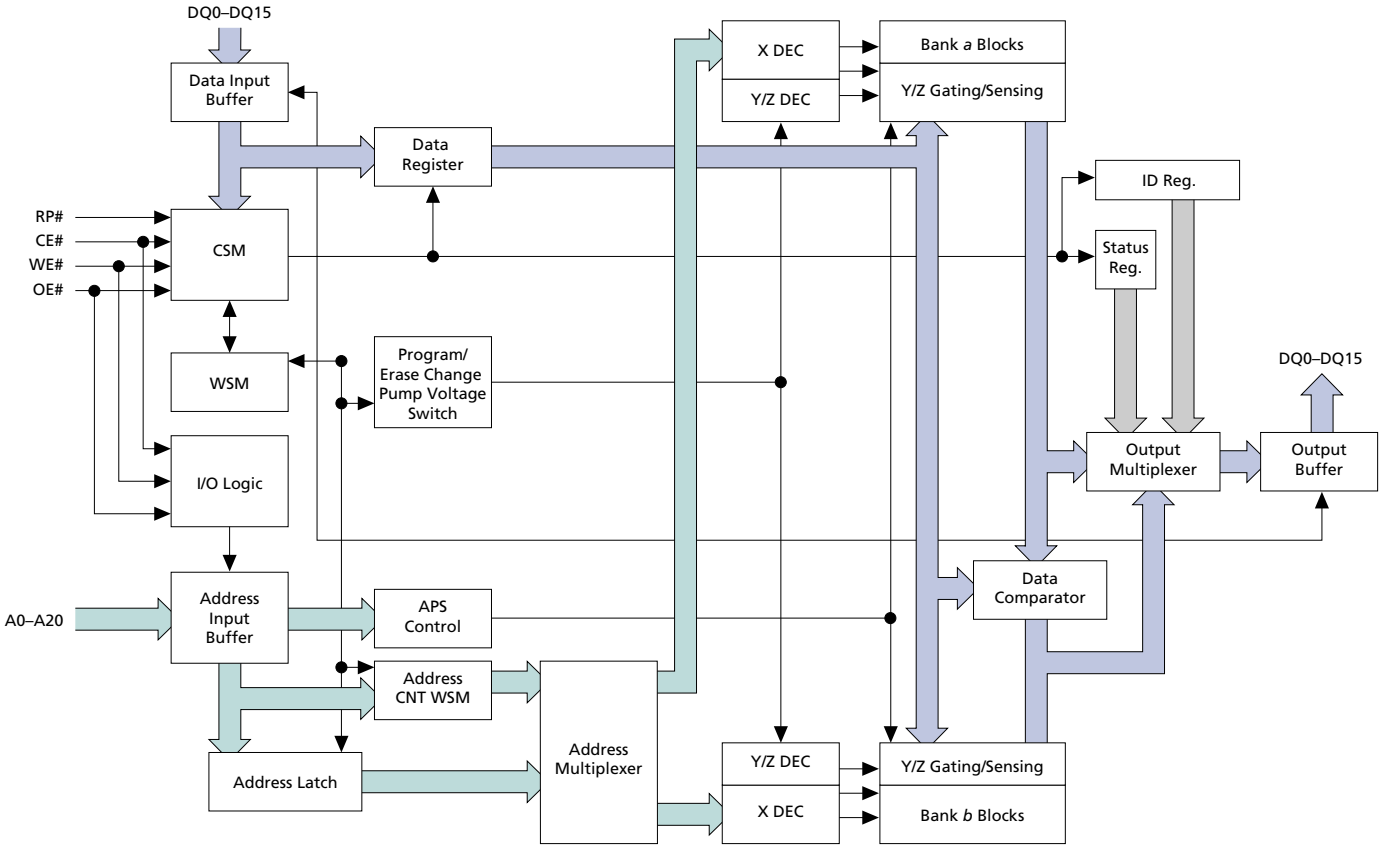
DEVICE MARKING

Due to the size of the package, Micron's standard part number is not printed on the top of each device. Instead, an abbreviated device mark comprised of a five-digit alphanumeric code is used. The abbreviated device marks are cross referenced to Micron part numbers in Table 1.

Table 1: Cross Reference for Abbreviated Device Marks

PART NUMBER	PRODUCT MARKING	SAMPLE MARKING	MECHANICAL SAMPLE MARKING
MT28F320A18FF-70 BET	FW722	FX722	FY722
MT28F320A18FF-70 TET	FW723	FX723	FY723

Functional Block Diagram



PART NUMBERING INFORMATION

Micron's low-power devices are available with several different combinations of features (see Figure 1). Valid combinations of features and their corresponding part numbers are listed in Table 2.

Figure 1: Part Number Chart

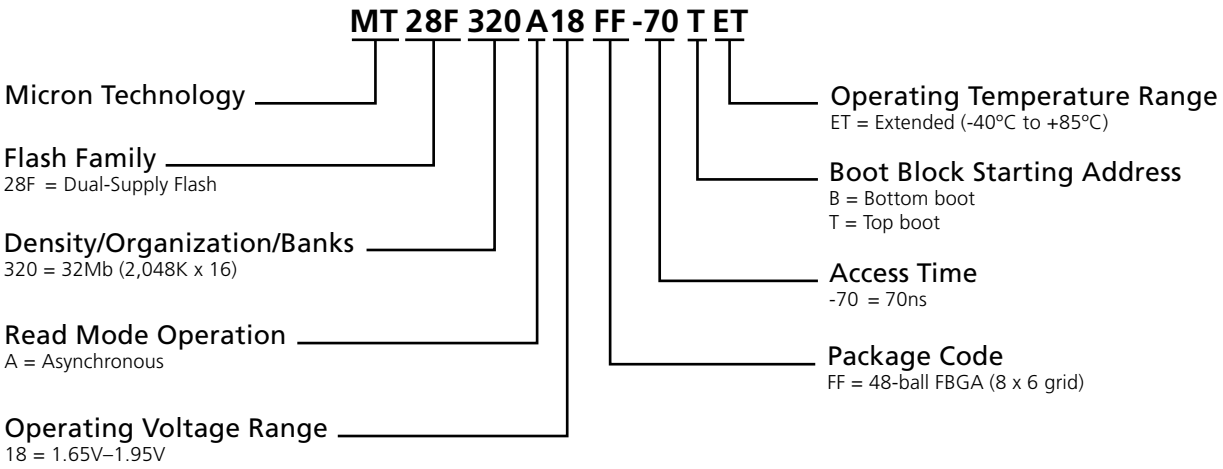


Table 2: Valid Part Number Combinations

PART NUMBER	ACCESS TIME (ns)	BOOT BLOCK STARTING ADDRESS	OPERATING TEMPERATURE RANGE
MT28F320A18FF-70 BET	70	Bottom	-40°C to +85°C
MT28F320A18FF-70 TET	70	Top	-40°C to +85°C

Figure 2: 32Mb Bottom Boot Block Memory Address Map

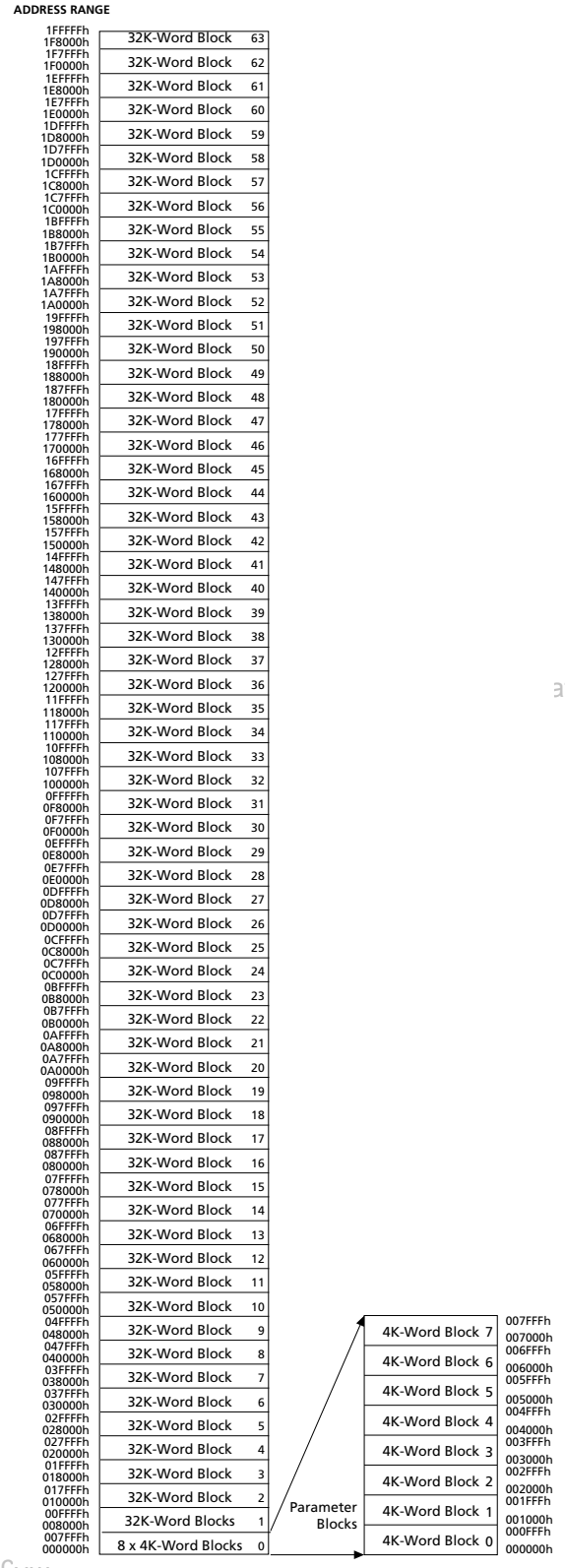
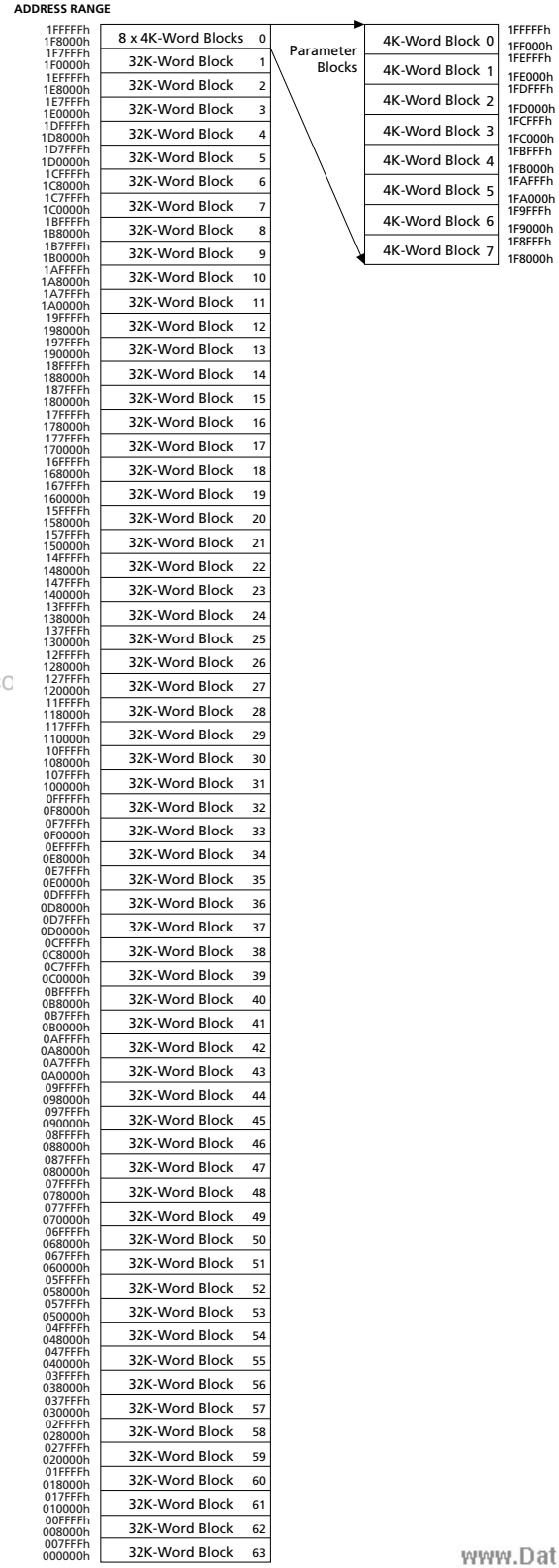


Figure 3: 32Mb Top Boot Block Memory Address Map



BALL DESCRIPTIONS

48-BALL FBGA NUMBERS	SYMBOL	TYPE	DESCRIPTION
D8, C8, B8, A8, C7, B7, A7, C6, B6, A6, C5, B5, C3, A3, C2, B2, A2, D1, C1, B1, A1	A0–A20	Input	Address Inputs: Inputs for the address during READ and WRITE operations. Addresses are internally latched during WRITE and ERASE cycles.
D7	CE#	Input	Chip Enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby power mode.
F8	OE#	Input	Output Enable: Enables the outputs buffer when LOW. When OE# is HIGH, the output buffers are disabled.
B3	WE#	Input	Write Enable: Determines if a given cycle is a WRITE cycle. If WE# is LOW, the cycle is either a WRITE to the command state machine (CSM) or to the memory array.
B4	RP#	Input	Reset: When RP# is a logic LOW, the device is in reset mode, which drives the outputs to High-Z and resets the write state machine (WSM). When RP# is at logic HIGH, the device is in standard operation. When RP# transitions from logic LOW to logic HIGH, the device resets all blocks to locked and defaults to the read array mode.
A5	WP#	Input	Write Protect: Controls the lock down function of the flexible locking feature.
E7, F7, D5, E5, F4, D3, E3, F2, D6, E6, F6, D4, E4, F3, D2, E2	DQ0–DQ15	Input/ Output	Data Inputs/Outputs: Inputs array data on the second CE# and WE# cycle during PROGRAM command. Inputs commands to the command user interface when CE# and WE# are active.
A4	V_{PP}	Supply	Block Erase and Program Power Supply: [V_{PP1} = 0.9V–1.95V or V_{PP2} = 11.4V–12.6V]. A valid voltage on this contact allows block erase or data programming. Memory contents cannot be altered when $V_{PP} \leq V_{PPLK}$. Block erase and program at invalid V_{PP} voltages should not be attempted. It provides factory programming compatibility when driven to 11.4V–12.6V
F5	V_{CC}	Supply	Device Power Supply: [1.65V–1.95V] Supplies power for device operation.
E1	V_{CCQ}	Supply	I/O Power Supply: [1.65V–1.95V] Supplies power for input/output buffers. This input should be tied directly to V_{CC}.
E8, F1	V_{SS}	Supply	Do not float any ground ball.
C4	NC	–	Internally not connected.

COMMAND STATE MACHINE

Commands are issued to the command state machine (CSM) using standard microprocessor write timings. The CSM acts as an interface between external microprocessors and the internal write state machine (WSM). The available commands are listed in Table 3, their definitions are given in Table 4 and their descriptions in Table 5. Program and erase algorithms are automated by an on-chip WSM. Table 6 shows the CSM transition states.

Once a valid PROGRAM/ERASE command is entered, the WSM executes the appropriate algorithm, which generates the necessary timing signals to control the device internally and accomplish the requested operation. A command is valid only if the exact sequence of WRITE cycles is completed. After the WSM completes its task, the WSM status bit (SR7) (see Table 8) is set to a logic HIGH level (1), allowing the CSM to respond to the full command set again.

OPERATIONS

Device operations are selected by entering a standard JEDEC 8-bit command code with conventional microprocessor timings into an on-chip CSM through I/Os DQ0–DQ7. The number of bus cycles required to activate a command is typically one or two. The first operation is always a WRITE. Control signals CE# and WE# must be at a logic LOW level (V_{IL}), and OE# and RP# must be at logic HIGH (V_{IH}). The second operation, when needed, can be a WRITE or a READ depending upon the command. During a READ operation, control signals CE# and OE# must be at a logic LOW level (Vil), and WE# and RP# must be at logic HIGH (V_{IH}).

Table 7 illustrates the bus operations for all the modes: write, read, reset, standby, and output disable.

When the device is powered up, internal reset circuitry initializes the chip to a read array mode of operation. Changing the mode of operation requires that a command code be entered into the CSM. An on-chip status register is available. The status register allows the monitoring of the progress of various operations that can take place on a memory. The status register is interrogated by entering a READ STATUS REGISTER command onto the CSM (cycle 1) and reading the register data on I/Os DQ0–DQ7 (cycle 2). Status register bits SR0–SR7 correspond to DQ0–DQ7 (see Table 8).

Command Definition

Once a specific command code has been entered, the WSM executes an internal algorithm, generating the necessary timing signals to program, erase, and verify data. See Table 4 for the CSM command definitions and data for each of the bus cycles.

Table 3: Command State Machine Codes For Device Mode Selection

COMMAND DQ0–DQ7	CODE ON DEVICE MODE
40h/10h	Program setup/alternate program setup
20h	Block erase setup
50h	Clear status register
60h	Protection configuration setup
70h	Read status register
90h	Read protection configuration register
98h	Read query
B0h	Program/erase suspend
C0h	Protection register program/lock
D0h	Program/erase resume – erase confirm
FFh	Read array

STATUS REGISTER

The status register allows the user to determine whether the state of a PROGRAM/ERASE operation is pending or complete. The status register is monitored by toggling OE# and CE# by reading the resulting status code on I/Os DQ0–DQ7. The high-order I/Os (DQ8–DQ15) are set to 00h internally, so only the low-order I/Os (DQ0–DQ7) need to be interpreted.

Register data is updated and latched on the falling edge of OE# or CE#, whichever occurs last. Latching the data prevents errors from occurring if the register input changes during a status register read.

The status register provides the internal state of the WSM to the external microprocessor. During periods when the WSM is active, the status register can be polled to determine the WSM status. Table 8 defines the status register bits.

After monitoring the status register during a PROGRAM/ERASE operation, the data appearing on DQ0–DQ7 remains as status register data until a new command is issued to the CSM. To return the device to other modes of operation, a new command must be issued to the CSM.

COMMAND STATE MACHINE OPERATIONS

The CSM decodes instructions for read array, read protection configuration register, read query, read status register, clear status register, program, erase, erase suspend, erase resume, erase confirm, program setup, alternate program setup, program suspend, program resume, lock block, unlock block and lock down block, chip protection register program, and chip protection register lock. The 8-bit command code is input to the device on DQ0–DQ7 (see Table 3 for CSM codes and Table 4 for command definitions). During a PROGRAM or ERASE cycle, the CSM informs the WSM that a PROGRAM or ERASE cycle has been requested. During a PROGRAM cycle, the WSM controls the program sequences and the CSM responds to a PROGRAM SUSPEND command only. During an ERASE cycle, the CSM responds to an ERASE SUSPEND command only. When the WSM has completed its task, the WSM status bit (SR7) is set to a logic HIGH level and the CSM responds to the full command set. The CSM stays in the current command state until the microprocessor issues another command.

The WSM successfully initiates an ERASE or PROGRAM operation only when V_{PP} is within its correct voltage range.

CLEAR STATUS REGISTER

The internal circuitry can set, but not clear, the block lock status bit (SR1), the V_{PP} status bit (SR3), the program status bit (SR4), and the erase status bit (SR5) of the status register. The CLEAR STATUS REGISTER command (50h) allows the external microprocessor to clear these status bits and synchronize to the internal operations. When the status bits are cleared, a READ ARRAY command (FFh) must be issued before data can be read from the memory array, or a READ STATUS REGISTER command (70h) must be issued to read status.

READ OPERATIONS

The following READ operations are available: READ ARRAY, READ PROTECTION CONFIGURATION REGISTER, READ QUERY and READ STATUS REGISTER.

Read Array

The array is read by entering the command code FFh on DQ0–DQ7. Control signals CE# and OE# must be at a logic LOW level (V_{IL}), and WE# and RP# must be at logic HIGH level (V_{IH}) to read data from the array. Data is available on DQ0–DQ15. Any valid address within any of the blocks selects that address and allows data to be read from that address. Upon initial power-up or device reset, the device defaults to the read array mode.

Read Chip Protection Configuration Register

The chip identification mode outputs four types of information: the manufacturer/device identifier, the block locking status, the protection register content, and protection register lock. Two bus cycles are required for this operation: the chip identification data is read by entering the command code 90h on DQ0–DQ7 and the identification code address on the address lines.

Control signals CE# and OE# must be at a logic LOW level (VIL), and WE# and RP# must be at a logic HIGH level (VIH) to read data from the protection configuration register. Data is available on DQ0–DQ15. To return to read array mode, write the read array command code FFh on DQ0–DQ7. See Table 10 for further details.

Table 4: Command Definitions

COMMAND	FIRST BUS CYCLE			SECOND BUS CYCLE		
	OPERATION	ADDRESS	DATA	OPERATION	ADDRESS	DATA
READ ARRAY	WRITE	X	FFh	READ	WA	AD
READ PROTECTION CONFIGURATION REGISTER	WRITE	X	90h	READ	IA	ID
READ STATUS REGISTER	WRITE	X	70h	READ	–	SRD
CLEAR STATUS REGISTER	WRITE	X	50h	–	–	–
READ QUERY	WRITE	X	98h	READ	QA	QD
BLOCK ERASE SETUP	WRITE	X	20h	WRITE	BA	D0h
PROGRAM SETUP/ALTERNATE PROGRAM SETUP	WRITE	X	40h/10h	WRITE	WA	WD
PROGRAM/ERASE SUSPEND	WRITE	X	B0h	–	–	–
PROGRAM/ERASE RESUME – ERASE CONFIRM	WRITE	X	D0h	–	–	–
LOCK BLOCK	WRITE	X	60h	WRITE	BA	01h
UNLOCK BLOCK	WRITE	X	60h	WRITE	BA	D0h
LOCK DOWN BLOCK	WRITE	X	60h	WRITE	BA	2Fh
PROTECTION REGISTER PROGRAM SETUP	WRITE	X	C0h	WRITE	PA	PD
PROTECTION REGISTER LOCK	WRITE	X	C0h	WRITE	LPA	FFFDh

WA: Word address of memory location to be written, or read
IA: Identification code address
BA: Address within the block
ID: Identification code data
SRD: Data read from the status register
QA: Query code address
QD: Query code data
WD: Data to be written at the location WA
PA: Protection register address
LPA: Lock protection register address
AD: Array data
PD: Protection register data
X: "Don't Care"

Table 5: Command Descriptions

CODE	DEVICE MODE	BUS CYCLE	DESCRIPTION
10h	Alt. Program Setup	First	Operates the same as a PROGRAM SETUP command.
20h	Erase Setup	First	Prepares the CSM for an ERASE CONFIRM command. If the next command is not an ERASE CONFIRM command, the command will be ignored, and the device will go to read status mode and wait for another command.
40h	Program Setup	First	A two-cycle command: The first cycle prepares for a PROGRAM operation, the second cycle latches addresses and data and initiates the WSM to execute the program algorithm. The Flash device outputs status register data on the falling edge of OE# or CE#, whichever occurs first.
50h	Clear Status Register	First	The WSM can set the block lock status (SR1), V_{PP} Status (SR3), program status (SR4),and erase status (SR5) bits in the status register to "1," but it cannot clear them to "0." Issuing this command clears those bits to "0."
60h	Protection Configuration Setup	First	Prepares the CSM for changes to the block locking status. If the next command is not BLOCK UNLOCK, BLOCK LOCK, or BLOCK LOCK DOWN, then the CSM will set both the program and erase status register bits to indicate a command sequence error.
70h	Read Status Register	First	Places the device into read status register mode. Reading the device will output the contents of the status register for the addressed bank. The device will automatically enter this mode for the addressed bank after a PROGRAM or ERASE operation has been initiated.
90h	Read Protection Configuration Register	First	Puts the device into the read protection configuration register mode so that reading the device will output the manufacturer/device codes, block lock status, protection register, or protection register lock.
98h	Read Query	First	Puts the device into the read query mode so that reading the device will output common flash interface information.
B0h	Program/Erase Suspend	First	Suspends the currently executing PROGRAM/ERASE operation. The status register will indicate when the operation has been successfully suspended by setting either the program suspend (SR2) or erase suspend (SR6) and the WSM status bit (SR7) to a "1" (ready). The WSM will continue to idle in the suspend state, regardless of the state of all input control pins except RP#, which will immediately shut down the WSM and the remainder of the chip if RP# is driven to V_{IL}.
C0h	Program Device Protection Register	First	Writes a specific code into the device protection register.
	Lock Device Protection Register	First	Locks the device protection register; data can no longer be changed.
D0h	Erase Confirm	Second	If the previous command was an ERASE SETUP command, then the CSM will close the address and data latches, and it will begin erasing the block indicated on the address pins. During programming/erase, the device will respond only to the READ STATUS REGISTER, PROGRAM/ERASE SUSPEND commands and will output status register data on the falling edge of OE# or CE#, whichever occurs last.
	Program/Erase Resume	First	If a program or erase operation was previously suspended, this command will resume the operation.
FFh	Read Array	First	During the read array mode, array data will be output on the data bus.
01h	Lock Block	Second	If the previous command was PROTECTION CONFIGURATION SETUP, the CSM will latch the address and lock the block indicated on the address bus.

Table 5: Command Descriptions (continued)

CODE	DEVICE MODE	BUS CYCLE	DESCRIPTION
2Fh	Lock Down	Second	If the previous command was PROTECTION CONFIGURATION SETUP, the CSM will latch the address and lock down the block indicated on the address bus.
D0h	Unlock Block	Second	If the previous command was PROTECTION CONFIGURATION SETUP, the CSM will latch the address and unlock the block indicated on the address bus. If the block had been previously set to lock down, this operation will have no effect.
00h	Invalid/Reserved		Unassigned command that should not be used.

Read Query

The read query mode outputs common flash interface (CFI) data when the device is read (see Table 12). Two bus cycles are required for this operation. It is possible to access the query by writing the read query command code 98h on DQ0–DQ7. Control signals CE# and OE# must be at a logic LOW level (V_{IL}), and WE# and RP# must be at logic HIGH level (V_{IH}) to read data from the query. The CFI data structure contains information such as block size, density, command set, and electrical specifications. To return to read array mode, write the read array command code FFh on DQ0–DQ7.

Read Status Register

The status register is read by entering the command code 70h on DQ0–DQ7. Two bus cycles are required for this operation: one to enter the command code and a second to read the status register. In a READ cycle, the register data is updated on the falling edge of OE# or CE#, whichever occurs last.

PROGRAMMING OPERATIONS

There are two CSM commands for programming: PROGRAM SETUP and ALTERNATE PROGRAM SETUP (see Table 3).

After the desired command code is entered (10h or 40h command code on DQ0–DQ7), the WSM takes over and correctly sequences the device to complete the PROGRAM operation. The WRITE operation may be monitored through the status register (see the Status Register section). During this time, the CSM will only respond to a PROGRAM SUSPEND command until the PROGRAM operation has been completed, after which time all commands to the CSM become valid again. The PROGRAM operation can be suspended by issuing a PROGRAM SUSPEND command (B0h). Once the WSM reaches the suspend state, it allows the CSM to respond only to READ ARRAY, READ STATUS REGISTER, READ PROTECTION CONFIGURATION, READ QUERY, and PROGRAM RESUME. During the PROGRAM SUSPEND operation, array data should be read from an address other than the one being programmed. To resume the PROGRAM operation, a PROGRAM RESUME command (D0h) must be issued to cause the CSM to clear the suspend state previously set (see Figure 4 for programming operation and Figure 5 for program suspend and program resume).

During programming, V_{PP} must remain in the appropriate V_{PP} voltage range as shown in the Recommended Operating Conditions table.

ERASE OPERATIONS

An ERASE operation must be used to initialize all bits in an array block to “1”. After BLOCK ERASE CONFIRM is issued, the CSM responds only to an ERASE SUSPEND command until the WSM completes its task.

Block erasure inside the memory array sets all bits within the address block to logic "1". Erase is accomplished only by blocks; data at single address locations within the array cannot be erased individually. The block to be erased is selected by using any valid address within that block. Block erasure is initiated by a command sequence to the CSM: BLOCK ERASE SETUP (20h) followed by BLOCK ERASE CONFIRM (D0h) (see Figure 6). A two-command erase sequence protects against accidental erasure of memory contents.

When the BLOCK ERASE CONFIRM command is complete, the WSM automatically executes a sequence of events to complete the block erasure. During this sequence, the block is programmed with logic "0", data is verified, all bits in the block are erased, and finally verification is performed to ensure that all bits are correctly erased. Monitoring the ERASE operation is possible through the status register (see the Status Register section).

During the execution of an ERASE operation the ERASE SUSPEND command (B0h) can be entered to direct the WSM to suspend the ERASE operation. Once the WSM has reached the suspend state, it allows the CSM to respond only to the READ ARRAY, READ STATUS REGISTER, READ QUERY, READ CHIP PROTECTION CONFIGURATION, PROGRAM SETUP, PROGRAM/ERASE RESUME and LOCK SETUP (see the Block Locking section). During the ERASE SUSPEND operation, array data must be read from a block other than the one being erased. To resume the ERASE operation, an ERASE RESUME command (D0h) must be issued to cause the CSM to clear the suspend state previously set (see Figure 7). It is also possible that an ERASE can be suspended and a write to another block can be initiated. After the completion of a write, an erase can be resumed by writing an ERASE RESUME command.

Table 6: Command State Machine Current/Next States

CURRENT STATE	SR7	COMMAND INPUT AND NEXT STATE						
		DATA WHEN READ	READ ARRAY	READ CONFIG.	READ STATUS REG.	CLEAR STATUS REG.	READ QUERY	ERASE SETUP
			FF	90	70	50	98	20
Read Array	1	Array	Read Array	Read Configuration	Read Status	Clear Status	Read Query	Erase Setup
Read Status	1	Status	Read Array	Read Configuration	Read Status	Clear Status	Read Query	Erase Setup
Read Configuration	1	Config.	Read Array	Read Configuration	Read Status	Clear Status	Read Query	Erase Setup
Read Query	1	CFI	Read Array	Read Configuration	Read Status	Clear Status	Read Query	Erase Setup
Clear Status	0	Status	Read Array	Read Configuration	Read Status	Clear Status	Read Query	Erase Setup
Program Setup	1	Status	Program					
Program (not done)	0	Status	Program					
Program (done)	1	Status	Read Array	Read Configuration	Read Status	Clear Status	Read Query	Erase Setup
Program Suspend Read Array	1	Array	Program Suspend Read Array	Program Suspend Read Configuration	Program Suspend Read Status	Program Suspend Clear Status	Program Suspend Read Query	Program Suspend Read Array
Program Suspend Read Status	1	Status	Program Suspend Read Array	Program Suspend Read Configuration	Program Suspend Read Status	Program Suspend Clear Status	Program Suspend Read Query	Program Suspend Read Array
Program Suspend Read Configuration	1	Config.	Program Suspend Read Array	Program Suspend Read Configuration	Program Suspend Read Status	Program Suspend Clear Status	Program Suspend Read Query	Program Suspend Read Array
Program Suspend Read Query	1	CFI	Program Suspend Read Array	Program Suspend Read Configuration	Program Suspend Read Status	Program Suspend Clear Status	Program Suspend Read Query	Program Suspend Read Array
Erase Setup	1	Status	Erase Command Error					
Erase (Not Done)	0	Status	Erase					
Erase (Done)	1	Status	Read Array	Read Configuration	Read Status	Clear Status	Read Query	Erase Setup
Erase Command Error	1	Status	Read Array	Read Configuration	Read Status	Clear Status	Read Query	Erase Setup
Program Setup in Erase Suspend	1	Status	Program in Erase Suspend					
Erase Suspend Program (Not Done)	1	Status	Program in Erase Suspend					
Erase Suspend (Done)	1	Status	Erase Suspend Read Array	Erase Suspend Read Configuration	Erase Suspend Read Status	Erase Suspend Clear Status	Erase Suspend Read Query	Erase Suspend Read Array
Erase Suspend Read Array	1	Array	Erase Suspend Read Array	Erase Suspend Read Configuration	Erase Suspend Read Status	Erase Suspend Clear Status	Erase Suspend Read Query	Erase Suspend Read Array
Erase Suspend Read Status	1	Status	Erase Suspend Read Array	Erase Suspend Read Configuration	Erase Suspend Read Status	Erase Suspend Clear Status	Erase Suspend Read Query	Erase Suspend Read Array
Erase Suspend Read Configuration	1	Config.	Erase Suspend Read Array	Erase Suspend Read Configuration	Erase Suspend Read Status	Erase Suspend Clear Status	Erase Suspend Read Query	Erase Suspend Read Array
Erase Suspend Read Query	1	CFI	Erase Suspend Read Array	Erase Suspend Read Configuration	Erase Suspend Read Status	Erase Suspend Clear Status	Erase Suspend Read Query	Erase Suspend Read Array
Erase Suspend Lock Setup	1	Status	Erase Suspend Lock Error					
Erase Suspend Lock	1	Status	Erase Suspend Read Array	Erase Suspend Read Configuration	Erase Suspend Read Status	Erase Suspend Clear Status	Erase Suspend Read Query	Erase Suspend Read Array
Erase Suspend Lock Down	1	Status	Erase Suspend Read Array	Erase Suspend Read Configuration	Erase Suspend Read Status	Erase Suspend Clear Status	Erase Suspend Read Query	Erase Suspend Read Array

Table 6: Command State Machine Current/Next States (continued)

CURRENT STATE	SR7	DATA WHEN READ	COMMAND INPUT AND NEXT STATE					
			READ ARRAY	READ CONFIG.	READ STATUS REG.	CLEAR STATUS REG.	READ QUERY	ERASE SETUP
			FF	90	70	50	98	20
Erase Suspend Unlock	1	Status	Erase Suspend Read Array	Erase Suspend Read Configuration	Erase Suspend Read Status	Erase Suspend Clear Status	Erase Suspend Read Query	Erase Suspend Read Array
Erase Suspend Lock Error	1	Status	Erase Suspend Read Array	Erase Suspend Read Configuration	Erase Suspend Read Status	Erase Suspend Clear Status	Erase Suspend Read Query	Erase Suspend Read Array
Erase Suspend Program Suspend Read Array	1	Array	Erase Suspend Program Suspend Read Array	Erase Suspend Program Suspend Read Configuration	Erase Suspend Program Suspend Read Status	Erase Suspend Program Suspend Clear Status	Erase Suspend Program Suspend Read Query	Erase Suspend Program Suspend Read Array
Erase Suspend Program Suspend Read Status	1	Status	Erase Suspend Program Suspend Read Array	Erase Suspend Program Suspend Read Configuration	Erase Suspend Program Suspend Read Status	Erase Suspend Program Suspend Clear Status	Erase Suspend Program Suspend Read Query	Erase Suspend Program Suspend Read Array
Erase Suspend Program Suspend Read Configuration	1	Config.	Erase Suspend Program Suspend Read Array	Erase Suspend Program Suspend Read Configuration	Erase Suspend Program Suspend Read Status	Erase Suspend Program Suspend Clear Status	Erase Suspend Program Suspend Read Query	Erase Suspend Program Suspend Read Array
Erase Suspend Program Suspend Read Query	1	CFI	Erase Suspend Program Suspend Read Array	Erase Suspend Program Suspend Read Configuration	Erase Suspend Program Suspend Read Status	Erase Suspend Program Suspend Clear Status	Erase Suspend Program Suspend Read Query	Erase Suspend Program Suspend Read Array
OTP Program Setup	1	Status	OTP Program					
OTP Program (Not Done)	0	Status	OTP Program					
OTP Program (Done)	1	Status	Read Array	Read Configuration	Read Status	Clear Status	Read Query	Erase Setup
Lock Setup	1	Status	Lock Error					
Lock	1	Status	Read Array	Read Configuration	Read Status	Clear Status	Read Query	Erase Setup
Lock Down	1	Status	Read Array	Read Configuration	Read Status	Clear Status	Read Query	Erase Setup
Unlock	1	Status	Read Array	Read Configuration	Read Status	Clear Status	Read Query	Erase Setup
Lock Error	1	Status	Read Array	Read Configuration	Read Status	Clear Status	Read Query	Erase Setup

Table 6: Command State Machine Current/Next States (continued)

CURRENT STATE	SR7	COMMAND INPUT AND NEXT TABLE						
		PROGRAM/ ERASE RESUME, UNLOCK	PROGRAM SETUP	PROGRAM/ ERASE SUSPEND	OTP PROGRAM SETUP	LOCK SETUP	LOCK	LOCK DOWN
		D0	10/40	B0	C0	60	01	2F
Read Array	1	Read Array	Program Setup	Read Array	OTP Program Setup	Lock Setup	Read Array	
Read Status	1	Read Array	Program Setup	Read Array	OTP Program Setup	Lock Setup	Read Array	
Read Configuration	1	Read Array	Program Setup	Read Array	OTP Program Setup	Lock Setup	Read Array	
Read Query	1	Read Array	Program Setup	Read Array	OTP Program Setup	Lock Setup	Read Array	
Clear Status	1	Read Array	Program Setup	Read Array	OTP Program Setup	Lock Setup	Read Array	
Program Setup	1	Program						
Program (not done)	0	Program		Program Suspend Status	Program			
Program (done)	1	Read Array	Program Setup	Read Array	OTP Program Setup	Lock Setup	Read Array	
Program Suspend Read Array	1	Program	Program Suspend Read Array					
Program Suspend Read Status	1	Program	Program Suspend Read Array					
Program Suspend Read Configuration	1	Program	Program Suspend Read Array					
Program Suspend Read Query	1	Program	Program Suspend Read Array					
Erase Setup	1	Erase	Erase Command Error					
Erase (Not Done)	0			Erase Suspend Read Status	Erase			
Erase (Done)	1	Read Array	Program Setup	Read Array	OTP Program Setup	Lock Setup	Read Array	
Erase Command Error	1	Read Array	Program Setup	Read Array	OTP Program Setup	Lock Setup	Read Array	
Program Setup in Erase Suspend	1	Program in Erase Suspend						
Erase Suspend Program (Not Done)	1	Program in Erase Suspend		Erase Suspend Program Suspend Read Status	Program in Erase Suspend			
Erase Suspend (Done)	1	Erase	Program Setup in Erase Suspend	Erase Suspend Read Array		Erase Suspend Lock Setup	Erase Suspend Read Array	
Erase Suspend Read Array	1	Erase	Program Setup in Erase Suspend	Erase Suspend Read Array		Erase Suspend Lock Setup	Erase Suspend Read Array	
Erase Suspend Read Status	1	Erase	Program Setup in Erase Suspend	Erase Suspend Read Array		Erase Suspend Lock Setup	Erase Suspend Read Array	
Erase Suspend Read Configuration	1	Erase	Program Setup in Erase Suspend	Erase Suspend Read Array		Erase Suspend Lock Setup	Erase Suspend Read Array	
Erase Suspend Read Query	1	Erase	Program Setup in Erase Suspend	Erase Suspend Read Array		Erase Suspend Lock Setup	Erase Suspend Read Array	
Erase Suspend Lock Setup	1	Erase Suspend Unlock	Erase Suspend Lock Error				Erase Suspend Lock	Erase Suspend Lock Down
Erase Suspend Lock	1	Erase	Program Setup in Erase Suspend	Erase Suspend Read Array		Erase Suspend Lock Setup	Erase Suspend Read Array	
Erase Suspend Lock Down	1	Erase	Program Setup in Erase Suspend	Erase Suspend Read Array		Erase Suspend Lock Setup	Erase Suspend Read Array	

Table 6: Command State Machine Current/Next States (continued)

CURRENT STATE	SR7	COMMAND INPUT AND NEXT TABLE						
		PROGRAM/ ERASE RESUME, UNLOCK	PROGRAM SETUP	PROGRAM/ ERASE SUSPEND	OTP PROGRAM SETUP	LOCK SETUP	LOCK	LOCK DOWN
		D0	10/40	B0	C0	60	01	2F
Erase Suspend Unlock	1	Erase	Program Setup in Erase Suspend	Erase Suspend Read Array		Erase Suspend Lock Setup	Erase Suspend Read Array	
Erase Suspend Lock Error	1	Erase	Program Setup in Erase Suspend	Erase Suspend Read Array		Erase Suspend Lock Setup	Erase Suspend Read Array	
Erase Suspend Program Suspend Read Array	1	Erase Suspend Program	Erase Suspend Program Suspend Read Array					
Erase Suspend Program Suspend Read Status	1	Erase Suspend Program	Erase Suspend Program Suspend Read Array					
Erase Suspend Program Susp. Read Configuration	1	Erase Suspend Program	Erase Suspend Program Suspend Read Array					
Erase Suspend Program Suspend Read Query	1	Erase Suspend Program	Erase Suspend Program Suspend Read Array					
OTP Program Setup	1							
OTP Program (Not Done)	0							
OTP Program (Done)	1	Read Array	Program Setup	Read Array	OTP Program Setup	Lock Setup	Read Array	
Lock Setup	1	Unlock	Lock Error				Lock	Lock Down
Lock	1	Read Array	Program Setup	Read Array	OTP Program Setup	Lock Setup	Read Array	
Lock Down	1	Read Array	Program Setup	Read Array	OTP Program Setup	Lock Setup	Read Array	
Unlock	1	Read Array	Program Setup	Read Array	OTP Program Setup	Lock Setup	Read Array	
Lock Error	1	Read Array	Program Setup	Read Array	OTP Program Setup	Lock Setup	Read Array	

BLOCK LOCKING

The MT28F320A18 Flash memory provides a flexible locking scheme that allows each block to be individually locked or unlocked with no latency.

The device offers two-level protection for the blocks. The first level allows software-only control of block locking (for data that needs to be changed frequently), while the second level requires hardware interaction before locking can be changed (code that does not require frequent updates). Control pins WP#, DQ1, and DQ0 define the state of a block; for example, state [001] means WP# = 0, DQ1 = 0 and DQ0 = 1. Table 9 defines all of the possible locking states.

Note: All blocks are software-locked upon power-up sequence completion.

Locking operation

The following summarizes the locking operation.

1. All blocks are locked on power-up. They can then be unlocked or locked down with the UNLOCK and LOCK DOWN commands.
2. The LOCK DOWN command locks a block and prevents it from being unlocked when WP# = 0.
   - When WP# = 1, lock down is overridden. Commands can then unlock/lock locked down blocks.
   - When WP# returns to 0, locked down blocks return to lock down.
   - Lock down is cleared only when the device is reset or powered down.

Locked State

After a power-up sequence completion, or after a reset sequence, all blocks are locked (states [001] or [101]). This means full protection from alteration. Any PROGRAM or ERASE operations attempted on a locked block will return an error on bit SR1 of the status register. The status of a locked block can be changed to unlocked or lock down using the appropriate software commands. Writing the lock command sequence, 60h followed by 01h, can lock an unlocked block.

Unlocked State

Unlocked blocks (states [000], [100], [110]) can be programmed or erased. All unlocked blocks return to the locked state when the device is reset or powered down. An unlocked block can be locked or locked down using the appropriate software command sequence (see Table 4).

Locked Down State

Blocks that are locked down (state [011]) are protected from PROGRAM and ERASE operations, but their protection status cannot be changed using software commands alone. A locked or unlocked block can be locked down by writing the lock down command sequence, 60h followed by 2Fh. Locked down blocks revert to the locked state when the device is reset or powered down.

The lock down function is dependent on the WP# input pin. When WP# = 0, blocks in lock down [011] are protected from program, erase and lock status changes. When WP# = 1, the lock down function is disabled ([111]) and locked down blocks can be individually unlocked by a software command to the [110] state, where they can be erased and programmed. These blocks can then be relocked [111] and unlocked [110] as desired as long as WP# remains HIGH. When WP# goes LOW, blocks that were previously locked down return to the locked down state [011] regardless of any changes made while WP# was HIGH. Device reset or power-down resets all locked blocks, including those in lock down, to locked state (see Table 9).

Reading a Block's Lock Status

The lock status of every block can be read in the read device identification mode. To enter this mode, write 90h to the device. Subsequent READs at block address + 00002h will output the lock status of that block. The lowest two outputs, DQ0 and DQ1, represent the lock status. DQ0 indicates the block lock/unlock status and is set by the LOCK command and cleared by the UNLOCK command. It is also automatically set when entering lock down. DQ1 indicates lock down status and is set by the LOCK DOWN command. It can only be cleared by reset or power-down, not by software. Table 9 shows the locking state transition scheme.

Locking Operations during Erase Suspend

Changes to block lock status can be performed during an ERASE SUSPEND by using the standard locking command sequences to unlock, lock, or lock down. This is useful in the case when another block needs to be updated while an ERASE operation is in progress.

To change block locking during an ERASE operation, first write the ERASE SUSPEND command (B0h), then check the status register until it indicates that the ERASE operation has been suspended. Next, write the desired lock command sequence to block lock, and the

lock status will be changed. After completing LOCK, READ or PROGRAM operations, resume the ERASE operation with the ERASE RESUME command (D0h).

If a block is locked or locked down during a suspend erase of the same block, the locking status bits will change immediately. But, when resumed, the erase operation will complete.

A locking operation cannot be performed during a PROGRAM SUSPEND.

Status Register Error checking

Using nested locking or program command sequences during ERASE SUSPEND can introduce ambiguity into status register results.

Following protection configuration setup (60h), an invalid command will produce a lock command error (SR4 and SR5 will be set to "1") in the status register. If a lock command error occurs during an ERASE SUSPEND, SR4 and SR5 will be set to "1" and will remain at "1" after the ERASE SUSPEND is resumed. When the ERASE is complete, any possible error during the ERASE cannot be detected via the status register because of the previous locking command error.

A similar situation happens if an error occurs during a program operation error nested within an ERASE SUSPEND.

Table 7: Bus Operations

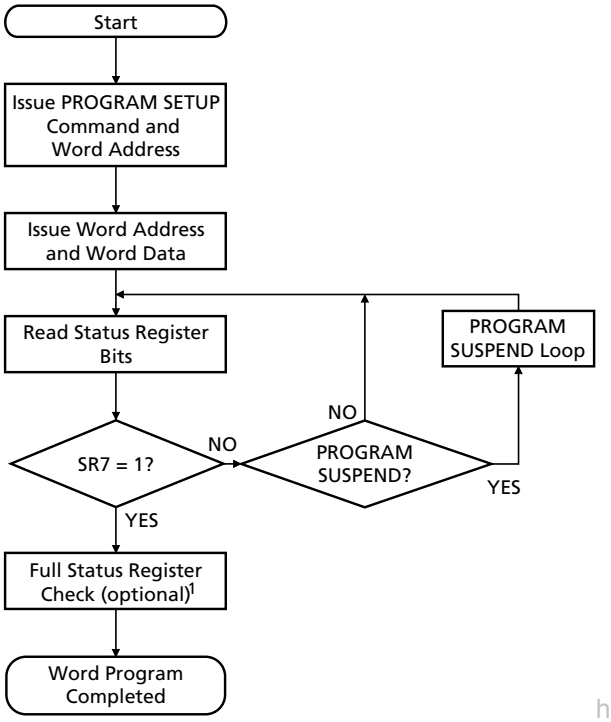
MODE	RP#	CE#	OE#	WE#	ADDRESS	DQ0–DQ15
Read (array, status registers, device identification register, or query)	VIH	VIL	VIL	VIH	X	DOUT
Standby	VIH	VIH	X	X	X	High-Z
Output Disable	VIH	VIL	VIH	X	X	High-Z
Reset	VIL	X	X	X	X	High-Z
Write	VIH	VIL	VIH	VIL	X	DIN

Table 8: Status Register Bit Definition

WSMS	ESS	ES	PS	VPPS	PSS	BLS	R
7	6	5	4	3	2	1	0

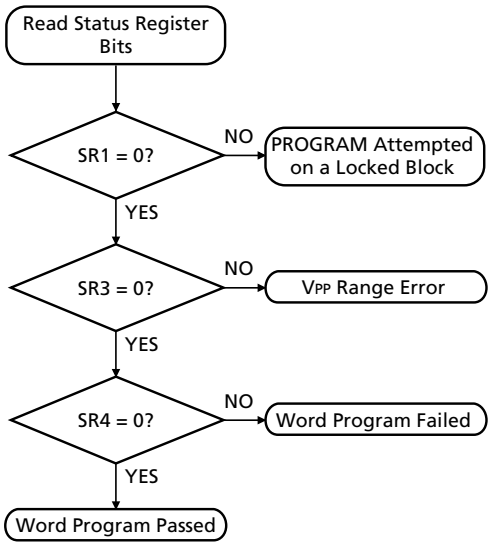
STATUS BIT #	STATUS REGISTER BIT	DESCRIPTION
SR7	WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy	Check write state machine bit first to determine word program or block erase completion, before checking program or erase status bits.
SR6	ERASE SUSPEND STATUS (ESS) 1 = BLOCK ERASE Suspended 0 = BLOCK ERASE in Progress/Completed	When ERASE SUSPEND is issued, WSM halts execution and sets both WSMS and ESS bits to "1." ESS bit remains set to "1" until an ERASE RESUME command is issued.
SR5	ERASE STATUS (ES) 1 = Error in Block Erasure 0 = Successful BLOCK ERASE	When this bit is set to "1," WSM has applied the maximum number of erase pulses to the block and is still unable to verify successful block erasure.
SR4	PROGRAM STATUS (PS) 1 = Error in PROGRAM 0 = Successful PROGRAM	When this bit is set to "1," WSM has attempted but failed to program a word.
SR3	VPP STATUS (VPPS) 1 = VPP Low Detect, Operation Abort 0 = VPP = OK	The VPP status bit does not provide continuous indication of the VPP level. The WSM interrogates the VPP level only after the program or erase command sequences have been entered. The WSM informs the system if VPP < 0.9V. The VPP level is also checked before the PROGRAM/ERASE operation is verified by the WSM.
SR2	PROGRAM SUSPEND STATUS (PSS) 1 = Program Suspended 0 = Program in Progress/Completed	When PROGRAM SUSPEND is issued, WSM halts execution and sets both WSMS and PSS bits to "1." PSS bit remains set to "1" until a PROGRAM RESUME command is issued.
SR1	BLOCK LOCK STATUS (BLS) 1 = PROGRAM/ERASE Attempted on a Locked Block; Operation Aborted 0 = No operation to locked blocks	If a PROGRAM or ERASE operation is attempted to one of the locked blocks, this is set by the WSM. The operation specified is aborted and the device is returned to read status mode.
SR0	RESERVED FOR FUTURE ENHANCEMENTS	This bit is reserved for future enhancements.

Figure 4: Automated Word Programming Flowchart



BUS OPERATION	COMMAND	COMMENTS
WRITE	WRITE PROGRAM SETUP	Data = 40h or 10h Addr = Address of word to be programmed
WRITE	WRITE DATA	Data = Word to be programmed Addr = Address of word to be programmed
READ		Status register data Toggle OE# or CE# to update status register.
Standby		Check SR7 1 = Ready, 0 = Busy
Repeat for subsequent words. Write FFh after the last word programming operation to return the device to read array mode.		

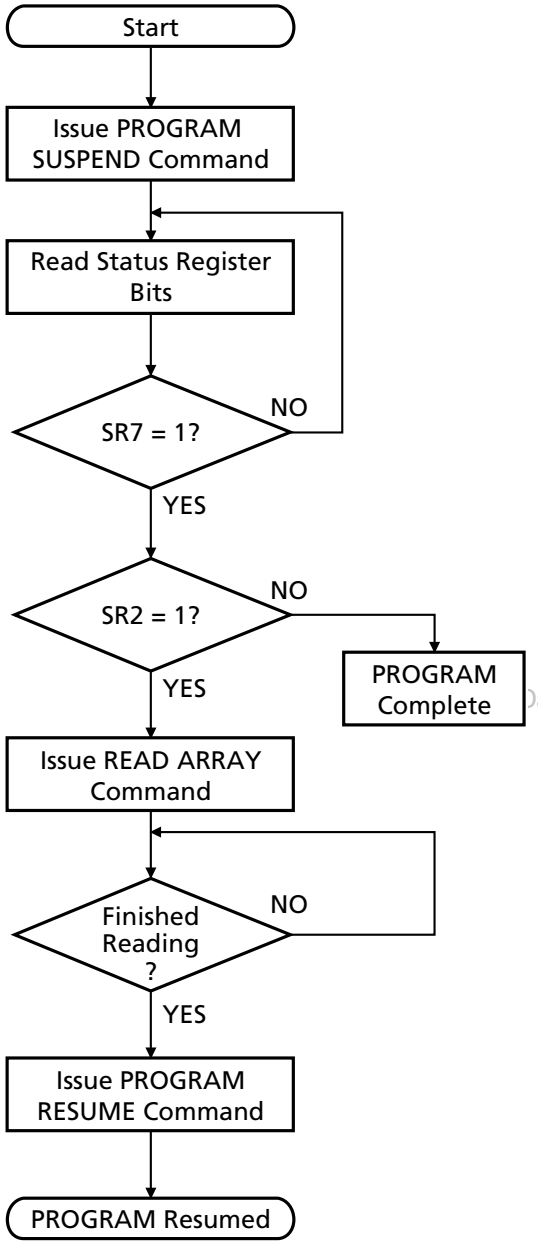
FULL STATUS REGISTER CHECK FLOW



BUS OPERATION	COMMAND	COMMENTS
Standby		Check SR1 1 = Detect locked block
Standby		Check SR3 1 = Detect VPP LOW
Standby		Check SR4[3] 1 = Word program error

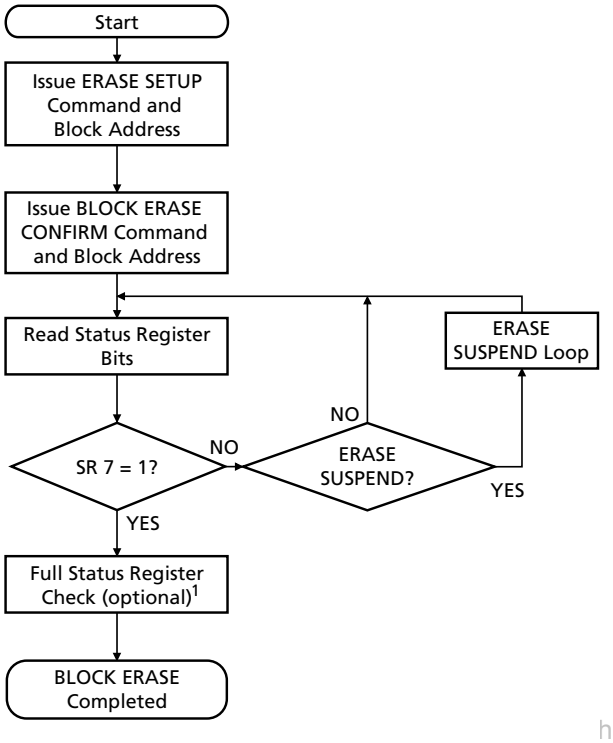
Notes: 1. Full status register check can be done after each word or after a sequence of words.
2. SR3 must be cleared before attempting additional PROGRAM/ERASE operations.
3. SR5 is cleared only by the CLEAR STATUS REGISTER command in cases where multiple blocks are erased before full status is checked.

Figure 5: PROGRAM SUSPEND/ PROGRAM RESUME Flowchart



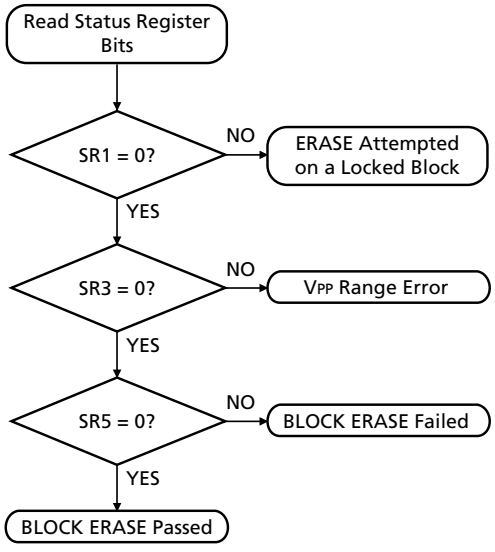
BUS OPERATION	COMMAND	COMMENTS
WRITE	PROGRAM SUSPEND	Data = B0h
READ		Status register data Toggle OE# or CE# to update status register.
Standby		Check SR7 1 = Ready
Standby		Check SR2 1 = Suspended
WRITE	READ MEMORY	Data = FFh
READ		Read data from block other than that being programmed.
WRITE	PROGRAM RESUME	Data = D0h

Figure 6: BLOCK ERASE Flowchart



BUS OPERATION	COMMAND	COMMENTS
WRITE	WRITE ERASE SETUP	Data = 20h Block Addr = Address within block to be erased
WRITE	ERASE	Data = D0h Block Addr = Address within block to be erased
READ		Status register data Toggle OE# or CE# to update status register.
Standby		Check SR7 1 = Ready, 0 = Busy
Repeat for subsequent blocks. Write FFh after the last BLOCK ERASE operation to return the device to read array mode.		

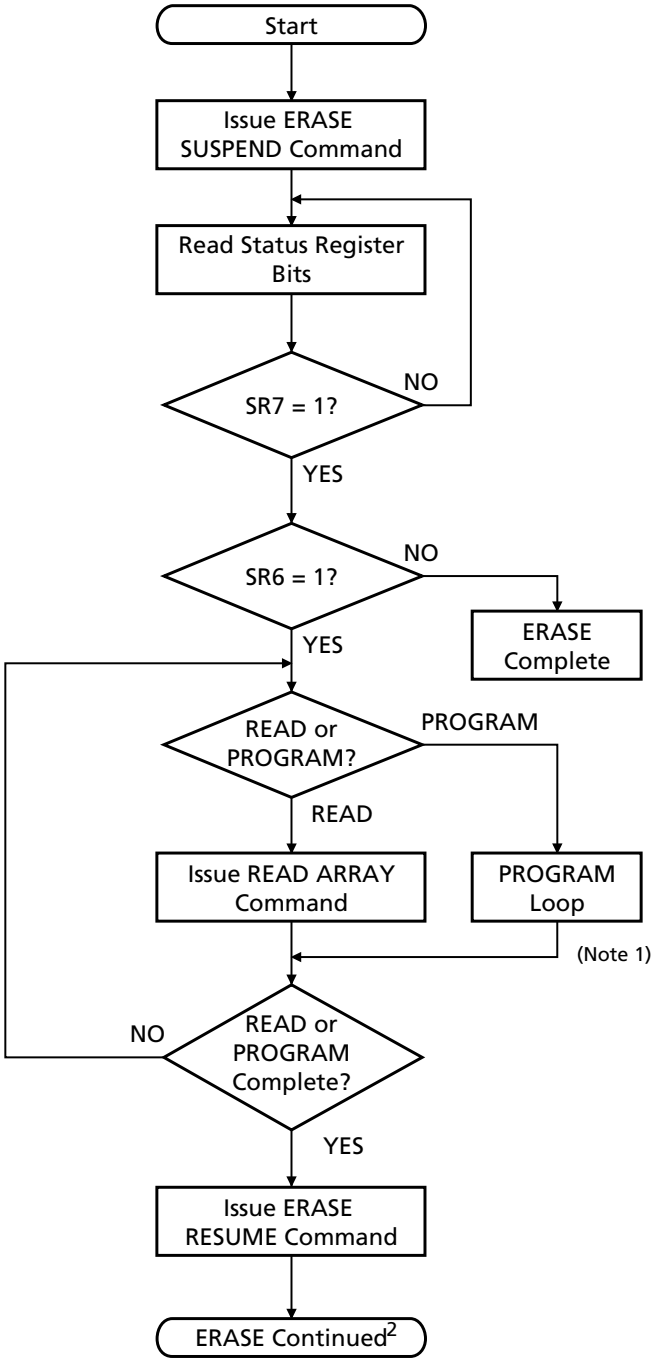
FULL STATUS REGISTER CHECK FLOW



BUS OPERATION	COMMAND	COMMENTS
Standby		Check SR1 1 = Detect locked block
Standby		Check SR3[2] 1 = Detect Vpp block
Standby		Check SR4 and SR5 1 = Block erase command error
Standby		Check SR5[3] 1 = Block erase error

Notes: **1.** Full status register check can be done after each block or after a sequence of blocks.
2. SR3 must be cleared before attempting additional PROGRAM/ERASE operations.
3. SR5 is cleared only by the CLEAR STATUS REGISTER command in cases where multiple blocks are erased before full status is checked.

Figure 7: ERASE SUSPEND/ERASE RESUME Flowchart



BUS OPERATION	COMMAND	COMMENTS
Write	ERASE SUSPEND	Data = B0h
READ		Status register data Toggle OE# or CE# to update status register.
Standby		Check SR7 1 = Ready
Standby		Check SR6 1 = Suspended
WRITE	READ MEMORY	Data = FFh
READ		Read data from block other than that being erased.
WRITE	ERASE RESUME	Data = D0h

Notes: **1.** See Word Programming Flowchart for complete programming procedure.
2. See BLOCK ERASE Flowchart for complete erasure procedure.

Table 9: Block Locking State Transition

WP#	DQ1	DQ0	NAME	ERASE/ PROGRAM ALLOWED	LOCK	UNLOCK	LOCK DOWN
0	0	0	Unlocked	Yes	To [001]	No Change	To [011]
0	0	1	Locked (Default)	No	No Change	To [000]	To [011]
0	1	1	Lock down	No	No Change	No Change	No Change
1	0	0	Unlocked	Yes	To [101]	No Change	To [111]
1	0	1	Locked	No	No Change	To [100]	To [111]
1	1	0	Lock down disabled	Yes	To [111]	No Change	To [111]
1	1	1	Lock down disabled	No	No Change	To [110]	No Change
0	1	0	Invalid	No	No Change	No Change	No Change

Table 10: Chip Configuration Addressing[1]

ITEM	ADDRESS[2]	DATA
Manufacturer Code (x16)	000000h	002Ch
Device Code	000001h	32Mb
Top boot configuration		00C2h
Bottom boot configuration		00C3h
Block Lock Configuration Block is unlocked Block is locked Block is locked down	BA + 000002h	Lock DQ0 = 0 DQ0 = 1 DQ1 = 1
Chip Protection Register Lock	80h	PR-Lock DQ1 = 0 locked DQ1 = 1 unlocked
Chip Protection Register 1	81h–84h	Factory Data
Chip Protection Register 2	85h–88h	User Data

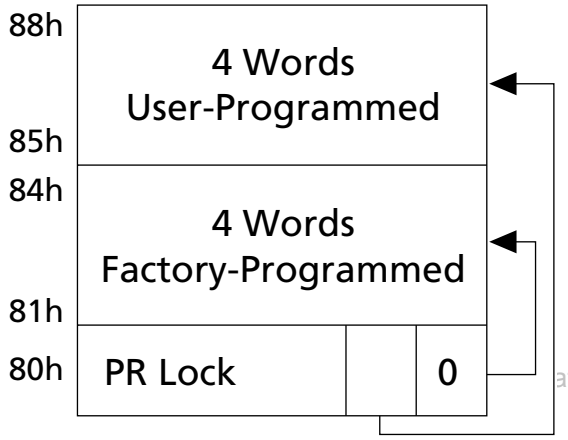
Notes: 1. Other locations within the configuration address space are reserved by Micron for future use.
2. "XX" specifies the block address of lock configuration.

CHIP PROTECTION REGISTER

A 128-bit protection register can be used to fulfill the security considerations in the system (preventing the device substitution).

The 128-bit security area is divided into two 64-bit segments. The first 64 bits are programmed at the manufacturing site with a unique 64-bit unchangeable number. The other segment is left blank for customers to program as desired. (See Figure 8).

Figure 8:
Protection Register Memory Map



Reading the Chip Protection Register

The chip protection register is read in the device identification mode, loading the 90h command to the bank containing address 00h. Once in this mode, READ cycles from addresses shown in Table 10 retrieve the specified information. To return to the read array mode, write the READ ARRAY command (FFh).

Programming the Chip Protection Register

Executing the PROTECTION PROGRAM command enables the customer to program the user portion of the protection register. First, write the PROTECTION PROGRAM SETUP command, C0h; then write address and data to program.

Attempts should not be made to address PROTECTION PROGRAM commands outside the defined protection register address space. Attempting to program to a previously locked protection register segment will result in a status register error (program error bit SR4 and lock error bit SR1 = 1)

Locking the Chip Protection Register

The customer-programmable segment of the protection register can be locked by programming bit 1 of the PR lock location to "0". Bit 0 of this location is programmed to a “0” at the Micron factory to protect the unique device number. Bit 1 is set using the PROTECTION PROGRAM command to program FFFDh to the PR lock location. After these bits have been programmed, no further changes can be made to the values stored in the protection register. PROTECTION PROGRAM commands to a locked section will result in a status register error program error bit SR4 and lock error bit SR1 will be set to 1. Protection register lockout is not reversible.

VPP/VCC Program and Erase Voltages

The MT28F320A18 Flash memory provides in-system programming and erase with VPP in the 0.9V–1.95V (VPP1) range. The 12V VPP (VPP2) mode programming is offered for compatibility with existing programming equipment. The fast programming algorithm is enabled at VPP = VPP2.

The device can withstand 100,000 WRITE/ERASE operations when VPP = VPP1 or 100 WRITE/ERASE operations and 10 cumulative hours when VPP = VPP2.

In addition to the flexible block locking, the VPP programming voltage can be held LOW for absolute hardware write protection of all blocks in the Flash device. When VPP is below VPPLK, any PROGRAM or ERASE operation will result in an error, prompting the corresponding status register bit (SR3) to be set.

During WRITE and ERASE operations, the WSM monitors the VPP voltage level. WRITE/ERASE operations are allowed only when VPP is within the range specified in TABLE 11.

When VCC is below VLKO or below VPPLK, any WRITE/ERASE operation will be disabled.

Table 11: VPP Range (V)

	MIN	MAX
In-System (VPP1)	0.9	1.95
In-Factory (VPP2)	11.4	12.6

READ CYCLE

Addresses can be accessed in a random order with an access time given by ^{t}AA = 70ns.

When CE# and OE# are LOW, the data is placed on the data bus and the processor can read the data.

STANDBY MODE

ICC supply current is reduced by applying a logic HIGH level on CE# and RP# to enter the standby mode. In the standby mode, the outputs are placed in High-Z. Applying a CMOS logic HIGH level on CE# and RP# reduces the current to ICC2 (MAX). If the device is deselected during an ERASE operation or during programming, the device continues to draw current until the operation is complete.

AUTOMATIC POWER SAVE MODE (APS)

Substantial power savings are realized during periods when the array is not being read and the device is in the active mode. During this time, the device switches to the automatic power saving mode. When the device switches to this mode, ICC is reduced to ICC2. The low level of power is maintained until another operation is initiated. In this mode, the I/O pins retain the data from the last memory address read until a new address is initiated. This mode is entered automatically if no address or control signal toggles.

POWER-UP SEQUENCE

The following power-up sequence is recommended to properly initialize internal chip operations:

- At power-up, RST# should be kept at VIL for 2µs after VCC reaches VCC (MIN).
- VccQ should not come up before Vcc.
- VPP should be kept at VIL to maximize data integrity.

When the power-up sequence is completed, RST# should be brought to VIH. To ensure proper power-up, the rise time of RST# (10%–90%) should be < 10µs.

ABSOLUTE MAXIMUM RATINGS*

Voltage to Any Ball Except Vcc and Vpp with Respect to Vss ..... -0.5V to +2.45V
Vpp Voltage (for BLOCK ERASE and PROGRAM with Respect to Vss) ..... -0.5V to +13.5V
Vcc and VccQ Supply Voltage with Respect to Vss ..... -0.3V to +2.45V
Output Short Circuit Current 100mA
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -55°C to +125°C
Soldering Cycle ..... 260°C for 10s

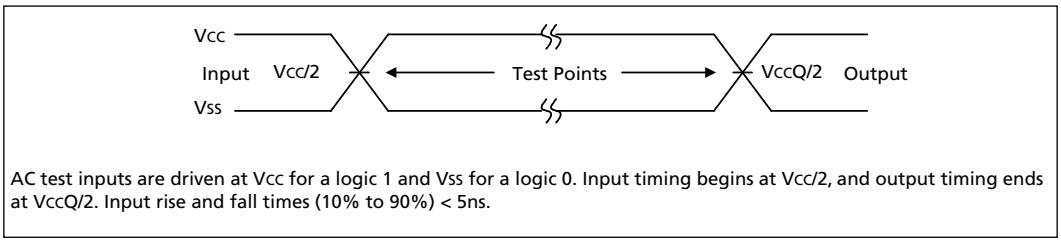
*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Operating temperature		^{t}A	-40	+85	°C	
Vcc supply voltage		Vcc	1.65	1.95	V	
I/O supply voltage (Vcc = 1.65V–1.95V)		VccQ1	1.65	1.95	V	
Supply voltage, when used as logic control		VPP1	0.9	1.95	V	
VPP in-factory programming voltage		VPP2	11.4	12.6	V	
Block erase cycling	VPP = VPP1	VPP1	100,000	–	Cycles	
	VPP = VPP2	VPP2	–	100	Cycles	1

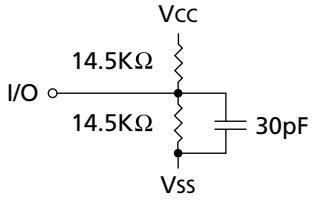
Notes: 1. VPP = VPP2 is a maximum of 10 cumulative hours.

Figure 9: AC Input/Output Reference Waveform



AC test inputs are driven at Vcc for a logic 1 and Vss for a logic 0. Input timing begins at Vcc/2, and output timing ends at VccQ/2. Input rise and fall times (10% to 90%) < 5ns.

Figure 10: Output Load Circuit



DC CHARACTERISTICS

PARAMETER	SYMBOL	Vcc = 1.65V–1.95V VccQ = 1.65V–1.95V			UNIT
		MIN	TYP	MAX	
Input Low Voltage	V_{IL}	-0.2	–	0.2	V
Input High Voltage	V_{IH}	VccQ - 0.2	–	VccQ + 0.2	V
Output Low Voltage I_{OL} = 100µA	V_{OL}	–	–	0.1	V
Output High Voltage I_{OH} = 100µA	V_{OH}	VccQ - 0.1	–	–	V
V_{PP} Lock Out Voltage	V_{PPLK}	–	–	0.4	V
V_{PP} During Program/Erase Operations	V_{PP1}	0.9	–	1.95	V
	V_{PP2}	11.4	–	12.6	V
V_{CC} Program/Erase Lock Voltage	V_{LKO}	1	–	–	V
Input Leakage Current	I_L	-1	–	1	µA
Output Leakage Current	I_{OZ}	-1	–	1	µA
V_{CC} Read Current, 70ns cycle[1,2]	I_{CC1}	–	9	18	mA
V_{CC} Standby Current[3]	I_{CC2}	–	15	50	µA
Program Current $V_{PP} = V_{PP1}$ $V_{PP} = V_{PP2}$	I_{CC3}	 – –	 25 12	 40 40	 mA mA
Erase Current $V_{PP} = V_{PP1}$ $V_{PP} = V_{PP2}$	I_{CC4}	 – –	 25 25	 40 40	 mA mA
V_{CC} Erase Suspend Current $V_{PP} = V_{PP1}$	I_{CC5}	–	5	85	µA
V_{CC} Program Suspend Current $V_{PP} = V_{PP1}$	I_{CC6}	–	5	85	µA
V_{PP} Read Current $V_{PP} \leq V_{CC}$	I_{PP1}	–	0.5	15	µA
V_{PP} Standby Current $V_{PP} = V_{PP1}$	I_{PP2}	–	0.5	5	µA
V_{PP} Erase Suspend Current $V_{PP} = V_{PP1}$	I_{PP5}	–	0.5	5	µA
V_{PP} Program Suspend Current $V_{PP} = V_{PP1}$	I_{PP6}	–	0.5	5	µA

Notes: **1.** Test conditions are V_{CC} = V_{CC} (MAX), CE# = V_{IL}, OE# = V_{IH}; all other inputs at V_{IH} or V_{IL}.
2. APS mode reduces I_{CC} to approximately I_{CC2} levels.
3. RP# = V_{IH} or V_{IL}.

READ CYCLE TIMING REQUIREMENTS[1]

PARAMETER	SYMBOL	-70 Vcc = 1.65V–1.95V MIN	-70 Vcc = 1.65V–1.95V MAX	UNITS
Address to output delay	^tAA		70	ns
CE# LOW to output delay	^tACE		70	ns
OE# LOW to output delay	^tAOE		20	ns
RP# HIGH to output delay	^tRWH		150	ns
CE# or OE# HIGH to output High-Z	^tOD		15	ns
Output hold from address, CE#, or OE# change	^tOH	0		ns
READ cycle time	^tRC	70		ns
OE# LOW to valid status register data	^tSRD		25	ns

Notes: 1. See Figures 11 and 12 for timing requirements and output load configuration.

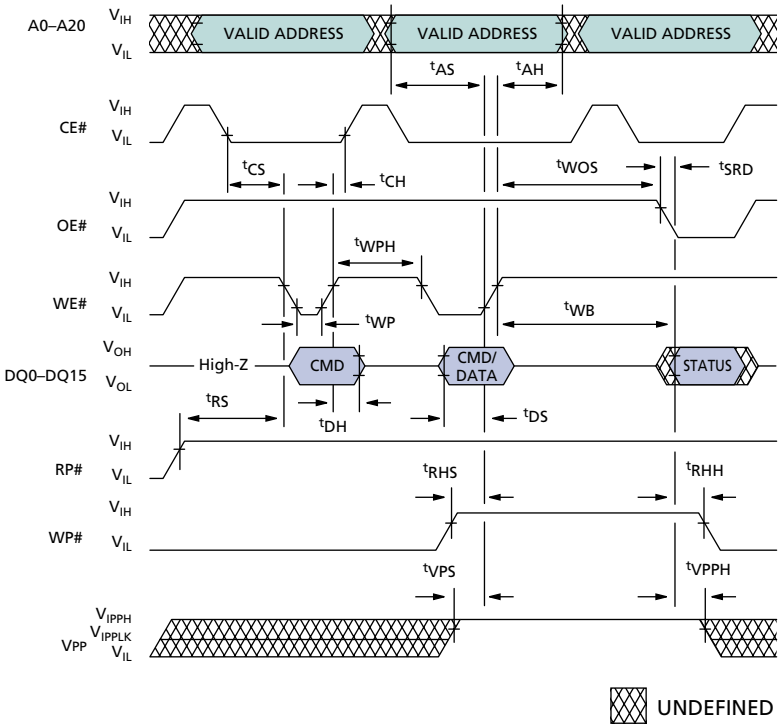
WRITE CYCLE TIMING REQUIREMENTS

PARAMETER	SYMBOL	-70 Vcc = 1.65V–1.95V MIN	-70 Vcc = 1.65V–1.95V MAX	UNITS
RP# HIGH recovery to WE# going LOW	^tRS	150		ns
CE# setup to WE# going LOW	^tCS	0		ns
Write pulse width	^tWP	70		ns
Data setup to WE# going HIGH	^tDS	70		ns
Address setup to WE# going HIGH	^tAS	70		ns
CE# hold from WE# HIGH	^tCH	0		ns
Data hold from WE# HIGH	^tDH	0		ns
Address hold from WE# HIGH	^tAH	0		ns
Write pulse width HIGH	^tWPH	30		ns
RP# pulse width	^tRP	100		ns
WP# setup to WE# going HIGH	^tRHS	200		ns
V_{PP} setup to WE# going HIGH	^tVPS	200		ns
Write recovery before READ	^tWOS	50		ns
WP# hold from valid SRD	^tRHH	0		ns
V_{PP} hold from valid SRD	^tVPPH	0		ns
WE# HIGH to data valid	^tWB		^tAA+50	ns

ERASE AND PROGRAM CYCLE TIMING REQUIREMENTS

PARAMETER	SYMBOL	V_{PP} = 1.65V–1.95V, V_{CC} = 1.65V–1.95V		V_{PP} = 12V ±5%, V_{CC} = 1.65V–1.95V		UNITS
		TYP	MAX	TYP	MAX	
4KW block program time	$^{t}BWPB$	0.1	0.3			s
32KW block program time	$^{t}BWMB$	0.8	2.4			s
Word program time	$^{t}WHQV1/^{t}EHQV1$	8	150	5	130	µs
4KW block erase time	$^{t}WHQV2/^{t}EHQV2$	0.3	2.5	0.03	2.5	s
32KW block erase time	$^{t}WHQV3/^{t}EHQV3$	1	4	0.3	4	s
Program suspend latency	$^{t}WHRH1/^{t}EHRH1$	2.5	5			µs
Erase suspend latency	$^{t}WHRH2/^{t}EHRH2$	2.5	5			µs

Two-Cycle Programming/ERASE Operation



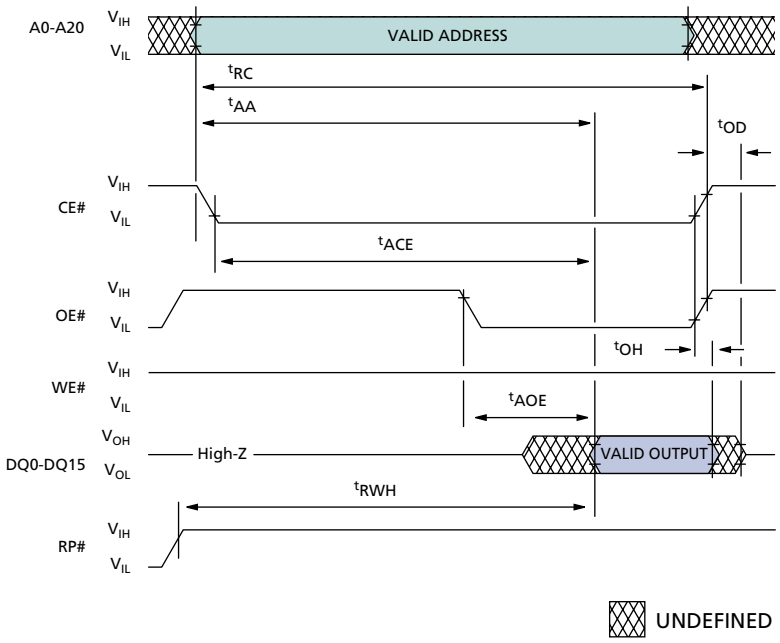
WRITE TIMING PARAMETERS

SYMBOL	-70 Vcc = 1.65V–1.95V MIN	MAX	UNITS
t_{RS}	150		ns
t_{CS}	0		ns
t_{WP}	70		ns
t_{DS}	70		ns
t_{AS}	70		ns
t_{CH}	0		ns
t_{DH}	0		ns
t_{AH}	0		ns

SYMBOL	-70 Vcc = 1.65V–1.95V MIN	MAX	UNITS
t_{WPH}	30		ns
t_{RHS}	200		ns
t_{VPS}	200		ns
t_{WOS}	50		ns
t_{RHH}	0		ns
t_{VPPH}	0		ns
t_{WB}		t_{AA}+50	ns
t_{SRD}		25	ns

Notes: 1. The WRITE cycles for the WORD PROGRAMMING command are followed by a READ ARRAY DATA cycle.

Single Asynchronous READ Operation

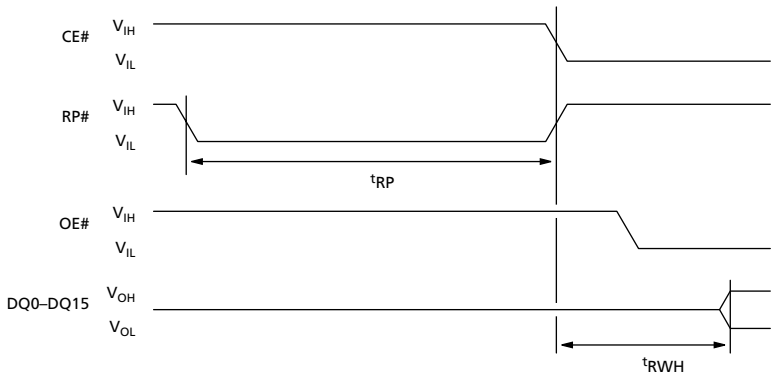


READ TIMING PARAMETERS

SYMBOL	-70 Vcc = 1.65V–1.95V MIN	-70 Vcc = 1.65V–1.95V MAX	UNITS
t_{AA}		70	ns
t_{ACE}		70	ns
t_{AOE}		20	ns
t_{RWH}		150	ns

SYMBOL	-70 Vcc = 1.65V–1.95V MIN	-70 Vcc = 1.65V–1.95V MAX	UNITS
t_{RC}		70	ns
t_{OD}		15	ns
t_{OH}	0		ns

Reset Operation



READ AND WRITE TIMING PARAMETERS

SYMBOL	-70 Vcc = 1.65V–1.95V MIN	-70 Vcc = 1.65V–1.95V MAX	UNITS
t_{RWH}		150	ns
t_{RP}	100		ns

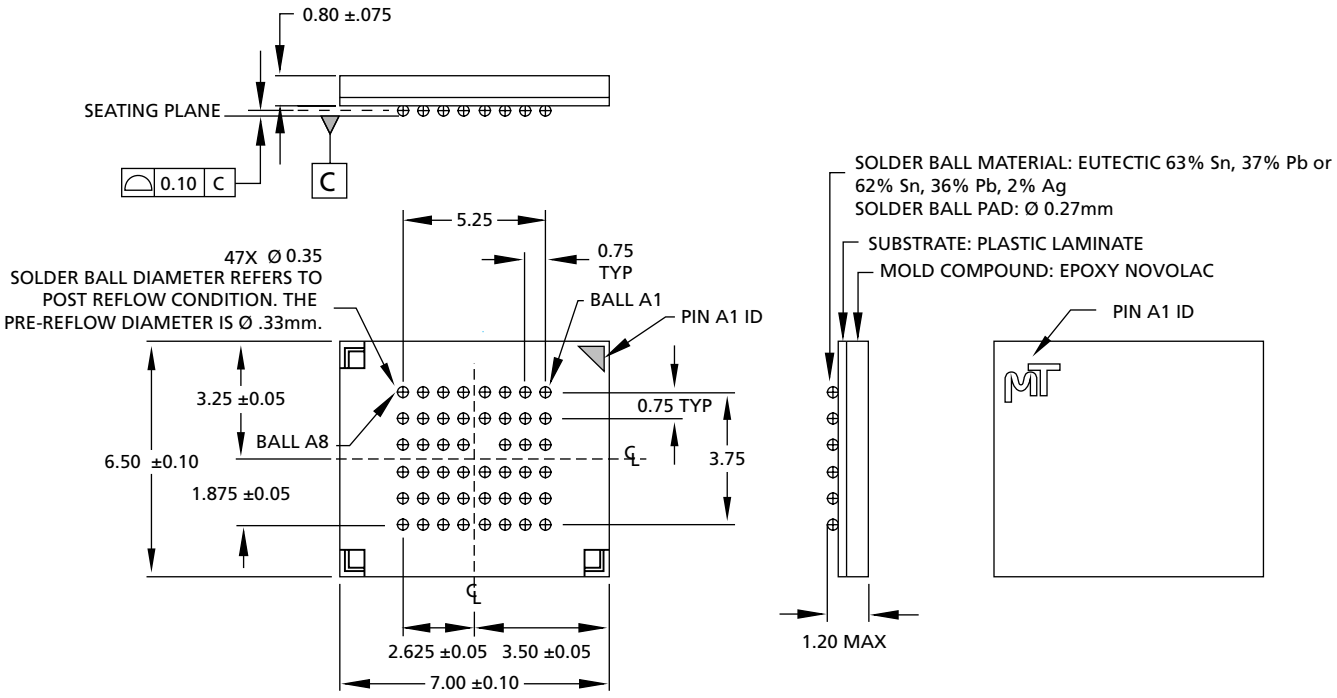
Table 12: CFI

OFFSET	DATA	DESCRIPTION
00	2Ch	Manufacturer Code
01	C2h/C3h	32Mb Top /Bottom Boot Block Device Code
03 - 0F	reserved	Reserved
10, 11	0051, 0052	"QR"
12	0059	"Y"
13, 14	0003, 0000	Primary OEM Command Set
15, 16	0035, 0000	Address for Primary Extended Table
17, 18	0000, 0000	Alternate OEM Command Set
19, 1A	0000, 0000	Address for OEM Extended Table
1B	0017	V_{CC} MIN for Erase/Write; Bit7–Bit4 Volts in BCD; Bit3–Bit0 100mV in BCD
1C	0019	V_{CC} MAX for Erase/Write; Bit7–Bit4 Volts in BCD; Bit3–Bit0 100mV in BCD
1D	00B4	V_{PP} MIN for Erase/Write; Bit7–Bit4 Volts in Hex; Bit3–Bit0 100mV in BCD, 0000 = V_{PP} input
1E	00C6	V_{PP} MAX for Erase/Write; Bit7–Bit4 Volts in Hex; Bit3–Bit0 100mV in BCD, 0000 = V_{PP} input
1F	0003	Typical timeout for single byte/word program, 2^n µs, 0000 = not supported
20	0000	Typical timeout for maximum size multiple byte/word program, 2^n µs, 0000 = not supported
21	0009	Typical timeout for individual block erase, 2^n ms, 0000 = not supported
22	0000	Typical timeout for full chip erase, 2^n ms, 0000 = not supported
23	000C	Maximum timeout for single byte/word program, 2^n µs, 0000 = not supported
24	0000	Maximum timeout for maximum size multiple byte/word program, 2^n µs, 0000 = not supported
25	000C	Maximum timeout for individual block erase, 2^n ms, 0000 = not supported
26	0000	Maximum timeout for full chip erase, 2^n ms, 0000 = not supported
27	0016	Device size, 2^n bytes; 0016 for 32Mb
28	0001	Bus Interface x8 = 0, x16 = 1, x8/x16 = 2
29	0000	Flash device interface description 0000 = async
2A, 2B	0000, 0000	Maximum number of bytes in multi-byte program or page, 2^n
2C	0002	Number of erase block regions within device (4K words and 32K words)
2D, 2E	0007, 0000	Erase block region information 1, 8 blocks ...
2F, 30	0020, 0000	...of 8KB
31, 32	001E, 0000	63 = 3Eh for 32Mb
33, 34	0000, 0001	...64KB
35, 36	0050, 0052	"PR"
37	0049	"I"
38	0030	Major Version number ASCII
39	0031	Minor version number, ASCII
3A 3B 3C 3D	0066 0000 0000 0000	Optional Feature and Command Support Bit 0 Chip erase supported no = 0 Bit 1 Suspend erase supported = yes = 1 Bit 2 Suspend program supported = yes = 1 Bit 3 Chip lock/unlock supported = no = 0 Bit 4 Queued erase supported = no = 0 Bit 5 Instant individual block locking supported = yes = 1 Bit 6 Protection bits supported = yes = 1 Bit 7 Page mode read supported = no = 0 Bit 8 Synchronous read supported = no = 0 Bit 9 Simultaneous operation supported = no = 0

Table 12: CFI (continued)

OFFSET	DATA	DESCRIPTION
3E	0001	Program supported after erase suspend = yes
3F, 40	0003, 0000	Bit 0 block lock status active = yes Bit 1 block lock down active = yes
41	0018	VCC supply optimum, 00 = not supported, Bit7–Bit4 Volts in BCD; Bit3–Bit0 100mV in BCD
42	00C0	VPP supply optimum, 00 = not supported, Bit7–Bit4 Volts in BCD; Bit3–Bit0 100mV in BCD
43	0001	Number of protection register fields in JEDEC ID space
44, 45	0080, 0000	Lock bytes LOW address, lock bytes HIGH address
46, 47	0003, 0003	2^n factory programmed bytes, 2^n user programmable bytes
48	0000	Background Operation 0000 = Not used 0001 = 4% block split 0002 = 12% block split 0003 = 25% block split 00004 = 50% block split
49	0000	Burst Mode Type 0000 = No burst mode 00x1 = 4 words max 00x2 = 8 words max 00x13 = 16 words max 001x = Linear burst, and/or 002x = Interleaved burst, and/or 004x = Continuous burst
4A	0000	Page Mode Type 0000 = No page mode 0001 = 4-word page 0002 = 8-word page 0003 = 16-word page 0004 = 32-word page
4B	0000	Not used

47-BALL FBGA



Notes: 1. All dimensions in millimeters.
2. Micron recommends a one-to-one ratio between the solder ball pad and the PCB. For more information, see Micron Technical Note, TN-00-11, "SMT Recommendations for BGA Assembly."

DATA SHEET DESIGNATIONS

No Marking: This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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REVISION HISTORY

Rev. F, PRODUCTION 9/03

- Added ^{t}SRD timing

Rev. E, PRODUCTION 3/03

- Update DC Characteristics values
- Icc5 from 50µA to 85µA
- Icc6 from 50µA to 85µA

Rev. 4, PRODUCTION 2/03

Rev. 3, PRELIMINARY 11/02

- Replaced mechanical drawing with correct version

Rev. 3, PRELIMINARY 9/02

- Updated Status Register section
- Updated Clear Status Register section
- Updated Read Array section
- Updated descriptions for command codes 20h, 70h, and D0h
- Updated Read Status Register section
- Removed ^{t}CBPH specification
- Removed 16Mb information

Rev. 2, ADVANCE 2/02

- Added reset pulse width information

Original document, Rev. 1, Advance 10/01