A2111
Preliminary Product Brief

Skyhawk

10 Gigabit Ethernet LAN/WAN PHY

Overview

The Skyhawk is a highly integrated, ultra-low-power frame processing solution for 10 Gigabit Ethernet (10 GbE) physical layer applications. The device provides complete PCS-R, PCS-W, and WIS functionality and can operate as a 10 GbE LAN or WAN PHY.

In 10 GbE WAN PHY mode, the line-side supports a standard 16-bit, 622.08 MHz XSBI / SFI-4 interface. In 10 GbE LAN PHY mode, the line-side supports a standard 16-bit, 644.53 MHz XSBI interface. The system-side interface is a selectable standard HSTL XGMII or SSTL-2 XGMII interface.

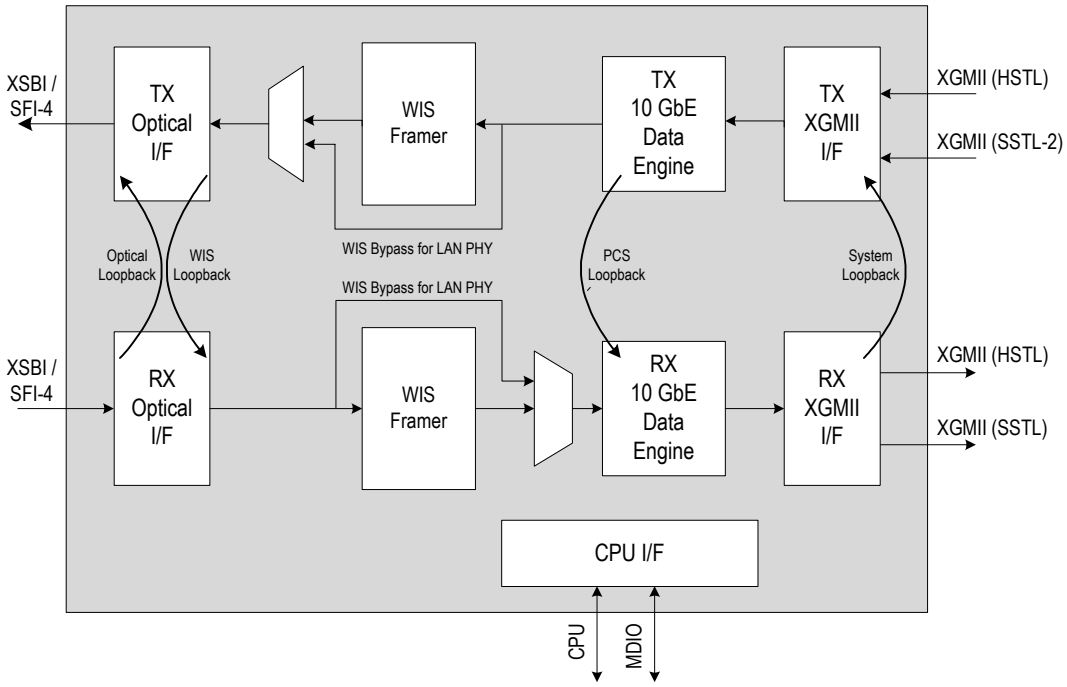
PCS layer functions include 64b/66b encoding and decoding, X^{58} scrambling and descrambling, gear boxing, and rate matching. Block-lock detection and remote and local fault handling are also supported.

WIS functions include WIS framing, pointer processing, and X^7 scrambling and descrambling, as well as error rate monitoring and alarm processing per ANSI T1-416 – 1999.

For device control and configuration, the Skyhawk provides a standard 32-bit processor interface, as well as a Management Data I/O (MDIO) interface and MDIO registers. The device conforms to the IEEE serial LAN-PHY and WAN-PHY proposals.

A key application for the device is to facilitate cost-effective interfacing between standard 10 Gbps optical modules with XSBI interfaces and link layer devices with XGMII interfaces. Other applications include optical core routers, enterprise switches, and Ethernet line terminating equipment.

Block Diagram



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7/8/02

Features

WIS Layer Processing

- Support for all WIS framing and frame synchronization functions
- Complete section, line, and path overhead layer termination
- Generation and verification of BIP-8 parity
- Pointer processing for receive payload extraction and transmit payload mapping
- Extraction and insertion of transport and path overhead from/to dedicated external pins or from registers
- WIS alarm insertion and detection
- Frame-synchronous $X^7 + X^6 + 1$ scrambling and descrambling
- Error rate monitoring

10 GbE Processing

- 10 GbE WAN and LAN PHY functionality
- Complete PCS-R and PCS-W functionality including:
  - 64b/66b encoding and decoding
  - $X^{58} + X^{39} + 1$ scrambling and descrambling
  - 66:16 gearboxing
  - Block synchronization
  - Rate matching
  - Block_lock detection
  - Remote and local fault handling

Line-Side Interface

- Support for two configurations
  - Standard XSBI (SFI-4) 16-bit, 622.08 MHz, LVDS interface for 10 GbE WAN PHY mode
  - Standard XSBI 16-bit, 644.53 MHz, LVDS interface for 10 GbE LAN PHY mode

System-Side Interfaces

- Selectable XGMII interface: HSTL2 or SSTL

CPU Interface

- 32-bit synchronous CPU interface; support for both Intel and Motorola-type processors
- MDIO and MDC management interface and registers

Test and Diagnostic Support

- Built-in pattern generators and verifiers
- Multiple diagnostic loopbacks
- IEEE 1149.1 port with memory BIST, scan, and JTAG boundary scan

General Specifications

- Packaging: 672-pin flip-chip BGA
- Technology: low-power CMOS 1.8V, 3.3V-tolerant I/Os on CPU and other interfaces
- Ambient operating temperature: 0°C to 70°C
- Power dissipation: 3.5 W max, 2.7 W typical

Standards Compliance

- IEEE 802.3ae-D3.1 draft specification
- ANSI T1.416 – 1999

Applications

- 10 GbE LAN or WAN switching equipment
- 10 GbE WAN or LAN PHYs
- Ethernet line-terminating equipment (ELTE)
- Edge and core routers
- Multiservice switches
- Uplink cards
- 10 GbE test equipment

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