

OBSOLETE

MICRON
TECHNOLOGY, INC.
**2, 4 MEG x 72
 NONBUFFERED DRAM DIMMs**

DRAM MODULE

MT9LD272A(X), MT18LD472A(X)

 For the latest data sheet revisions, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- JEDEC-standard, eight-CAS#, ECC pinout in a 168-pin, dual in-line memory module (DIMM)
- 16MB (2 Meg x 72) and 32MB (4 Meg x 72)
- Nonbuffered
- High-performance CMOS silicon-gate process
- Single +3.3V $\pm 0.3V$ power supply
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS#-ONLY, CAS#-BEFORE-RAS# (CBR) and HIDDEN
- 2,048-cycle refresh distributed across 32ms
- FAST-PAGE-MODE (FPM) or Extended Data-Out (EDO) PAGE MODE access cycles
- Serial presence-detect (SPD)

OPTIONS

- Package
168-pin DIMM (gold)
- Timing
50ns access
60ns access
- Access Cycles
FAST PAGE MODE
EDO PAGE MODE

MARKING

G

-5*

-6

None

X

*EDO version only

KEY TIMING PARAMETERS

EDO Operating Mode

SPEED	t _{RC}	t _{RAC}	t _{PC}	t _{AA}	t _{CAC}	t _{CAS}
-5	84ns	50ns	20ns	25ns	13ns	8ns
-6	104ns	60ns	25ns	30ns	15ns	10ns

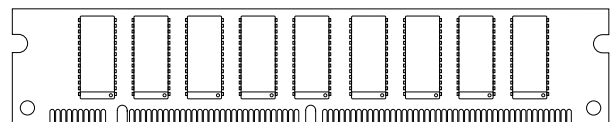
FPM Operating Mode

SPEED	t _{RC}	t _{RAC}	t _{PC}	t _{AA}	t _{CAC}	t _{RP}
-6	110ns	60ns	35ns	30ns	15ns	40ns

NOTE: Pin symbols in parentheses are not used on these modules but may be used for other modules in this product family. They are for reference only.

PIN ASSIGNMENT (Front View)

168-Pin DIMM



PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	V _{SS}	43	V _{SS}	85	V _{SS}	127	V _{SS}
2	DQ0	44	OE2#	86	DQ32	128	RFU
3	DQ1	45	RAS2#	87	DQ33	129	NC/RAS3#*
4	DQ2	46	CAS2#	88	DQ34	130	CAS6#
5	DQ3	47	CAS3#	89	DQ35	131	CAS7#
6	V _{DD}	48	WE2#	90	V _{DD}	132	RFU
7	DQ4	49	V _{DD}	91	DQ36	133	V _{DD}
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	V _{SS}	54	V _{SS}	96	V _{SS}	138	V _{SS}
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V _{DD}	101	DQ45	143	V _{DD}
18	V _{DD}	60	DQ20	102	V _{DD}	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	RFU	104	DQ47	146	RFU
21	CB0	63	NC	105	CB4	147	NC
22	CB1	64	V _{SS}	106	CB5	148	V _{SS}
23	V _{SS}	65	DQ21	107	V _{SS}	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	V _{DD}	68	V _{SS}	110	V _{DD}	152	V _{SS}
27	WE0#	69	DQ24	111	RFU	153	DQ56
28	CAS0#	70	DQ25	112	CAS4#	154	DQ57
29	CAS1#	71	DQ26	113	CAS5#	155	DQ58
30	RAS0#	72	DQ27	114	NC	156	DQ59
31	OE0#	73	V _{DD}	115	RFU	157	V _{DD}
32	V _{SS}	74	DQ28	116	V _{SS}	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V _{SS}	120	A7	162	V _{SS}
37	A8	79	NC	121	A9	163	NC
38	A10	80	NC	122	NC (A11)	164	NC
39	NC (A12)	81	NC	123	NC (A13)	165	SA0
40	V _{DD}	82	SDA	124	V _{DD}	166	SA1
41	V _{DD}	83	SCL	125	RFU	167	SA2
42	RFU	84	V _{DD}	126	RFU	168	V _{DD}

PART NUMBERS

EDO Operating Mode

PART NUMBER	CONFIGURATION	SPEED
MT9LD272AG-5 X	2 Meg x 72 ECC	50ns
MT9LD272AG-6 X	2 Meg x 72 ECC	60ns
MT18LD472AG-5 X	4 Meg x 72 ECC	50ns
MT18LD472AG-6 X	4 Meg x 72 ECC	60ns

FPM Operating Mode

PART NUMBER	CONFIGURATION	SPEED
MT9LD272AG-6	2 Meg x 72 ECC	60ns
MT18LD472AG-6	4 Meg x 72 ECC	60ns

GENERAL DESCRIPTION

The MT9LD272A(X) and MT18LD472A(X) are randomly accessed 16MB and 32MB memories organized in a x72 configuration. They are specially processed to operate from 3V to 3.6V for low-voltage memory systems.

During READ or WRITE cycles, each bit is uniquely addressed through the 21/22 address bits, which are entered 11 bits (A0-A10) at RAS# time and 10/11 bits (A0-A10) at CAS# time.

READ and WRITE cycles are selected with the WE# input. A logic HIGH on WE# dictates read mode, while a logic LOW on WE# dictates write mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. An EARLY WRITE occurs when WE# is taken LOW prior to CAS# falling. A LATE WRITE or READ-MODIFY-WRITE occurs when WE# falls after CAS# was taken LOW. During EARLY WRITE cycles, the data-outputs (Q) will remain High-Z regardless of the state of OE#. During LATE WRITE or READ-MODIFY-WRITE cycles, OE# must be taken HIGH to disable the data-outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping OE# LOW, no WRITE will occur, and the data-outputs will drive read data from the accessed location.

FAST PAGE MODE

FAST-PAGE-MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST-PAGE-MODE cycle is always initiated with a row address strobed in by RAS#, followed by a column address strobed in by CAS#. Additional columns may be accessed by providing valid column addresses, strobing CAS# and holding RAS# LOW, thus executing faster memory cycles. Returning RAS# HIGH terminates the FAST-PAGE-MODE operation.

EDO PAGE MODE

EDO PAGE MODE, designated by the "X" version, is an accelerated FAST-PAGE-MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS# goes back HIGH. EDO provides for CAS# precharge time (^tCP) to occur without the output data going invalid. This elimination of CAS# output control provides for pipelined READs.

FAST-PAGE-MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. EDO-PAGE-MODE DRAMs operate like FAST-PAGE-MODE DRAMs, except data will remain valid or become valid after CAS# goes HIGH during READs, provided RAS# and OE# are held LOW. If OE# is pulsed while RAS# and CAS# are LOW, data will toggle from valid data to High-Z and back to the same valid data. If OE# is toggled or pulsed after CAS# goes HIGH while RAS# remains LOW, data will transition to and remain High-Z.

During an application, if the DQ outputs are wire OR'd, OE# must be used to disable idle banks of DRAMs. Alternatively, pulsing WE# to the idle banks during CAS# HIGH time will also High-Z the outputs. Independent of OE# control, the outputs will disable after ^tOFF, which is referenced from the rising edge of RAS# or CAS#, whichever occurs last. (Refer to the 4 Meg x 4 [MT4LC4M4E8] DRAM data sheet for additional information on EDO functionality.)

REFRESH

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS# HIGH time. Correct memory cell data is preserved by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# REFRESH cycle (RAS#-ONLY, CBR or HIDDEN) so that all combinations of RAS# addresses (A0-A9/A10) are executed at least every ^tREF, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS# addressing.

SERIAL PRESENCE-DETECT OPERATION

This module family incorporates serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various DRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals,

together with SA(2:0), which provide eight unique DIMM/EEPROM addresses.

SPD CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figures 1 and 2).

SPD START CONDITION

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

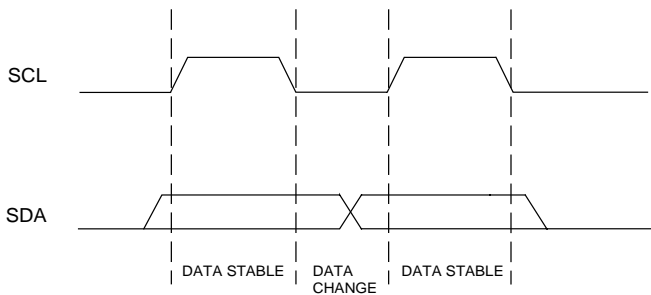
SPD STOP CONDITION

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

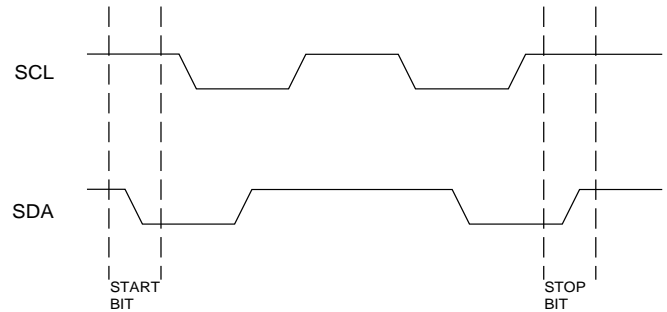
SPD ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (Figure 3).

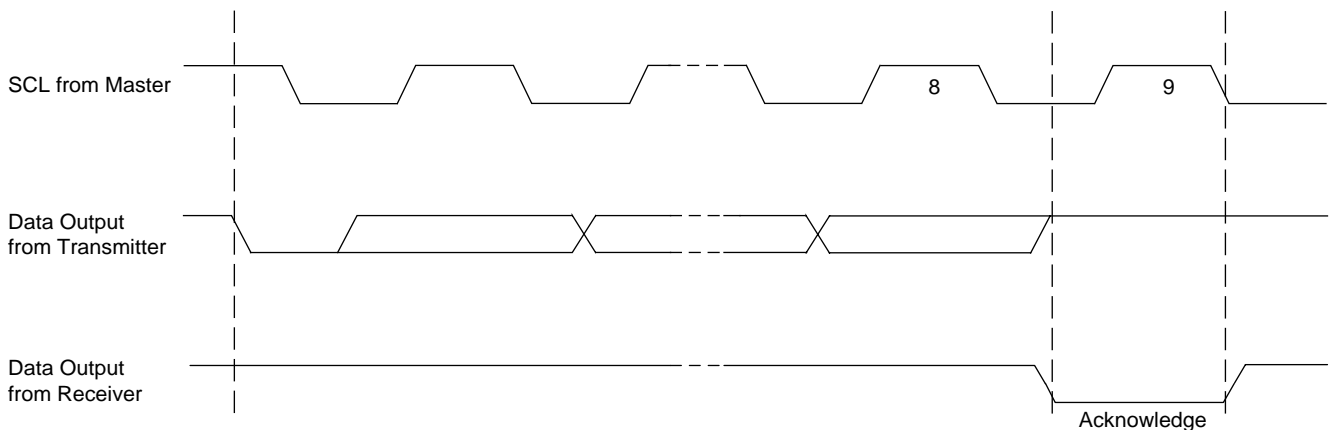
The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.



**Figure 1
DATA VALIDITY**



**Figure 2
DEFINITION OF START AND STOP**



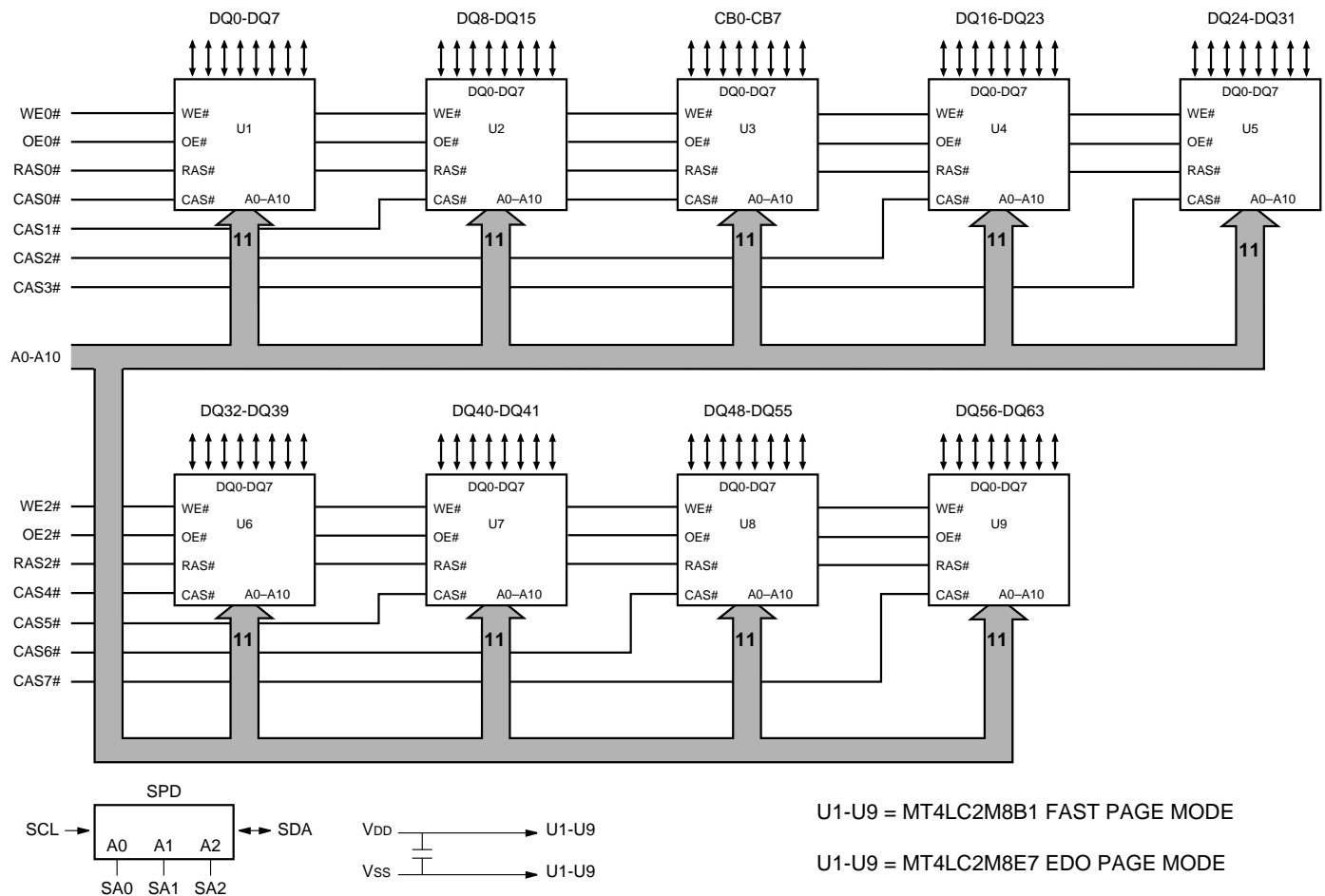
**Figure 3
ACKNOWLEDGE RESPONSE FROM RECEIVER**

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2, 4 MEG x 72
NONBUFFERED DRAM DIMMs

FUNCTIONAL BLOCK DIAGRAM
MT9LD272A(X) (16MB)

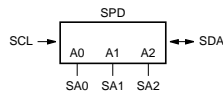
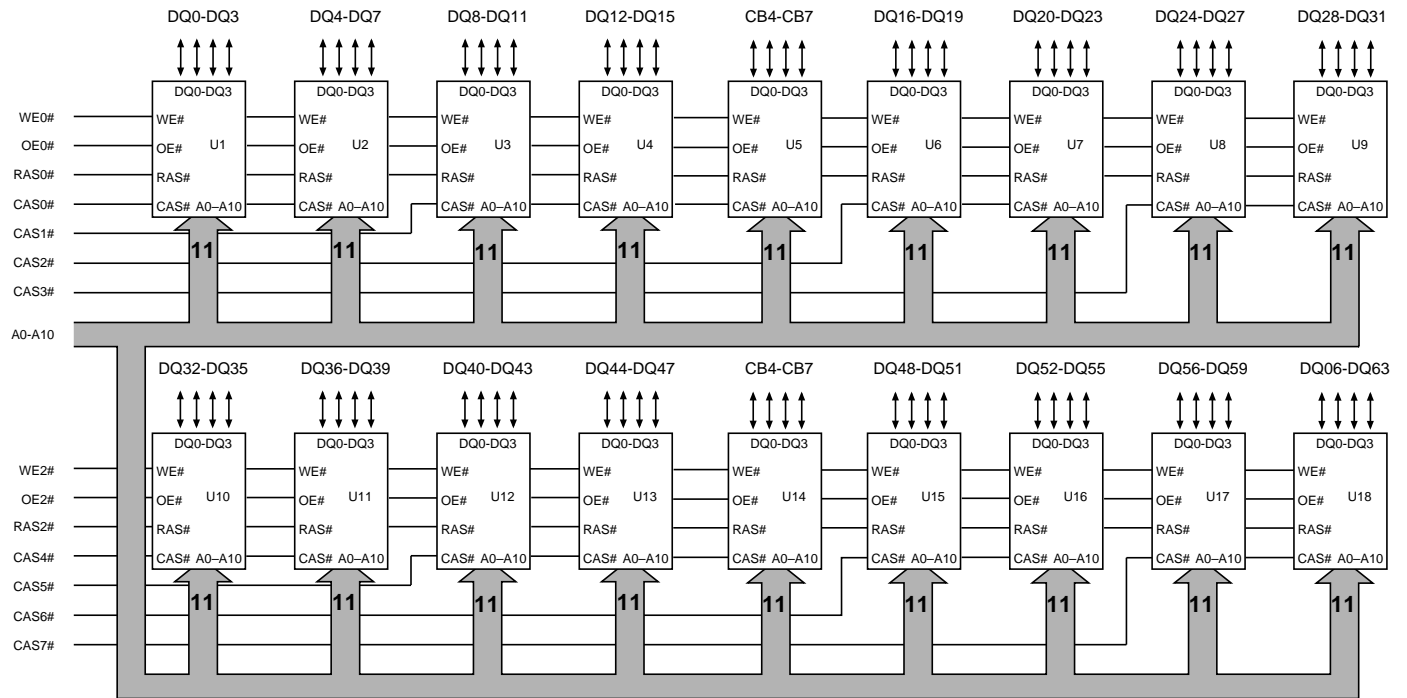


OBSOLETE



2, 4 MEG x 72
NONBUFFERED DRAM DIMMs

**FUNCTIONAL BLOCK DIAGRAM
MT18LD472A(X) (32MB)**



U1-U18 = MT4LC4M4B1 FAST PAGE MODE
U1-U18 = MT4LC4M4E8 EDO PAGE MODE

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
30, 45	RAS0#, RAS2#	Input	Row-Address Strobe: RAS# is used to clock-in the row-address bits. Two RAS# inputs allow for one x72 bank or two x36 banks.
28, 29, 46, 47, 112, 113, 130, 131	CAS0#-CAS7#	Input	Column-Address Strobe: CAS# is used to clock-in the column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles. Eight CAS# inputs allow byte access control for any memory bank configuration.
27, 48	WE0#, WE2#	Input	Write Enable: WE# is the READ/WRITE control for the DQ pins. If WE# is LOW prior to CAS# going LOW, the access is an EARLY WRITE cycle. If WE# is HIGH while CAS# is LOW, the access is a READ cycle, provided OE# is also LOW. If WE# goes LOW after CAS# goes LOW, then the cycle is a LATE WRITE cycle. A LATE WRITE cycle is generally used in conjunction with a READ cycle to form a READ-MODIFY-WRITE cycle.
31, 44	OE0#, OE2#	Input	Output Enable: OE# is the input/output control for the DQ pins. These signals may be driven, allowing LATE WRITE cycles.
33-38, 117-121	A0-A10	Input	Address Inputs: These inputs are multiplexed and clocked by RAS# and CAS#.
2-5, 7-11, 13-17, 19-20, 55-58, 60, 65-67, 69-72, 74-77, 86-89, 91-95, 97-101, 103-104, 139-142, 144, 149-151, 153-156, 158-161	DQ0-DQ63	Input/Output	Data I/O: For WRITE cycles, DQ0-DQ63 act as inputs to the addressed DRAM location. For READ access cycles, DQ0-DQ63 act as outputs for the addressed DRAM location.
21-22, 52-53, 105-106, 136-137	CB0-CB7	Input/Output	Check Bits.
42, 62, 111, 115, 125-126, 128, 132, 146	RFU	–	Reserved for Future Use: These pins should be left unconnected.
6, 18, 26, 40, 41, 49, 59, 73, 84, 90, 102, 110, 124, 133, 143, 157, 168	V _{DD}	Supply	Power Supply: +3.3V ±0.3V.
1, 12, 23, 32, 43, 54, 64, 68, 78, 85, 96, 107, 116, 127, 138, 148, 152, 162	V _{SS}	Supply	Ground.
82	SDA	Input/Output	Serial Presence-Detect Data. SDA is a bidirectional pin used to transfer addresses and data into and data out of the presence-detect portion of the module.
83	SCL	Input	Serial Clock for Presence-Detect. SCL is used to synchronize the presence-detect data transfer to and from the module.
165-167	SA0-SA2	Input	Presence-Detect Address Inputs. These pins are used to configure the presence-detect device.

SERIAL PRESENCE-DETECT MATRIX

BYTE	DESCRIPTION	ENTRY (VERSION)	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
0	NUMBER OF BYTES USED BY MICRON	128	1	0	0	0	0	0	0	0	80
1	TOTAL NUMBER OF SPD MEMORY BYTES	256	0	0	0	0	1	0	0	0	08
2	MEMORY TYPE	FAST PAGE MODE	0	0	0	0	0	0	0	1	01
		EDO PAGE MODE	0	0	0	0	0	0	1	0	02
3	NUMBER OF ROW ADDRESSES	11	0	0	0	0	1	0	1	1	0B
4	NUMBER OF COLUMN ADDRESSES	10 (16MB)	0	0	0	0	1	0	1	0	0A
		11 (32MB)	0	0	0	0	1	0	1	1	0B
5	NUMBER OF BANKS	1	0	0	0	0	0	0	0	1	01
6	DATA WIDTH	x72	0	1	0	0	1	0	0	0	48
7	DATA WIDTH (continued)	NONE	0	0	0	0	0	0	0	0	00
8	VOLTAGE INTERFACE	LVTTL	0	0	0	0	0	0	0	1	01
9	RAS# ACCESS TIME (t _{RAC})	50ns (-5)	0	0	1	1	0	0	1	0	32
		60ns (-6)	0	0	1	1	1	1	0	0	3C
10	CAS# ACCESS TIME (t _{CAC})	13ns (-5)	0	0	0	0	1	1	0	1	0D
		15ns (-6)	0	0	0	0	1	1	1	1	0F
11	MODULE CONFIGURATION TYPE	ECC	0	0	0	0	0	0	1	0	02
12	REFRESH RATES	15.625µs/NORMAL	0	0	0	0	0	0	0	0	00
13	DRAM WIDTH (PRIMARY DRAM)	x8 (16MB)	0	0	0	0	1	0	0	0	08
		x4 (32MB)	0	0	0	0	0	1	0	0	04
14	ERROR CHECKING DRAM DATA WIDTH	x8 (16MB)	0	0	0	0	1	0	0	0	08
		x4 (32MB)	0	0	0	0	0	1	0	0	04
15-61	RESERVED		0	0	0	0	0	0	0	0	00
62	SPD REVISION	REV. 0	0	0	0	0	0	0	0	0	00
63	CHECKSUM FOR BYTES 0-62	16MB -5 (EDO)	0	0	1	1	1	0	1	0	3A
		16MB -6 (EDO)	0	1	0	0	0	1	1	0	46
		16MB -6 (FPM)	0	1	0	0	0	1	0	1	45
		32MB -5 (EDO)	0	0	1	1	0	0	1	1	33
		32MB -6 (EDO)	0	0	1	1	1	1	1	1	3F
		32MB -6 (FPM)	0	0	1	1	1	1	1	1	0
64	MANUFACTURER'S JEDEC ID CODE	MICRON	0	0	1	0	1	1	0	0	2C
65-71	MANUFACTURER'S JEDEC CODE (CONT.)		1	1	1	1	1	1	1	1	FF
72	MANUFACTURING LOCATION		0	0	0	0	0	0	0	1	01
			0	0	0	0	0	0	1	0	02
			0	0	0	0	0	0	1	1	03
			0	0	0	0	0	1	0	0	04
73-90	MODULE PART NUMBER (ASCII)		x	x	x	x	x	x	x	x	XX
91	PCB IDENTIFICATION CODE	1	0	0	0	0	0	0	0	1	01
		2	0	0	0	0	0	0	1	0	02
		3	0	0	0	0	0	0	1	1	03
		4	0	0	0	0	0	1	0	0	04
92	IDENTIFICATION CODE (CONT.)	0	0	0	0	0	0	0	0	0	00
93	YEAR OF MANUFACTURE IN BCD		x	x	x	x	x	x	x	x	XX
94	WEEK OF MANUFACTURE IN BCD		x	x	x	x	x	x	x	x	XX
95-98	MODULE SERIAL NUMBER		x	x	x	x	x	x	x	x	XX
99-125	MANUFACTURE SPECIFIC DATA (RSVD)		-	-	-	-	-	-	-	-	-

NOTE: 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."
2. x = Variable Data.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V _{DD} Pin Relative to V _{SS}	-1V to +4.6V
Voltage on Inputs or I/O Pins	
Relative to V _{SS}	-1V to +4.6V
Operating Temperature, T _A (ambient)	0°C to +70°C
Storage Temperature (plastic)	-55°C to +125°C
Power Dissipation	9W

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	SIZE	MIN	MAX	UNITS	NOTES	
SUPPLY VOLTAGE	V _{DD}	ALL	3	3.6	V		
INPUT HIGH VOLTAGE: Logic 1; All inputs	V _{IH}	ALL	2	V _{DD} + 0.3	V	30	
INPUT LOW VOLTAGE: Logic 0; All inputs	V _{IL}	ALL	-0.5	0.8	V	30	
INPUT LEAKAGE CURRENT: Any input 0V ≤ V _{IN} ≤ V _{DD} + 0.3V (All other pins not under test = 0V)	CAS0#-CAS7#	I _{I1}	16MB 32MB	-4 -6	4 6	μA	
	A0-A10	I _{I2}	16MB 32MB	-18 -36	18 36	μA	
	WE0#, WE2#, OE0#, OE2#	I _{I3}	16MB 32MB	-10 -18	10 18	μA	
	RAS0#-RAS3#	I _{I4}	16MB 32MB	-10 -18	10 18	μA	
OUTPUT LEAKAGE CURRENT: DQ is disabled; 0V ≤ V _{OUT} ≤ V _{DD} + 0.3V	DQ0-DQ63, CB0-CB7	I _{OZ}	16MB 32MB	-5 -5	5 5	μA	
OUTPUT LEVELS: Output High Voltage (I _{OUT} = -2mA) Output Low Voltage (I _{OUT} = 2mA)	V _{OH}	ALL	2.4	–	V		
	V _{OL}	ALL	–	0.4	V		

I_{CC} OPERATING CONDITIONS AND MAXIMUM LIMITS

 (Notes: 1, 5, 6) ($V_{DD} = +3.3V \pm 0.3V$)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX		UNITS	NOTES
			-5*	-6		
STANDBY CURRENT: TTL (RAS# = CAS# = V_{IH})	I _{CC1}	16MB 32MB	9 18	9 18	mA	
STANDBY CURRENT: CMOS (RAS# = CAS# = $V_{DD} - 0.2V$)	I _{CC2}	16MB 32MB	9 9	9 9	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, address cycling: $t_{RC} = t_{RC}$ [MIN])	I _{CC3}	16MB 32MB	990 1,980	900 1,800	mA	3, 24
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS# = V_{IL} , CAS#, address cycling: $t_{PC} = t_{PC}$ [MIN])	I _{CC4}	16MB 32MB	– –	720 1,440	mA	3, 24
OPERATING CURRENT: EDO PAGE MODE ("X" version only) Average power supply current (RAS# = V_{IL} , CAS#, address cycling: $t_{PC} = t_{PC}$ [MIN])	I _{CC5} (X only)	16MB 32MB	990 1,980	900 1,800	mA	3, 24
REFRESH CURRENT: RAS#-ONLY Average power supply current (RAS# cycling, CAS# = V_{IH} : $t_{RC} = t_{RC}$ [MIN])	I _{CC6}	16MB 32MB	990 1,980	900 1,800	mA	3, 24
REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, address cycling: $t_{RC} = t_{RC}$ [MIN])	I _{CC7}	16MB 32MB	990 1,980	900 1,800	mA	3, 4

* EDO version only

CAPACITANCE

PARAMETER	SYMBOL	MAX		UNITS	NOTES
		16MB	32MB		
Input Capacitance: A0-A10	C _{I1}	51	96	pF	2
Input Capacitance: WE0#, WE2#, OE0#, OE2#	C _{I2}	39	67	pF	2
Input Capacitance: RAS0#, RAS2#	C _{I3}	39	67	pF	2
Input Capacitance: CAS0#-CAS7#	C _{I4}	17	24	pF	2
Input Capacitance: SCL, SA0-SA2	C _{I5}	6	6	pF	2
Input/Output Capacitance: DQ0-DQ63, CB0-CB7, SDA	C _{I0}	10	10	pF	2

FAST PAGE MODE

AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 12, 29) (V_{DD} = +3.3V ±0.3V)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6		UNITS	NOTES
PARAMETER	SYMBOL	MIN	MAX		
Access time from column address	t _{AA}		30	ns	
Column-address hold time (referenced to RAS#)	t _{AR}	45		ns	
Column-address setup time	t _{ASC}	0		ns	
Row-address setup time	t _{ASR}	0		ns	
Column address to WE# delay time	t _{AWD}	55		ns	23
Access time from CAS#	t _{CAC}		15	ns	14
Column-address hold time	t _{CAH}	10		ns	
CAS# pulse width	t _{CAS}	15	10,000	ns	
CAS# hold time (CBR Refresh)	t _{CHR}	10		ns	4
CAS# to output in Low-Z	t _{CLZ}	3		ns	25
CAS# precharge time	t _{CP}	10		ns	15
Access time from CAS# precharge	t _{CPA}		35	ns	
CAS# to RAS# precharge time	t _{CRP}	5		ns	
CAS# hold time	t _{CSH}	60		ns	
CAS# setup time (CBR Refresh)	t _{CSR}	5		ns	4
CAS# to WE# delay time	t _{CWD}	40		ns	23
WRITE command to CAS# lead time	t _{CWL}	15		ns	
Data-in hold time	t _{DH}	10		ns	22
Data-in setup time	t _{DS}	0		ns	22
Output disable	t _{OD}	3	15	ns	
Output enable	t _{OE}		15	ns	
OE# hold time from WE# during READ-MODIFY-WRITE cycle	t _{OEH}	15		ns	21
Output buffer turn-off delay	t _{OFF}	3	15	ns	19, 25, 26
OE# setup prior to RAS# during HIDDEN REFRESH cycle	t _{ORD}	0		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t _{PC}	35		ns	

**FAST PAGE MODE
AC ELECTRICAL CHARACTERISTICS**

 (Notes: 5, 6, 7, 8, 9, 12, 29) ($V_{DD} = +3.3V \pm 0.3V$)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6		UNITS	NOTES
PARAMETER	SYMBOL	MIN	MAX		
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	85		ns	
Access time from RAS#	t_{RAC}		60	ns	13
RAS# to column-address delay time	t_{RAD}	15		ns	17
Row-address hold time	t_{RAH}	10		ns	
RAS# pulse width	t_{RAS}	60	10,000	ns	
RAS# pulse width (FAST PAGE MODE)	t_{RASP}	60	125,000	ns	
Random READ or WRITE cycle time	t_{RC}	110		ns	
RAS# to CAS# delay time	t_{RCD}	20		ns	16
READ command hold time (referenced to CAS#)	t_{RCH}	0		ns	18
READ command setup time	t_{RCS}	0		ns	
Refresh period (2,048 cycles)	t_{REF}		32	ms	
RAS# precharge time	t_{RP}	40		ns	
RAS# to CAS# precharge time	t_{RPC}	0		ns	
READ command hold time (referenced to RAS#)	t_{RRH}	0		ns	18
RAS# hold time	t_{RSH}	15		ns	
READ-WRITE cycle time	t_{RWC}	155		ns	
RAS# to WE# delay time	t_{RWD}	85		ns	23
WRITE command to RAS# lead time	t_{RWL}	15		ns	
Transition time (rise or fall)	t_T	2	50	ns	
WRITE command hold time	t_{WCH}	10		ns	
WRITE command hold time (referenced to RAS#)	t_{WCR}	45		ns	
WE# command setup time	t_{WCS}	0		ns	23
WRITE command pulse width	t_{WP}	10		ns	
WE# hold time (CBR Refresh)	t_{WRH}	10		ns	
WE# setup time (CBR Refresh)	t_{WRP}	10		ns	

**EDO PAGE MODE
AC ELECTRICAL CHARACTERISTICS**
(Notes: 5, 6, 7, 8, 9, 12, 29) ($V_{DD} = +3.3V \pm 0.3V$)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-5		-6		UNITS	NOTES
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX		
Access time from column address	t_{AA}		25		30	ns	
Column-address setup to CAS# precharge	t_{ACH}	12		15		ns	
Column-address hold time (referenced to RAS#)	t_{AR}	38		45		ns	
Column-address setup time	t_{ASC}	0		0		ns	
Row-address setup time	t_{ASR}	0		0		ns	
Column-address to WE# delay time	t_{AWD}	42		49		ns	23
Access time from CAS#	t_{CAC}		13		15	ns	14
Column-address hold time	t_{CAH}	8		10		ns	
CAS# pulse width	t_{CAS}	8	10,000	10	10,000	ns	
CAS# hold time (CBR Refresh)	t_{CHR}	8		10		ns	4
CAS# to output in Low-Z	t_{CLZ}	0		0		ns	
Data output hold after CAS# LOW	t_{COH}	3		3		ns	
CAS# precharge time	t_{CP}	8		10		ns	15
Access time from CAS# precharge	t_{CPA}		28		35	ns	
CAS# to RAS# precharge time	t_{CRP}	5		5		ns	
CAS# hold time	t_{CSH}	38		45		ns	
CAS# setup time (CBR Refresh)	t_{CSR}	5		5		ns	4
CAS# to WE# delay time	t_{CWD}	28		35		ns	23
WRITE command to CAS# lead time	t_{CWL}	8		10		ns	
Data-in hold time	t_{DH}	8		10		ns	22
Data-in setup time	t_{DS}	0		0		ns	22
Output disable	t_{OD}	0	12	0	15	ns	
Output enable	t_{OE}		12		15	ns	
OE# hold time from WE# during READ-MODIFY-WRITE cycle	t_{OEH}	8		10/12*		ns	21
OE# HIGH hold time from CAS# HIGH	t_{OEHC}	5		10		ns	21
OE# HIGH pulse width	t_{OEP}	5		5		ns	
OE# LOW to CAS# HIGH setup time	t_{OES}	4		5		ns	
Output buffer turn-off delay	t_{OFF}	0	12	0	15	ns	19, 26
OE# setup prior to RAS# during HIDDEN REFRESH cycle	t_{ORD}	0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	t_{PC}	20		25		ns	
EDO-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	47		56		ns	
Access time from RAS#	t_{RAC}		50		60	ns	13
RAS# to column-address delay time	t_{RAD}	9		12		ns	17
Row-address hold time	t_{RAH}	9		10		ns	
RAS# pulse width	t_{RAS}	50	10,000	60	10,000	ns	
RAS# pulse width (EDO PAGE MODE)	t_{RASP}	50	125,000	60	125,000	ns	
Random READ or WRITE cycle time	t_{RC}	84		104		ns	
RAS# to CAS# delay time	t_{RCD}	11		14		ns	16
READ command hold time (referenced to CAS#)	t_{RCH}	0		0		ns	18
READ command setup time	t_{RCS}	0		0		ns	
Refresh period (2,048 cycles)	t_{REF}		32		32	ms	
RAS# precharge time	t_{RP}	30		40		ns	

OBSOLETE



2, 4 MEG x 72 NONBUFFERED DRAM DIMMS

EDO PAGE MODE AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 12, 29) ($V_{DD} = +3.3V \pm 0.3V$)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-5		-6			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
RAS# to CAS# precharge time	t_{RPC}	5		5		ns	
READ command hold time (referenced to RAS#)	t_{RRH}	0		0		ns	18
RAS# hold time	t_{RSH}	13		15		ns	
READ WRITE cycle time	t_{RWC}	116		140		ns	
RAS# to WE# delay time	t_{RWD}	67		79		ns	23
WRITE command to RAS# lead time	t_{RWL}	13		15		ns	
Transition time (rise or fall)	t_T	2	50	2	50	ns	
WRITE command hold time	t_{WCH}	8		10		ns	
WRITE command hold time (referenced to RAS#)	t_{WCR}	38		45		ns	
WE# command setup time	t_{WCS}	0		0		ns	23
Output disable delay from WE# (CAS# HIGH)	t_{WHZ}	0	12	0	15	ns	
WRITE command pulse width	t_{WP}	5		5		ns	
WE# pulse to disable at CAS# HIGH	t_{WPZ}	10		10		ns	
WE# hold time (CBR Refresh)	t_{WRH}	8		10		ns	
WE# setup time (CBR Refresh)	t_{WRP}	8		10		ns	

SERIAL PRESENCE-DETECT EEPROM OPERATING CONDITIONS

 (Notes: 1) ($V_{DD} = +3.3V \pm 0.3V$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V_{DD}	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{IH}	$V_{DD} \times 0.7$	$V_{DD} + 0.5$	V	
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-1	$V_{DD} \times 0.3$	V	
OUTPUT LOW VOLTAGE: $I_{OUT} = 3mA$	V_{OL}	-	0.4	V	
INPUT LEAKAGE CURRENT: $V_{IN} = GND$ to V_{DD}	I_{LI}	-	10	μA	
OUTPUT LEAKAGE CURRENT: $V_{OUT} = GND$ to V_{DD}	I_{LO}	-	10	μA	
STANDBY CURRENT: SCL = SDA = $V_{DD} - 0.3V$; All other inputs = GND or $3.3V + 10\%$	I_{SB}	-	30	μA	
POWER SUPPLY CURRENT: SCL clock frequency = 100 KHz	I_{CC}	-	2	mA	

SERIAL PRESENCE-DETECT EEPROM AC ELECTRICAL CHARACTERISTICS

 (Notes: 1) ($V_{DD} = +3.3V \pm 0.3V$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SCL LOW to SDA data-out valid	t_{AA}	0.3	3.5	μs	
Time the bus must be free before a new transition can start	t_{BUF}	4.7		μs	
Data-out hold time	t_{DH}	300		ns	
SDA and SCL fall time	t_F		300	ns	
Data-in hold time	$t_{HD:DAT}$	0		μs	
Start condition hold time	$t_{HD:STA}$	4		μs	
Clock HIGH period	t_{HIGH}	4		μs	
Noise suppression time constant at SCL, SDA inputs	t_I		100	ns	
Clock LOW period	t_{LOW}	4.7		μs	
SDA and SCL rise time	t_R		1	μs	
SCL clock frequency	f_{SCL}		100	KHz	
Data-in setup time	$t_{SU:DAT}$	250		ns	
Start condition setup time	$t_{SU:STA}$	4.7		μs	
Stop condition setup time	$t_{SU:STO}$	4.7		μs	
WRITE cycle time	t_{WR}		10	ms	28

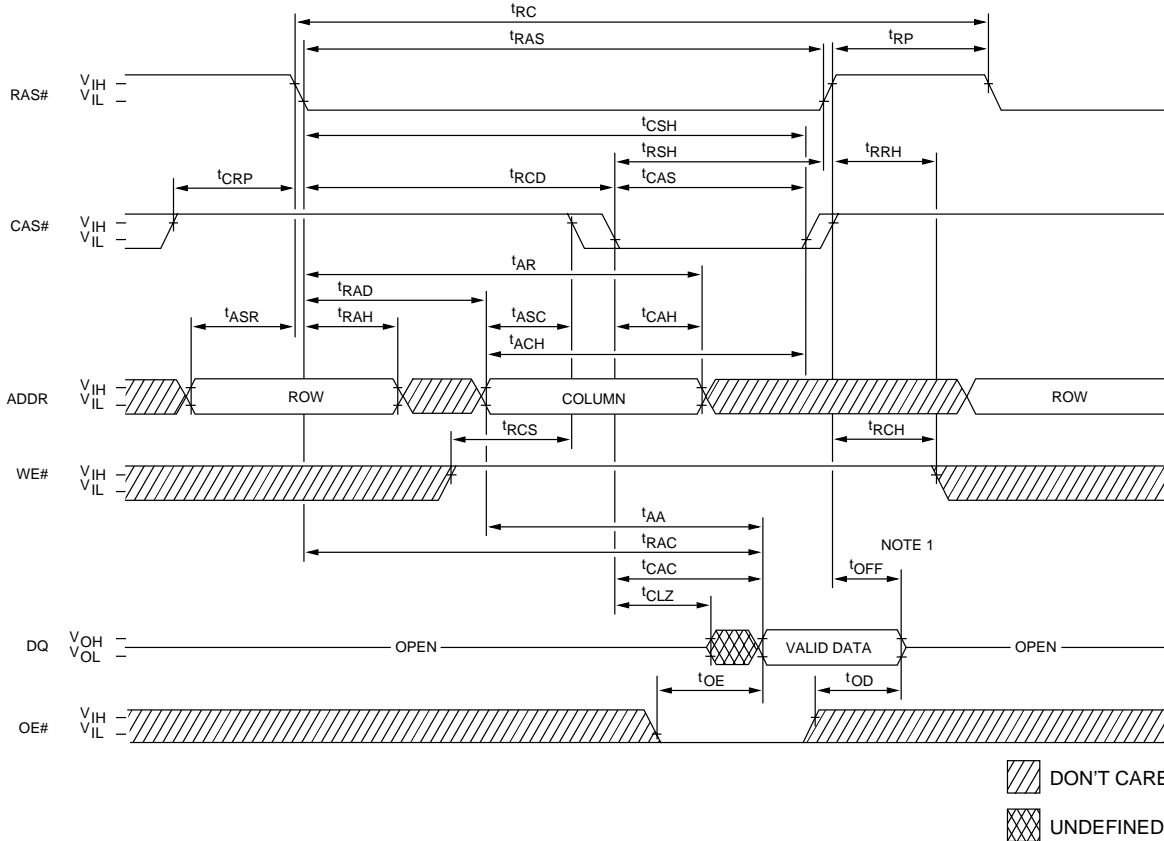
NOTES

1. All voltages referenced to V_{SS} .
2. This parameter is sampled. $V_{DD} = +3.3V$; $f = 1$ MHz.
3. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
6. An initial pause of $100\mu s$ is required after power-up, followed by eight RAS# REFRESH cycles (RAS#-ONLY or CBR with WE# HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.
7. AC characteristics assume $t_T = 5ns$ for FPM and $2.5ns$ for EDO.
8. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
9. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
10. If $CAS\# = V_{IH}$, data output is High-Z.
11. If $CAS\# = V_{IL}$, data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates and $100pF$ and $V_{OL} = 0.8V$ and $V_{OH} = 2V$.
13. Requires that t_{AA} and t_{RAC} are not violated.
14. Requires that t_{AA} and t_{CAC} are not violated.
15. If $CAS\#$ is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $CAS\#$ must be pulsed HIGH for t_{CP} .
16. The t_{RCD} (MAX) limit is no longer specified. t_{RCD} (MAX) was specified as a reference point only. If t_{RCD} was greater than the specified t_{RCD} (MAX) limit, then access time was controlled exclusively by t_{CAC} (t_{RAC} [MIN] no longer applied). With or without the t_{RCD} (MAX) limit, t_{AA} and t_{CAC} must always be met.
17. The t_{RAD} (MAX) limit is no longer specified. t_{RAD} (MAX) was specified as a reference point only. If t_{RAD} was greater than the specified t_{RAD} (MAX) limit, then access time was controlled exclusively by t_{AA} (t_{RAC} and t_{CAC} no longer applied). With or without the t_{RAD} (MAX) limit, t_{AA} , t_{RAC} and t_{CAC} must always be met.
18. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
19. t_{OFF} (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $WE\# = LOW$ and $OE\# = HIGH$.
21. LATE WRITE and READ-MODIFY-WRITE cycles must have both t_{OD} and t_{OEH} met ($OE\# HIGH$ during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $CAS\#$ remains LOW and $OE\#$ is taken back LOW after t_{OEH} is met. If $CAS\#$ goes HIGH prior to $OE\#$ going back LOW, the DQs will remain open.
22. These parameters are referenced to $CAS\#$ leading edge in EARLY WRITE cycles and $WE\#$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. t_{WCS} , t_{RWD} , t_{AWD} and t_{CWD} are not restrictive operating parameters. t_{WCS} applies to EARLY WRITE cycles. t_{RWD} , t_{AWD} and t_{CWD} apply to READ-MODIFY-WRITE cycles. If $t_{WCS} \geq t_{WCS}$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $t_{WCS} < t_{WCS}$ (MIN) and $t_{RWD} \geq t_{RWD}$ (MIN), $t_{AWD} \geq t_{AWD}$ (MIN) and $t_{CWD} \geq t_{CWD}$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $OE\#$ held HIGH and $WE\#$ taken LOW after $CAS\#$ goes LOW result in a LATE WRITE ($OE\#$ -controlled) cycle. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not applicable in a LATE WRITE cycle.
24. Column address changed once each cycle.
25. The $3ns$ minimum parameter guaranteed by design.
26. With the FPM option, t_{OFF} is determined by the first RAS# or CAS# signal to transition HIGH. In comparison, t_{OFF} on an EDO option is determined by the latter of the RAS# and CAS# signals to transition HIGH.
27. Applies to both FPM and EDO modules.

NOTES (continued)

28. The SPD EEPROM WRITE cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit are disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.
29. If OE# is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
30. V_{IH} overshoot: $V_{IH} (MAX) = V_{DD} + 2V$ for a pulse width $\leq 10ns$, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: $V_{IL} (MIN) = -2V$ for a pulse width $\leq 10ns$, and the pulse width cannot be greater than one third of the cycle rate.

READ CYCLE ²⁷



**FAST PAGE MODE AND EDO PAGE MODE
TIMING PARAMETERS**

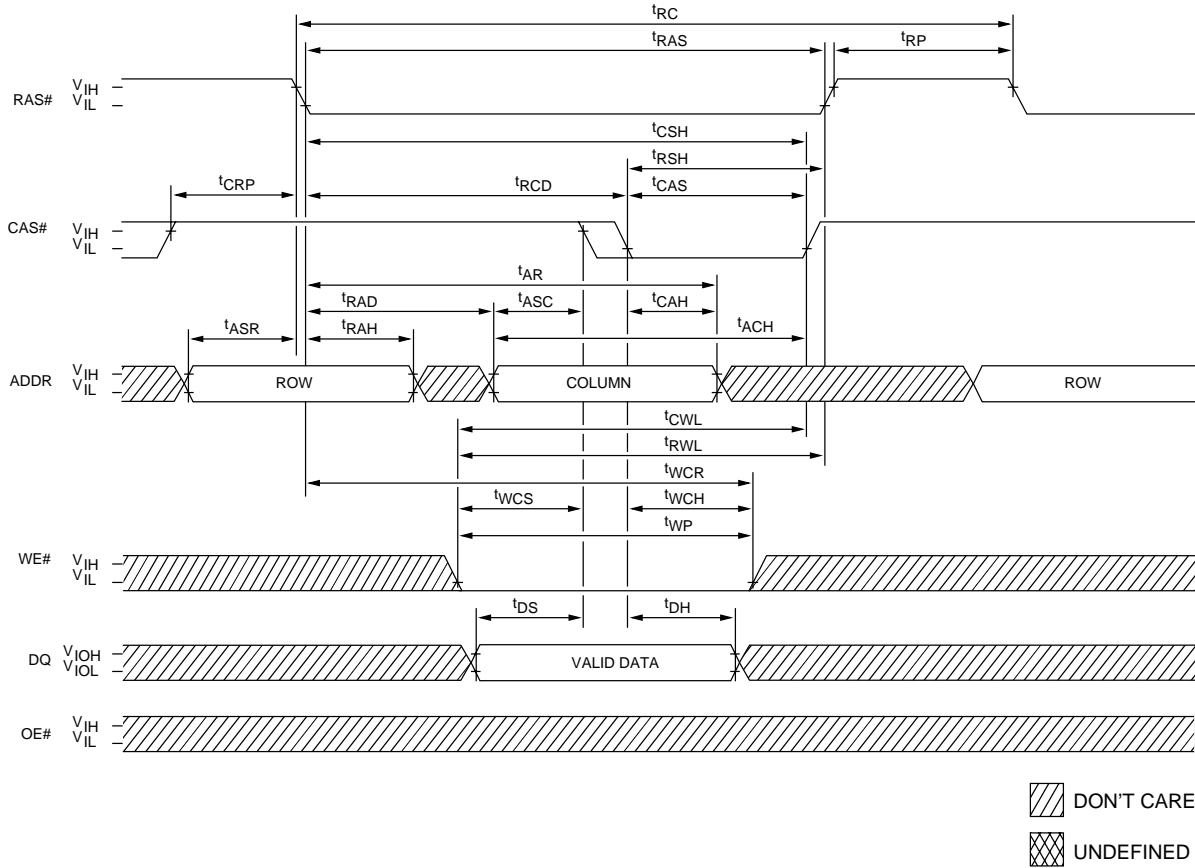
SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{AA}		25		30	ns
t_{ACH} (EDO)	12		15		ns
t_{AR}	38		45		ns
t_{ASC}	0		0		ns
t_{ASR}	0		0		ns
t_{CAC}		13		15	ns
t_{CAH}	8		10		ns
t_{CAS} (EDO)	8	10,000	10	10,000	ns
t_{CAS} (FPM)	-	-	15	10,000	ns
t_{CLZ} (EDO)	0		0		ns
t_{CLZ} (FPM)	-		3		ns
t_{CRP}	5		5		ns
t_{CSH} (EDO)	38		45		ns
t_{CSH} (FPM)	-		60		ns
t_{OD} (EDO)	0	12	0	15	ns
t_{OD} (FPM)	-	-	3	15	ns
t_{OE}		12		15	ns

SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{OFF} (EDO)	0	12	0	15	ns
t_{OFF} (FPM)	-	-	3	15	ns
t_{RAC}		50		60	ns
t_{RAD} (EDO)	9		12		ns
t_{RAD} (FPM)	-		15		ns
t_{RAH}	9		10		ns
t_{RAS}	50	10,000	60	10,000	ns
t_{RC} (EDO)	84		104		ns
t_{RC} (FPM)	-		110		ns
t_{RCD} (EDO)	11		14		ns
t_{RCD} (FPM)	-		20		ns
t_{RCH}	0		0		ns
t_{RCS}	0		0		ns
t_{RP}	30		40		ns
t_{RRH}	0		0		ns
t_{RSH}	13		15		ns

*EDO version only

NOTE: 1. For EDO, t_{OFF} is referenced from rising edge of RAS# or CAS#, whichever occurs last. For FPM, t_{OFF} is referenced from rising edge of RAS# or CAS#, whichever occurs first.

EARLY WRITE CYCLE ²⁷



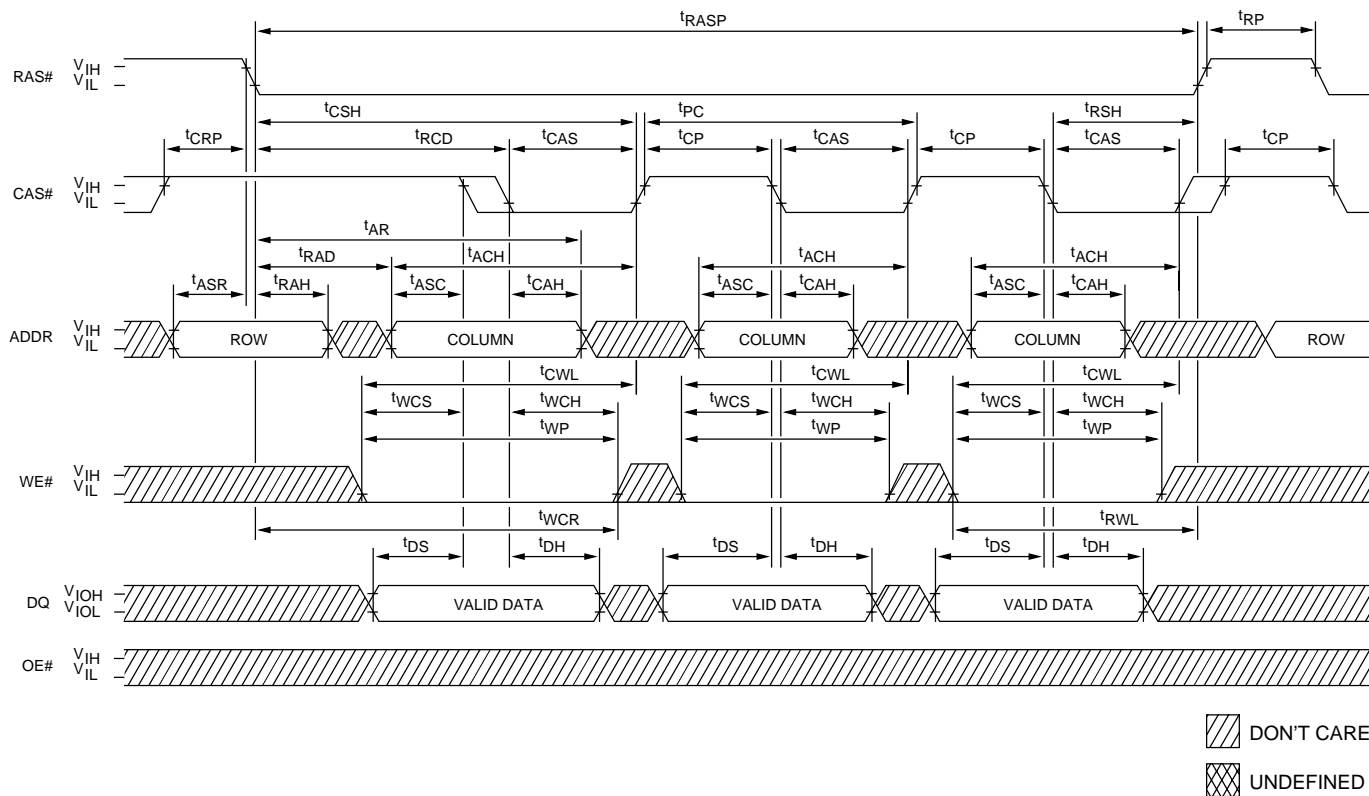
FAST PAGE MODE AND EDO PAGE MODE
TIMING PARAMETERS

SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{ACH} (EDO)	12		15		ns
t_{AR}	38		45		ns
t_{ASC}	0		0		ns
t_{ASR}	0		0		ns
t_{CAH}	8		10		ns
t_{CAS} (FPM)	-	-	15	10,000	ns
t_{CAS} (EDO)	8	10,000	10	10,000	ns
t_{CRP}	5		5		ns
t_{CSH} (FPM)	-		60		ns
t_{CSH} (EDO)	38		45		ns
t_{CWL} (FPM)	-		15		ns
t_{CWL} (EDO)	8		10		ns
t_{DH}	8		10		ns
t_{DS}	0		0		ns
t_{RAD} (FPM)	-		15		ns

SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{RAD} (EDO)	9		12		ns
t_{RAH}	9		10		ns
t_{RAS}	50	10,000	60	10,000	ns
t_{RC} (FPM)	-		110		ns
t_{RC} (EDO)	84		104		ns
t_{RCD} (FPM)	-		20		ns
t_{RCD} (EDO)	11		14		ns
t_{RP}	30		40		ns
t_{RSH}	13		15		ns
t_{RWL}	13		15		ns
t_{WCH}	8		10		ns
t_{WCR}	38		45		ns
t_{WCS}	0		0		ns
t_{WP} (FPM)	-		10		ns
t_{WP} (EDO)	5		5		ns

*EDO version only

FAST/EDO-PAGE-MODE EARLY WRITE CYCLE 27



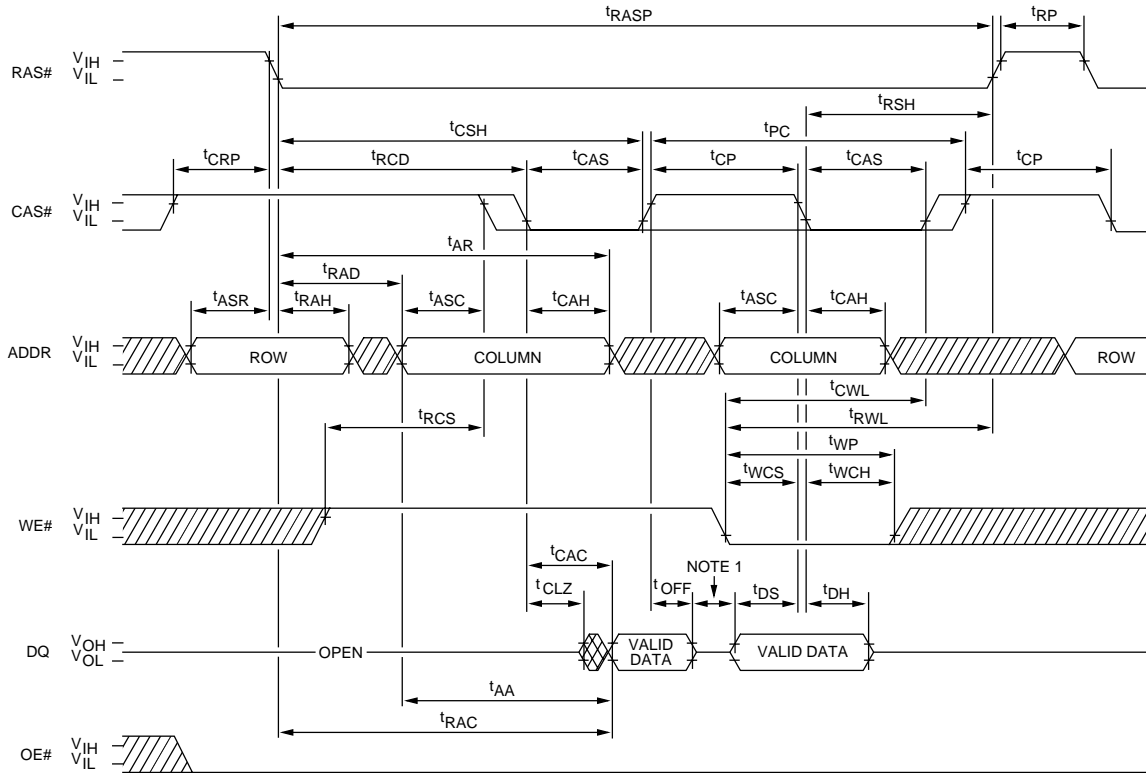
FAST PAGE MODE AND EDO PAGE MODE
TIMING PARAMETERS

SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{ACH} (EDO)	12		15		ns
t _{AR}	38		45		ns
t _{ASC}	0		0		ns
t _{ASR}	0		0		ns
t _{CAH}	8		10		ns
t _{CAS} (EDO)	8	10,000	10	10,000	ns
t _{CAS} (FPM)	-	-	15	10,000	ns
t _{CP}	8		10		ns
t _{CRP}	5		5		ns
t _{CSH} (EDO)	38		45		ns
t _{CSH} (FPM)	-		60		ns
t _{CWL} (EDO)	8		10		ns
t _{CWL} (FPM)	-		15		ns
t _{DH}	8		10		ns
t _{DS}	0		0		ns
t _{PC} (EDO)	20		25		ns

SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{PC} (FPM)	-		35		ns
t _{RAD} (EDO)	9		12		ns
t _{RAD} (FPM)	-		15		ns
t _{RAH}	9		10		ns
t _{RASP}	50	125,000	60	125,000	ns
t _{RCD} (EDO)	11		14		ns
t _{RCD} (FPM)	-		20		ns
t _{RP}	30		40		ns
t _{RSH}	13		15		ns
t _{RWL}	13		15		ns
t _{WCH}	8		10		ns
t _{WCR}	38		45		ns
t _{WCS}	0		0		ns
t _{WP} (EDO)	5		5		ns
t _{WP} (FPM)	-		10		ns

*EDO version only

FAST-PAGE-MODE READ EARLY WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



DON'T CARE
 UNDEFINED

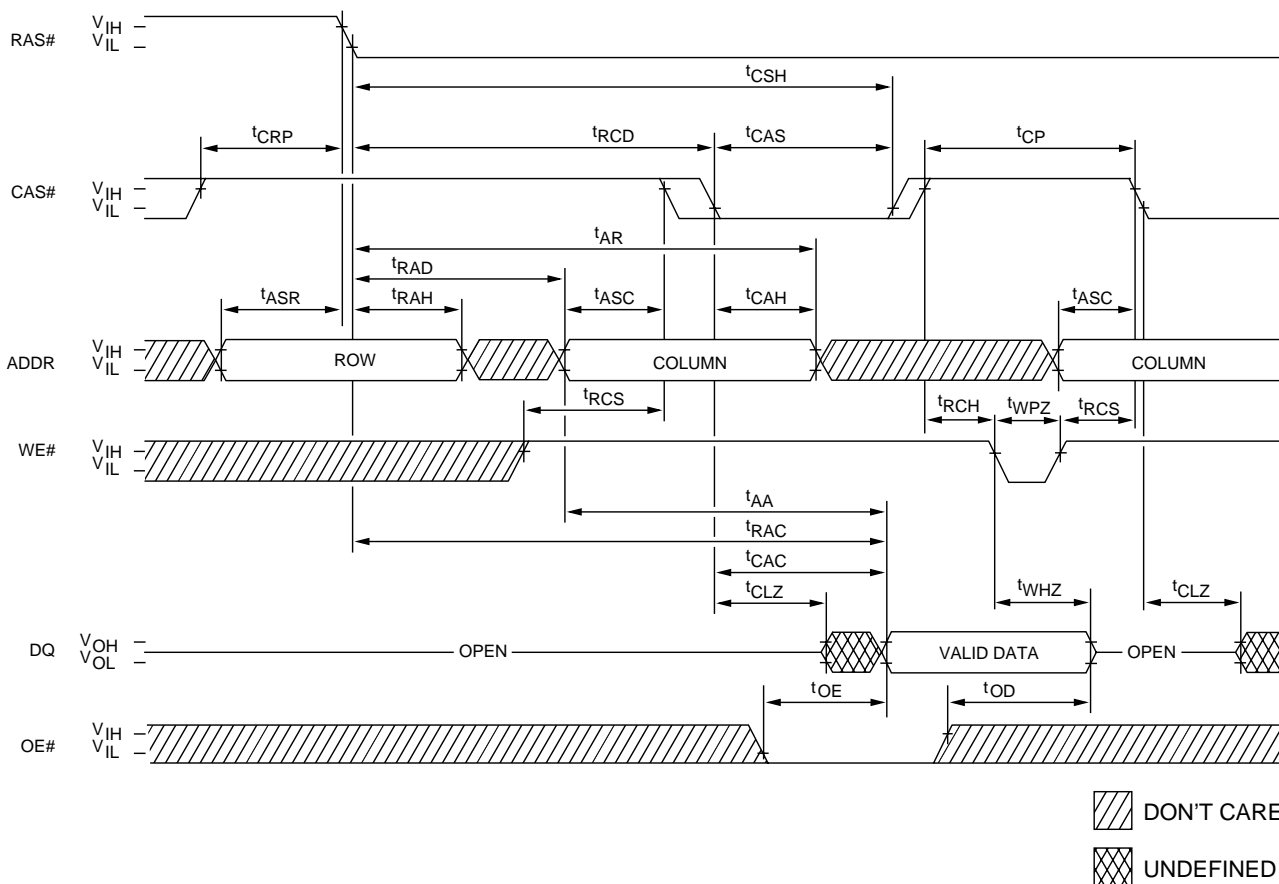
**FAST PAGE MODE
TIMING PARAMETERS**

SYMBOL	-6		UNITS
	MIN	MAX	
tAA		30	ns
tAR	45		ns
tASC	0		ns
tASR	0		ns
tCAC		15	ns
tCAH	10		ns
tCAS	15	10,000	ns
tCLZ	3		ns
tCP	10		ns
tCRP	5		ns
tCSH	60		ns
tCWL	15		ns
tDH	10		ns
tDS	0		ns

SYMBOL	-6		UNITS
	MIN	MAX	
tOFF	3	15	ns
tPC	35		ns
tRAC		60	ns
tRAD	15		ns
tRAH	10		ns
tRASP	60	125,000	ns
tRCD	20		ns
tRCS	0		ns
tRP	40		ns
tRSH	15		ns
tRWL	15		ns
tWCH	10		ns
tWCS	0		ns
tWP	10		ns

NOTE: 1. Do not drive data prior to tristate.

EDO READ CYCLE
(with WE#-controlled disable)

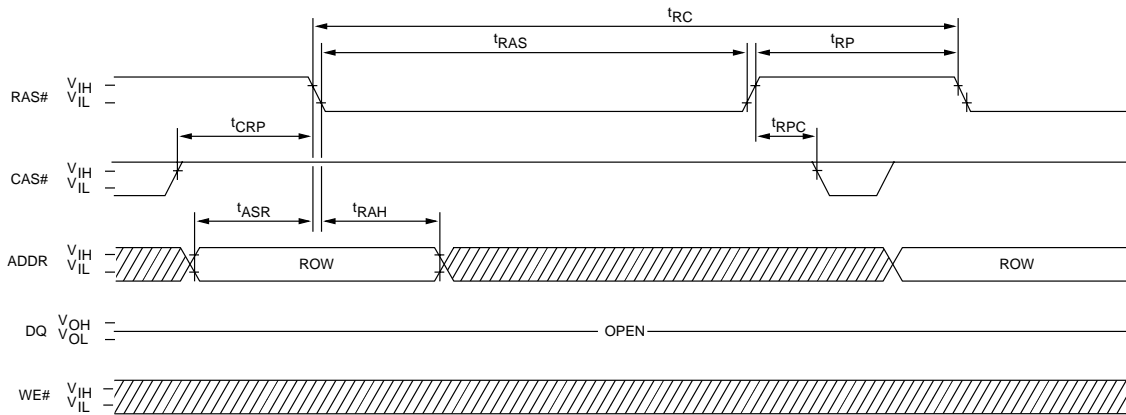


**EDO PAGE MODE
TIMING PARAMETERS**

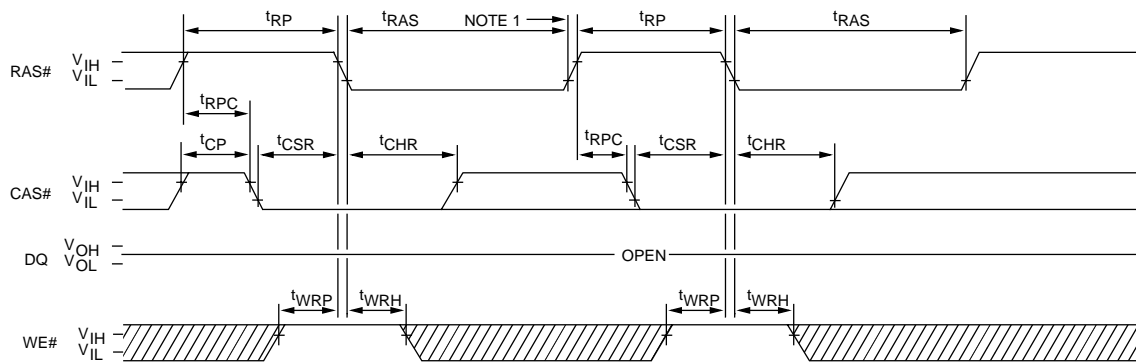
SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{AA}		25		30	ns
t _{AR}	38		45		ns
t _{ASC}	0		0		ns
t _{ASR}	0		0		ns
t _{CAC}		13		15	ns
t _{CAH}	8		10		ns
t _{CAS}	8	10,000	10	10,000	ns
t _{CLZ}	0		0		ns
t _{CP}	8		10		ns
t _{CRP}	5		5		ns
t _{CSH}	38		45		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{OD}	0	12	0	15	ns
t _{OE}		12		15	ns
t _{RAC}		50		60	ns
t _{RAD}	9		12		ns
t _{RAH}	9		10		ns
t _{RCD}	11		14		ns
t _{RCH}	0		0		ns
t _{RCS}	0		0		ns
t _{WHZ}	0	12	0	15	ns
t _{WPZ}	10		10		ns

RAS#-ONLY REFRESH CYCLE ²⁷



CBR REFRESH CYCLE ²⁷
(Addresses, OE# = DON'T CARE)



DON'T CARE
 UNDEFINED

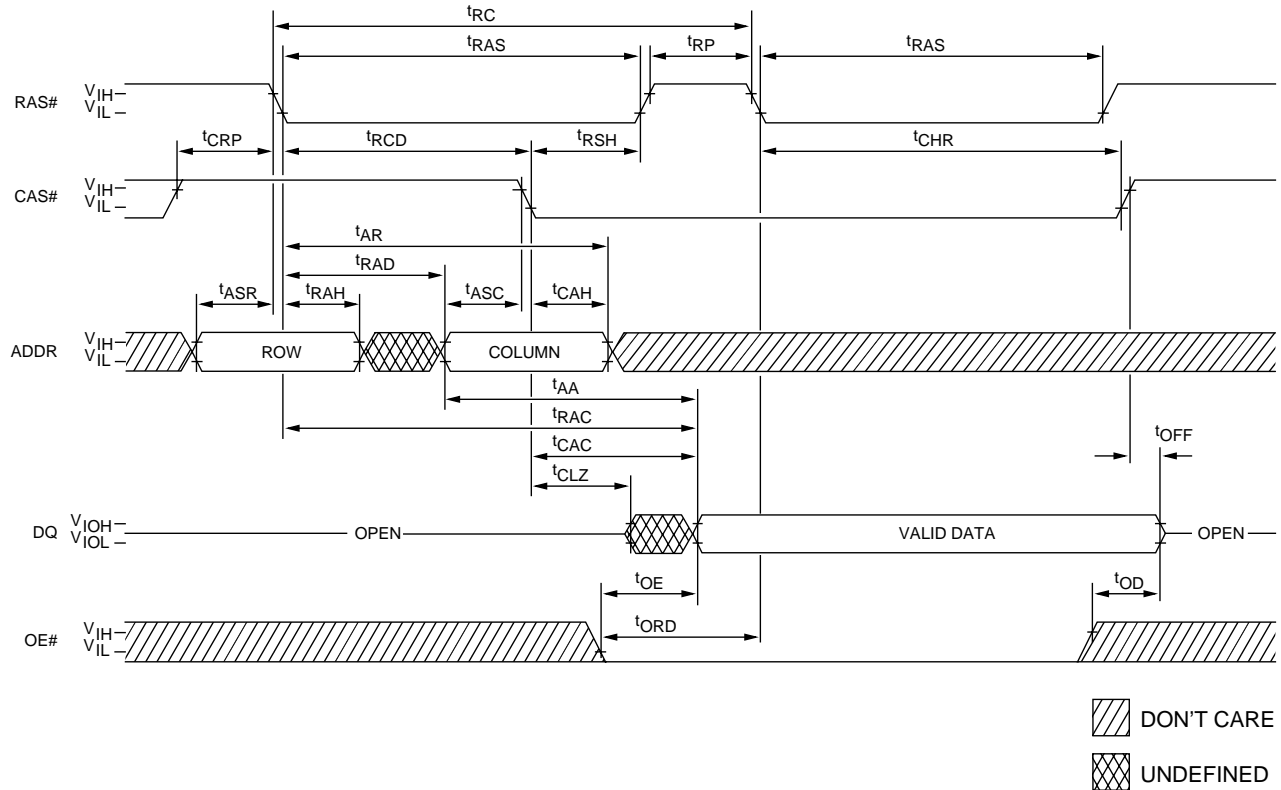
**FAST PAGE MODE AND EDO PAGE MODE
TIMING PARAMETERS**

SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{ASR}	0		0		ns
t _{CHR}	8		10		ns
t _{CP}	8		10		ns
t _{CRP}	5		5		ns
t _{CSR}	5		5		ns
t _{RAH}	9		10		ns
t _{RAS}	50	10,000	60	10,000	ns

SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{RC} (FPM)	—		110		ns
t _{RC} (EDO)	84		104		ns
t _{RP}	30		40		ns
t _{RPC} (FPM)	—		0		ns
t _{RPC} (EDO)	5		5		ns
t _{WRH}	8		10		ns
t _{WRP}	8		10		ns

*EDO version only

HIDDEN REFRESH CYCLE ^{20, 27}
(WE# = HIGH; OE# = LOW)



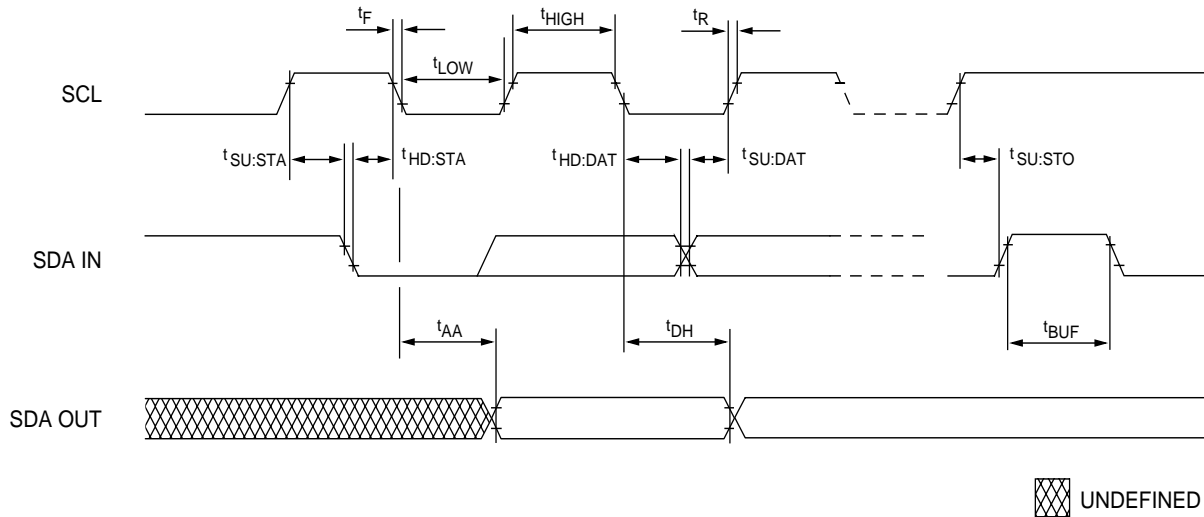
**FAST PAGE MODE AND EDO PAGE MODE
TIMING PARAMETERS**

SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCHR	8		10		ns
tCLZ (FPM)	-		3		ns
tCLZ (EDO)	0		0		ns
tCRP	5		5		ns
tOD (FPM)	-		3	15	ns
tOD (EDO)	0	12	0	15	ns
tOE		12		15	ns
tOFF (FPM)	-		3	15	ns

SYMBOL	-5*		-6		UNITS
	MIN	MAX	MIN	MAX	
tOFF (EDO)	0	12	0	15	ns
tORD	0		0		ns
tRAC		50		60	ns
tRAD (FPM)	-		15		ns
tRAD (EDO)	9		12		ns
tRAH	9		10		ns
tRAS	50	10,000	60	10,000	ns
tRC (FPM)	-		110		ns
tRC (EDO)	84		104		ns
tRCD (FPM)	-		20		ns
tRCD (EDO)	11		14		ns
tRP	30		40		ns
tRSH	13		15		ns

*EDO version only

SPD EEPROM



**SERIAL PRESENCE-DETECT EEPROM
TIMING PARAMETERS**

SYMBOL	MIN	MAX	UNITS
t_{AA}	0.3	3.5	μs
t_{BUF}	4.7		μs
t_{DH}	300		ns
t_F		300	ns
$t_{HD:DAT}$	0		μs
$t_{HD:STA}$	4		μs

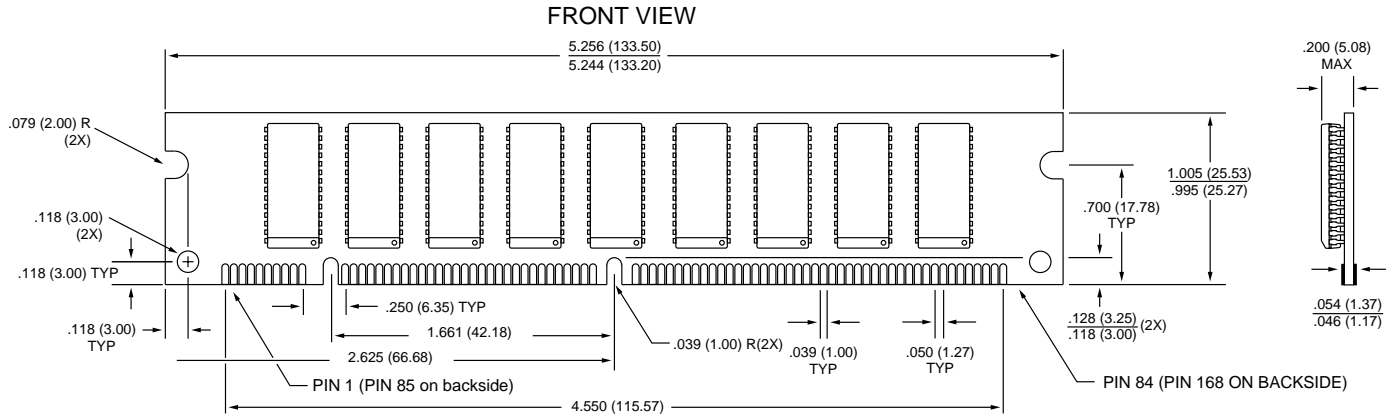
SYMBOL	MIN	MAX	UNITS
t_{HIGH}	4		μs
t_{LOW}	4.7		μs
t_R		1	μs
$t_{SU:DAT}$	250		ns
$t_{SU:STA}$	4.7		μs
$t_{SU:STO}$	4.7		μs

OBSOLETE

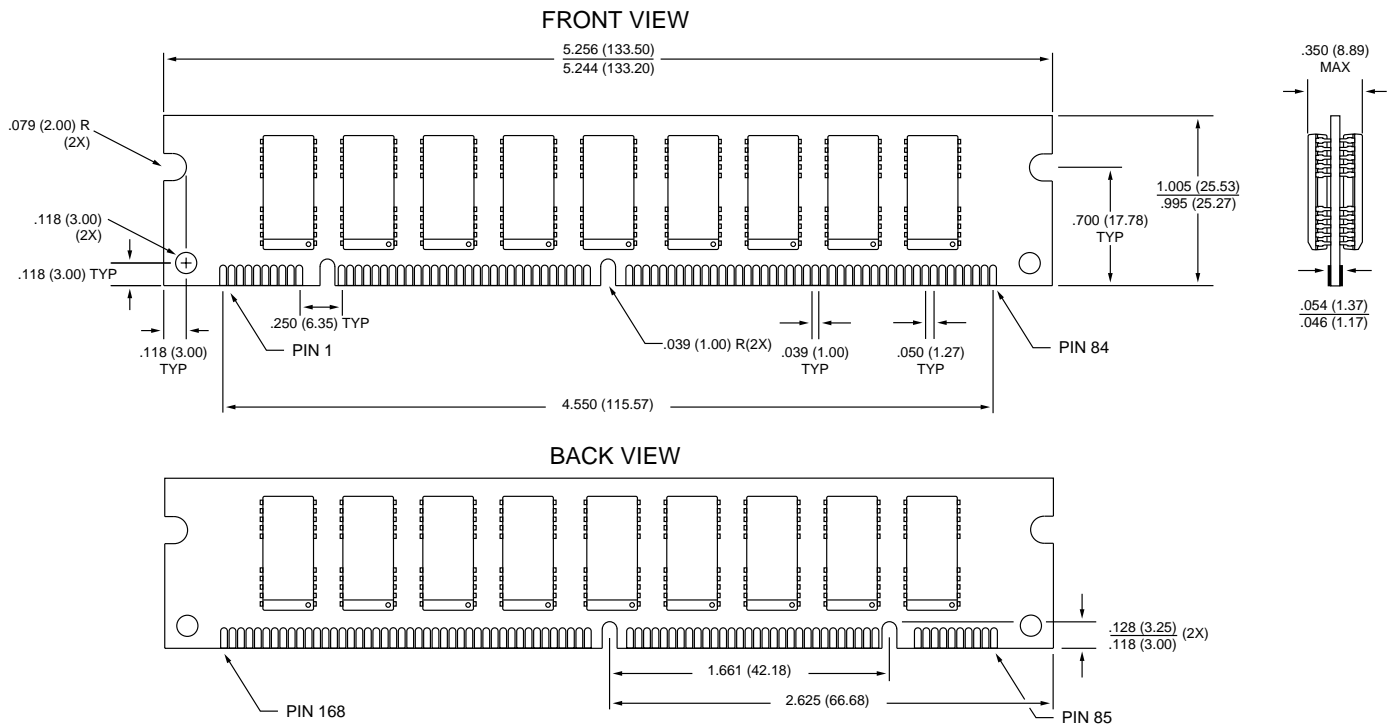


2, 4 MEG x 72
NONBUFFERED DRAM DIMMs

168-PIN DIMM DF-12 (16MB)



168-PIN DIMM DF-13 (32MB)



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.