
Integrated PC Camera Chip

*Scatch*TM

Sunplus Camera Solution

www.DataSheet4U.com

SPCA561A

Data Sheet

Version 0.2.0

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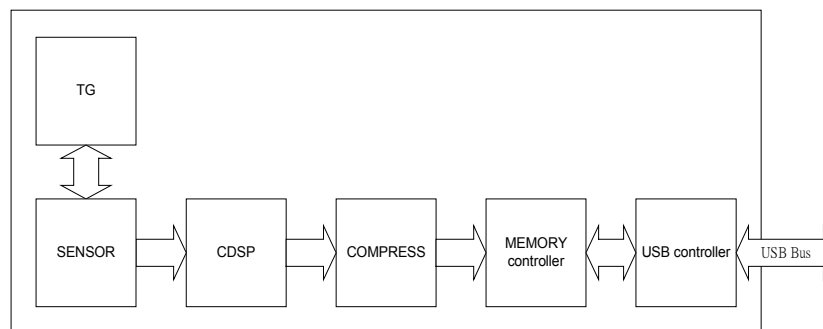
1. General Description

The SPCA561A provides a single chip solution to PC camera application. It includes a CIF format (352H x 288V) CMOS sensor and a backend processor for all image processing, image compression and data transaction units needed by a PC camera. The compressed data is transmitted to the PC side via the USB bus without external DRAM. In addition, the embedded USB controller is a hard-wired state machine. There is no need to use external microprocessors.

2. Features

1. Embedded 1/5-inch CMOS image sensor with 352Hx288V sensor array structure
2. 7.8um x 7.8um active pixel photodiode-type with R, G, B, primary color filters.
3. Programmable sensor controls: window size, gain, frame rate and ADC reference.
4. Provide real-time and high-quality video formats :
 - 24 fps @ SQVGA (160x120) with 5.6 ~ 6 M bit/sec USB bandwidth
 - 24 fps @ QCIF (176x144) with 5.6 ~ 6 M bit/sec USB bandwidth
 - 14-16 fps @ QVGA (320x240) with 6.8 M bit/sec USB bandwidth
 - 14-16 fps @ CIF (352x288) with 6.8 M bit/sec USB bandwidth
5. Video processing :
 - Bad pixels concealment
 - White balance measurement and gain parameter control
 - Exposure and sharpness measurement
6. Support USB Suspend mode
7. USB Vendor ID, Product ID, device release number, maximum power consumption and the string descriptor index and data selectable via an serial EEPROM (93C66) or internal ROM
8. 3.3 Volt power supply.
9. 48 pins PLCC package

3. Block Diagram



The TG block receives timing signals from the CMOS sensor and generates all the synchronization signals needed inside the SPCA561A, while the CDSP block receives and processes image data from the sensor. The image data is then further compressed by the Compression block and directly transmitted to the USB bus via the USB controller. The detailed function of each block is described in the following subsections.