凌陽科技
SUNPLUS

DATA SHEET

SPC41A1

40KB Sound Controller

SEP. 04, 2001

Version 1.3

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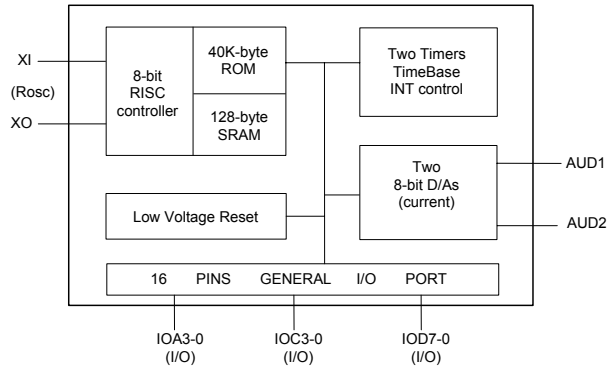
40KB SOUND CONTROLLER

1. GENERAL DESCRIPTION

The SPC41A1 is a CPU based two-channel speech/melody synthesizer including CMOS 8-bit microprocessor with 69 instructions, 40K-byte ROM for speech and melody data (Speech is compressed by a 4-bit ADPCM with approx. 13 sec speech duration @ 6KHz sampling rate) and 128-byte working SRAM. It includes two Timer/Counters, 16 Software Selectable I/Os, and two 8-bit current output (D/A). For audio processing, melody and speech can be mixed into one output. It operates over a wide voltage range of 2.4V - 5.5V and includes Low Voltage Reset function. The Low Voltage Reset automatically resets when the working voltage is less than 2.2V. In addition, SPC41A1 has a Clock Stop mode for power savings. The power savings mode saves the RAM contents, but freezes the oscillator, causing all other chip functions to be inoperative. The Max. CPU clock frequency is 6.0MHz. It has an Instruction Cycle Rate of 2 clock cycles (min.) - 6 clock cycles (max.). The SPC41A1 includes, not only the latest technology, but also the full commitment and technical support of Sunplus.

2. BLOCK DIAGRAM



3. FEATURES

- 8-bit microprocessor
- **Provides 40K-byte ROM for program and audio data**
- 128-byte working SRAM
- Software-based audio processing
- Wide operating voltage: 2.4V - 3.6V @ 4.0MHz
  3.6V - 5.5V @ 6.0MHz
- Supports Crystal Resonator or Rosc (with Mask option)
- Max. CPU clock: 4.0MHz @ 2.4V - 3.6V
  6.0MHz @ 3.6V - 5.5V
- Standby mode (Clock Stop mode) for power savings.
  Max. 2μA @ 5.0V
- 500ns instruction cycle time @ 4.0MHz CPU clock
- **Provides 16 general I/Os**
- Two 12-bit timer/counters
- 6 INT sources
- Key wake-up function
- **Approx. 13 sec speech**
  @ 6KHz sampling rate with 4-bit ADPCM
- **Two 8-bit current output (D/A)**
- **Low Voltage Reset**

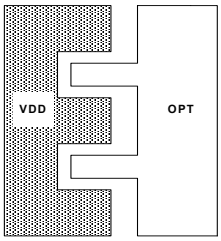
4. APPLICATION FIELD

- Intelligent education toys
  Ex. Pattern to voice (animal, car, color, etc.)
  Spelling (English or Chinese)
  Math
- High end toy controller
- Talking instrument controller
- General speech synthesizer
- Industrial controller

5. SIGNAL DESCRIPTIONS**

Mnemonic	PIN No.	Type	Description
VDD	12	I	Logic and I/O VDD
VSS	5	I	Logic GND
	11		I/O GND
XI	15	I	Oscillator crystal input or RESISTOR (Resistor should be connected to VDD)
XO	14	O	Oscillator crystal output
*OPT	13	I	ROSC option, connect to VDD
RESET	6	I	This pin is an active low reset for the chip
TEST	18	I	TEST MODE
AUD1	16	O	AUDIO OUTPUT
AUD2	17		
IOA0	4	I/O	Port A is a 4-bit bi-directional Input / Output port with Pull-high or Open-drain option. As inputs, Port A can be in either the Pure or Pull-high states. As outputs Port A can be a Buffer type or Open-drain type. Port A3 - 0 are Open-drain NMOS type (Sink current). **See note 1 and 2 below.
IOA1	3	I/O	
IOA2	2	I/O	
IOA3	1	I/O	
IOC0	10	I/O	Port C is a 4-bit bi-directional Input / Output port with Pull-high or Open-drain option. As inputs, Port C can be in either the Pure or Pull-high states. As outputs Port C can be a Buffer type or Open-drain type. Port C3 - 0 are Open-drain NMOS type (Sink current). **See note 1 and 2 below.
IOC1	9	I/O	
IOC2	8	I/O	
IOC3	7	I/O	
IOD0	26	I/O	Port D is an 8-bit bi-directional Input / Output port with Pull-low or Open-drain option. As inputs, Port D can be either buffer or Open-drain PMOS (Send current). Also, Port D can be software programmed for wake-up I/O pins. (Programmable I/O, Key Change, Wake-up I/O). **See note 1 and 2 below.
IOD1	25	I/O	
IOD2	24	I/O	
IOD3	23	I/O	
IOD4	22	I/O	
IOD5	21	I/O	
IOD6	20	I/O	
IOD7	19	I/O	

* OPT is the selection pin for ROSC or X'TAL. The shape looks like in the right figure. When ROSC is selected, OPT is connected to VDD and if X'TAL is selected, OPT is floating. The reason of OPT near by VDD is that when ROSC is selected, it is easy to make connection between VDD and OPT.



** Refer to SPC Programming Guide for complete information.

***Note:** 1). Two input states can be specified; Pure Input, Pull-High or Pull Low.

2). Three output states can be specified, Buffer output, Open Drain PMOS output <send>, Open Drain NMOS output <sink>.

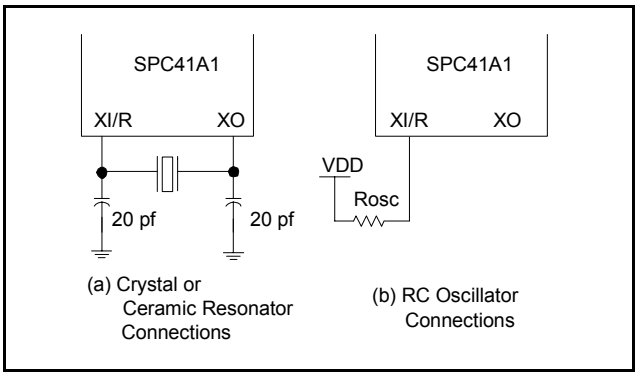
6. FUNCTIONAL DESCRIPTIONS

6.1. CPU

The 8-bit micro-processor of SPC41A1 is a high performance processor equipped with Accumulator, Program Counter, X Register, Stack pointer and Processor Status Register (this is the same as the 6502 instruction structure). SPC41A1 is able to perform with 6.0MHz (max.) depending on the application specifications.

6.2. Oscillator

The SPC41A1 supports AT-cut parallel resonant oscillated Crystal / Resonator or RC Oscillator or external clock sources by mask option (select one from those three types). The design of application circuit should follow the vendors' specifications or recommendations. The diagrams listed below are typical X'TAL/ROSC circuits for most applications:



(a) Crystal or Ceramic Resonator Connections

(b) RC Oscillator Connections

6.3. Bonding Option

The SPC41A1 has the following bonding option:

- Supports Crystal Resonator or Rosc (with bonding option).

6.4. ROM Area

The SPC41A1 provides a 40K-byte ROM that can be defined as the program area, audio data area, or both. To access ROM, users should program the BANK SELECT Register, choose bank, and access address to fetch data.

6.5. RAM Area

The total RAM consists of 128 bytes (including Stack) at locations from $80 through $FF.

6.6. Map of Memory and I/Os

*I/O PORT:

– PORT IOA $0002
IOC $0004
IOD $0005

– I/O CONFIG $0000
$0001

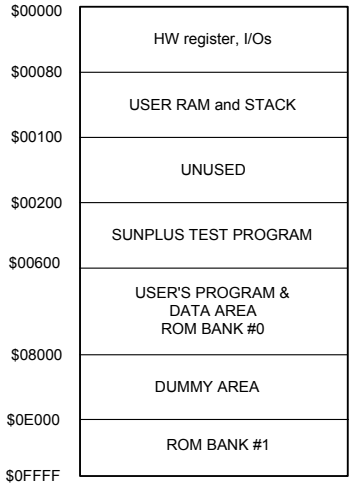
*NMI SOURCE:

– INTA (from TIMER A)

*INT SOURCE:

– INTA (from TIMER A)
– INTB (from TIMER B)
– CPU CLK / 1024
– CPU CLK / 8192
– CPU CLK / 65536
– EXT INT

*MEMORY MAP (From ROM view)



6.7. Speech and Melody

Since the SPC41A1 provides a large ROM and wide range of CPU operation speeds, it is most suitable for speech and melody synthesis. For speech synthesis, the SPC41A1 can provide NMI for accurate sampling frequency. Users can record or synthesize the sound and digitize it into the ROM. The sound data can be played back in the sequence of the control functions as designed by the user's program. Several algorithms are recommended for high fidelity and compression of sound including PCM, LOG PCM, and ADPCM. For melody synthesis, the SPC41A1 provides dual tone mode. Once the SPC41A1 enters the dual tone mode, users only need to fill either TMA or TMB, or both TMA and TMB to the tone frequency for each channel, and count the envelope of each channel. The hardware will toggle the tone wave automatically without INT.

6.8. Power Savings Mode

The SPC41A1 provides a power savings mode (Standby mode) for those applications that require very low stand-by current. To enter standby mode, the Wake-Up Register should be enabled and then stop the CPU clock by writing the STOP CLOCK Register. The CPU will then go to the stand-by mode. In such a mode, RAM and I/Os will remain in their previous states until being awoken. Port IOD7-0 is the only wake-up source in the SPC41A1. After the SPC41A1 is awoken, the internal CPU will go to the RESET State (Tw ≧ 65536 x T1) and then continue processing the program. Wakeup Reset will not affect RAM or I/Os (FIG.1).

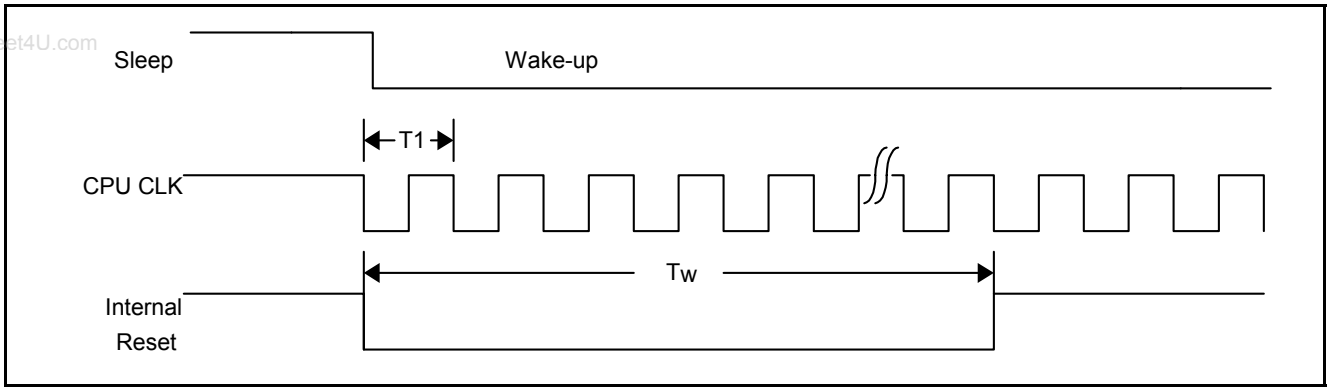
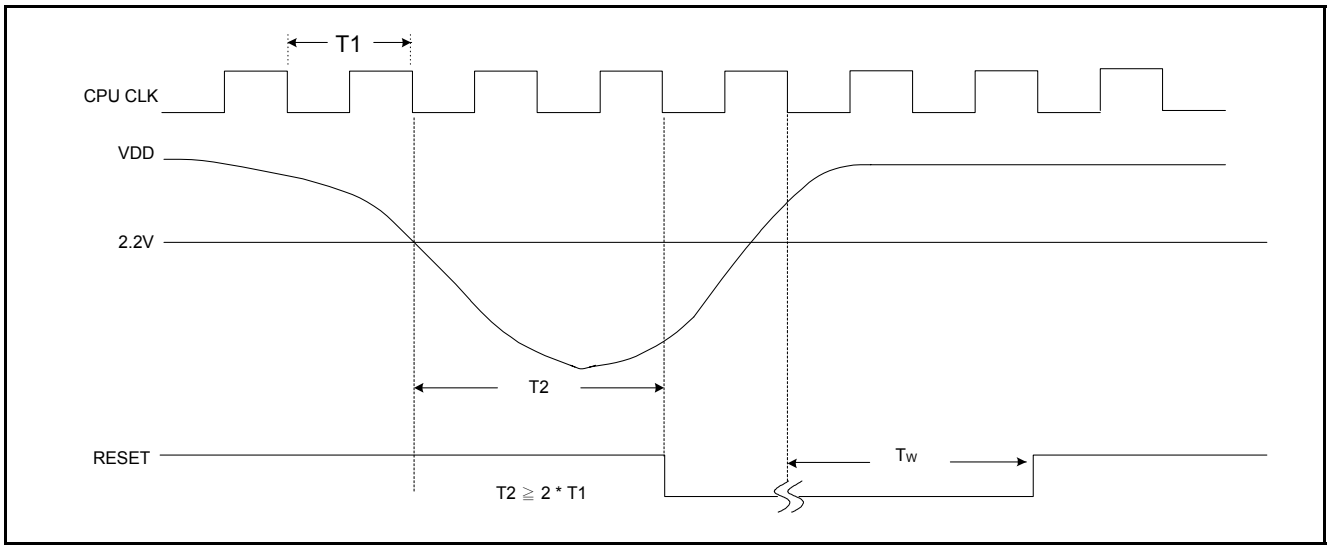


FIG. 1

$T1 = 1 / (F_{CPU})$, Tw ≧ 65536 x T1

6.9. Low Voltage Reset

The SPC41A1 includes a Low Voltage Reset (LVR) function. Below the minimum power-supply voltage of 2.2V, the CPU system will become unstable and malfunction. Low Voltage Reset will reset all functions into the initial operational (stable) state if the VDD power-supply voltage drops below 2.2V (FIG.2).



(The LVR function is the same as Power ON Reset or External Reset.)

FIG. 2

6.10. Timer/Counter

The SPC41A1 contains two 12-bit timer/counters, TMA and TMB respectively. TMA can be specified as a timer or a counter, but TMB can only be used as a timer. In the timer mode, TMA and TMB are re-loaded up-counters. When timer overflows from $0FFF to $0000, the carry signal will make the timer automatically reload to the user's pre-set value and be up-counted again. At the same time, the carry signal will generate the INT signal if the corresponding bit is enabled in the INT ENABLE Register. If TMA is specified as a counter, users can reset by loading #0 into the counter. After the counter has been activated, the value of the counter can also be read from the counters at the same time.

Clock source of Timer/Counter can be selected as follows:

Timer/Counter		Clock Source
TMA	12-BIT TIMER	CPU CLOCK (T) or T/4
	12-BIT COUNTER	T/64, T/8192, T/65536 or EXT CLK
TMB	12-BIT TIMER	T or T/4
MODE SELECT REGISTER		TMA only, select timer or counter
TIMER CLOCK SELECTOR		Select T or T/4

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

7.2. AC Characteristics (T_A = 25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
CPU Clock	F_{CPU}	-	2.0	4.0	MHz	VDD = 2.4V - 3.6V, 2-battery
		-	4.0	6.0	MHz	VDD = 3.6V - 5.5V, 3-battery

7.3. DC Characteristics (VDD = 3.0V, T_A = 25℃)

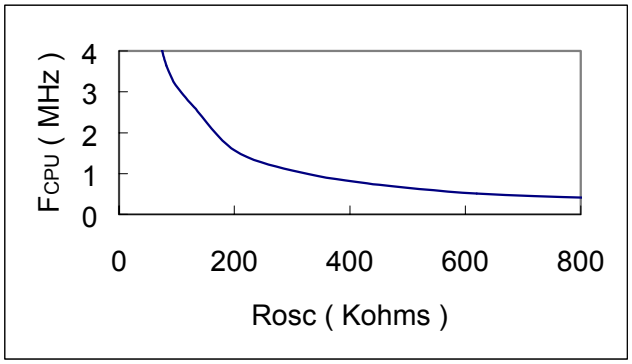
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	3.6	V	For 2-battery
Operating Current	I_{OP}	-	1.5	2.0	mA	F_{CPU} = 3.0MHz @ 3.0V, no load
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 3.0V
Audio output current	I_{AUD}		-1.6		mA	VDD = 3.0V, full-scale
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output High I IOA, IOC, IOD	I_{OH}	-1.0	-	-	mA	VDD = 3.0V V_{OH} = 2.0V
Output Sink I IOA, IOC, IOD	I_{OL}	2.0	-	-	mA	VDD = 3.0V V_{OL} = 0.8V
Input Resistor IOD	R_{IN}	-	100	-	Kohm	Pull Low VDD = 3.0V

7.4. DC Characteristics (VDD = 5.0V, T_A = 25℃)

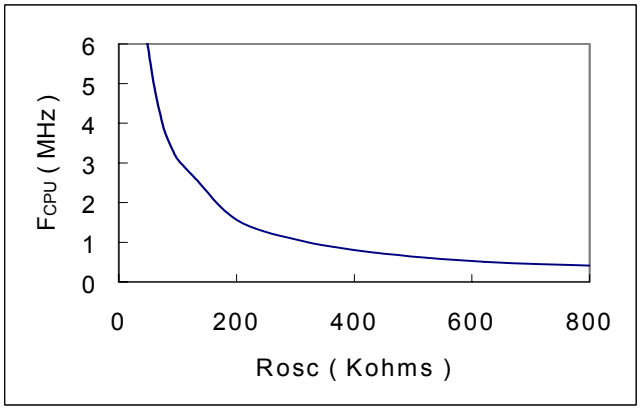
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	3.6	-	5.5	V	For 3-battery
Operating Current	I_{OP}	-	4.0	5.0	mA	F_{CPU} = 4.0MHz @ 5.0V, no load
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 5.0V
Audio output current	I_{AUD}	-	-3.0	-	mA	VDD = 5.0V, full-scale
Input High Level	V_{IH}	3.0	-	-	V	VDD = 5.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 5.0V
Output High I IOA, IOC, IOD	I_{OH}	-1.0	-	-	mA	VDD = 5.0V V_{OH} = 4.2V
Output Sink I IOA, IOC, IOD	I_{OL}	4.0	-	-	mA	VDD = 5.0V V_{OL} = 0.8V
Input Resistor IOD	R_{IN}	-	60	-	Kohm	Pull Low VDD = 5.0V

7.5. The Relationship between the R_{OSC} and the F_{CPU}

7.5.1. VDD = 3.0V, T_A = 25℃

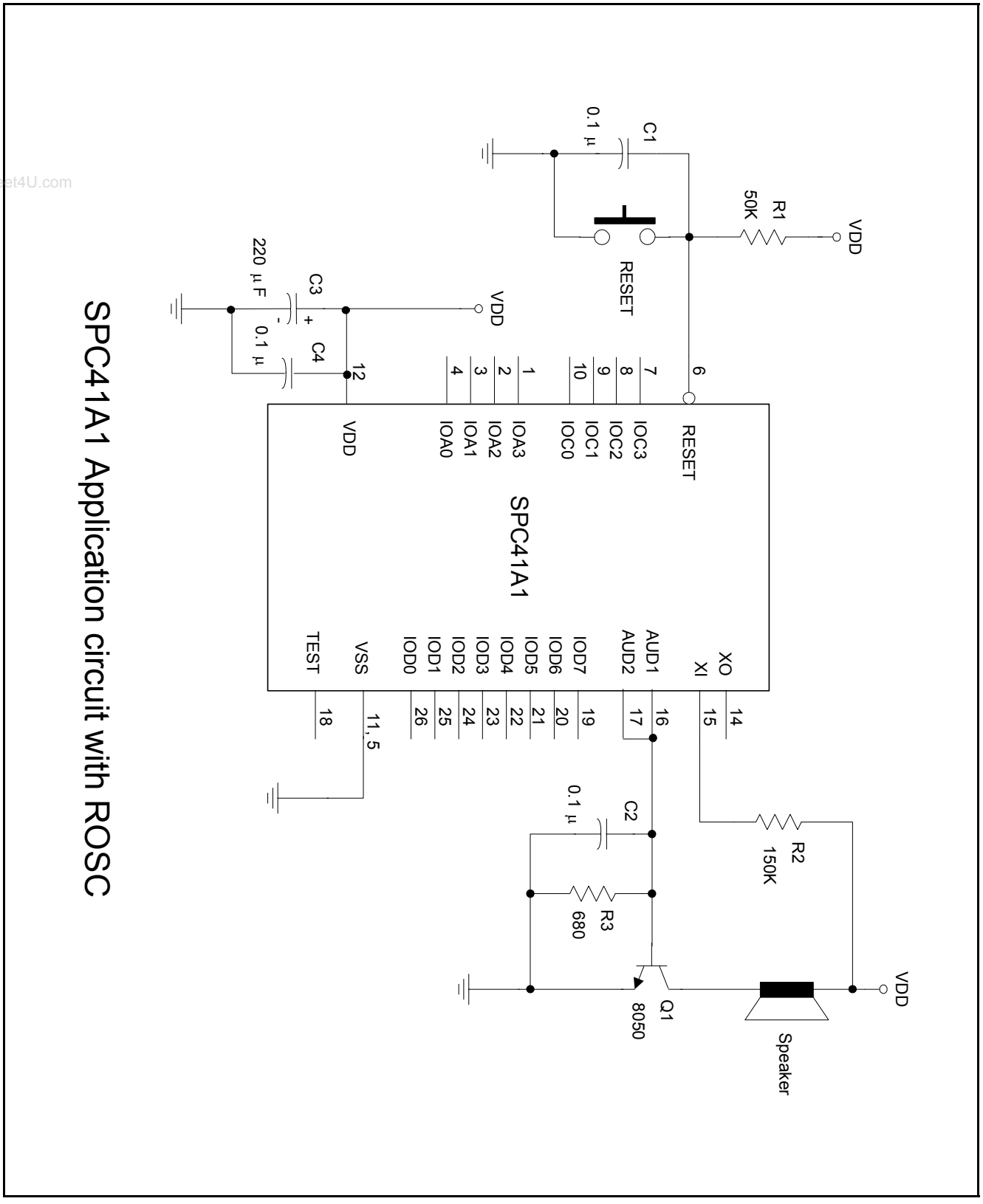


7.5.2. VDD = 4.5V, T_A = 25℃

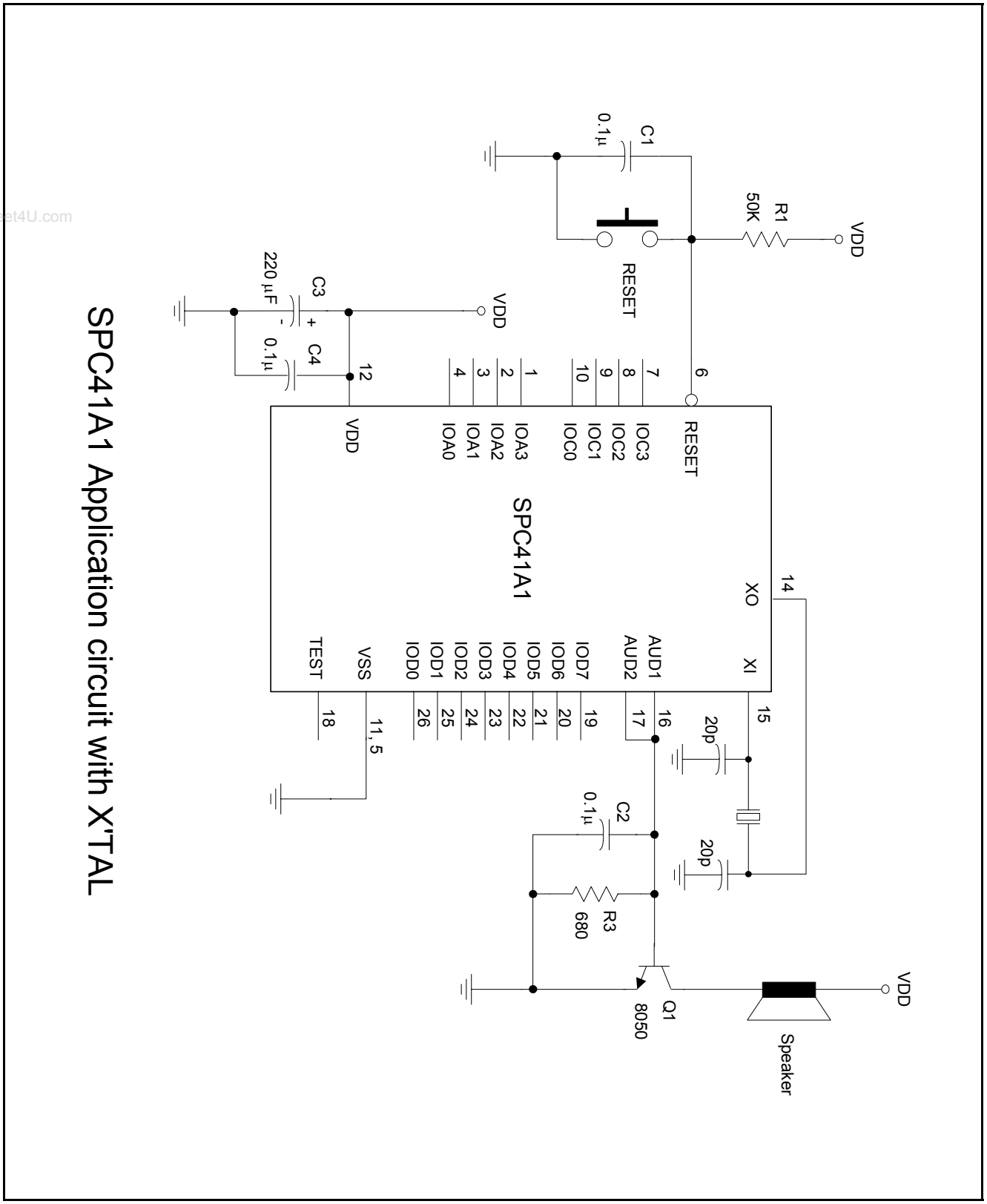


8. APPLICATION CIRCUITS

8.1. Application Circuit - (1)

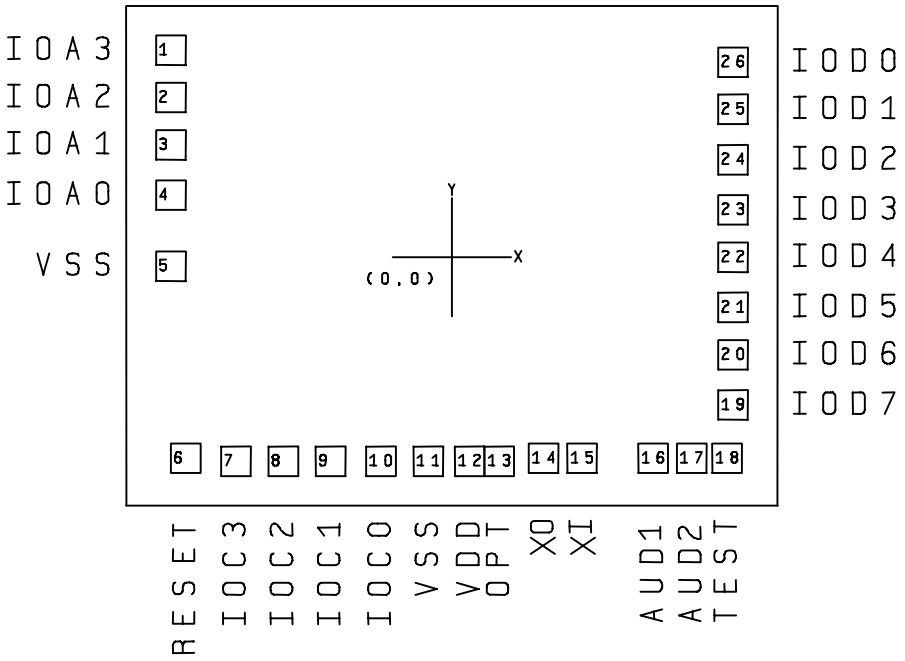


8.2. Application Circuit - (2)



9. PACKAGE/PAD LOCATIONS

9.1. PAD Assignment



Chip Size: 2330μm x 1820μm

This IC substrate should be connected to VSS

Note1: Chip size included scribe line.

Note2: To ensure that the IC functions properly, please bond all of VDD and VSS pins.

Note3: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

9.2. Ordering Information

Product Number	Package Type
SPC41A1-nnnnV-C	Chip form

Note1: Code number (nnnnV) is assigned for the customer.

Note2: Code number (nnnn=0000 - 9999); version (V=A - Z).

9.3. PAD Locations

PAD No.	PAD Name	X	Y
1	IOA3	-953	698
2	IOA2	-953	537
3	IOA1	-953	372
4	IOA0	-953	210
5	VSS	-953	-39
6	RESET	-901	-686
7	IOC3	-734	-698
8	IOC2	-569	-698
9	IOC1	-407	-698
10	IOC0	-242	-698
11	VSS	-81	-698
12	VDD	59	-698
13	OPT	157	-698
14	XO	314	-686
15	XI	440	-686
16	AUD1	676	-686
17	AUD2	807	-686
18	TEST	929	-686
19	IOD7	955	-501
20	IOD6	955	-332
21	IOD5	955	-170
22	IOD4	955	-1
23	IOD3	955	160
24	IOD2	955	330
25	IOD1	955	491
26	IOD0	955	660

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11. REVISION HISTORY

Date	Revision #	Description	Page
SEP. 02, 1999	0.1	Original	
NOV. 17, 1999	1.0	Delete "*PRELIMINARY*"	
FEB. 09, 2000	1.1	Add, The relationship between the Rosc and the Fcpu	
NOV. 08, 2000	1.2	1. VDD = 2.4V - 3.6V for 2-battery application 2. Speech duration @ 6KHz sampling rate with 4-bit ADPCM 3. Approx. 13 sec. speech.	
SEP. 04, 2001	1.3	1. Correct chip size 2. Add Note1 and Note3 in the "*9.s1 PAD Assignment*" 3. Renew to a new document format	12 12