BATTERY PROTECTION IC WITH CELL-BALANCE FUNCTION

S-8209B Series

The S-8209B Series is a protection IC for lithium-ion / lithium polymer rechargeable batteries and includes a high-accuracy voltage detection circuit and a delay circuit.
This IC has a transmission function and two types of cell-balance function so that users are also able to configure a protection circuit with series multi-cell.

■ Features

(1) High-accuracy voltage detection circuit

• Overcharge detection voltage[*1]	3.55 V to 4.40 V (5 mV step)	Accuracy ±25 mV
• Overcharge release voltage[*1]	3.50 V to 4.40 V[*2]	Accuracy ±50 mV
• Cell-balance detection voltage[*1]	3.55 V to 4.40 V (5 mV step)[*3]	Accuracy ±25 mV
• Cell-balance release voltage[*1]	3.50 V to 4.40 V[*4]	Accuracy ±50 mV
• Overdischarge detection voltage	2.0 V to 3.0 V (10 mV step)	Accuracy ±50 mV
• Overdischarge detection voltage	2.0 V to 3.4 V[*5]	Accuracy ±100 mV

(2) Settable delay time by external capacitor for output pin
(3) Control charging, discharging, cell-balance by CTLC, CTLD pins
(4) Two types of cell-balance function; charge/discharge[*6]
(5) Wide range of operation temperature −40°C to +85°C
(6) Low current consumption 7.0 μA max.
(7) Small package SNT-8A, 8-Pin TSSOP
(8) Lead-free product

***1.** Regarding selection of overcharge detection voltage, overcharge release voltage, cell-balance detection voltage and cell-balance release voltage, refer to remark in "■ **Product Name Structure**, **2. Product Name list**".
***2.** Overcharge release voltage = Overcharge detection voltage − Overcharge hysteresis voltage
(Overcharge hysteresis voltage is selectable in 0 V to 0.4 V in 50 mV step.)
***3.** Select as to overcharge detection voltage > cell-balance detection voltage.
***4.** Cell-balance release voltage = Cell-balance detection voltage − Cell-balance hysteresis voltage
(Cell-balance hysteresis voltage is selectable in 0 V to 0.4 V in 50 mV step.)
***5.** Overdischarge release voltage = Overdischarge detection voltage + Overdischarge hysteresis voltage
(Overdischarge hysteresis voltage is selectable in 0 V to 0.7 V in 100 mV step.)
***6.** Also available the product without discharge cell-balance function

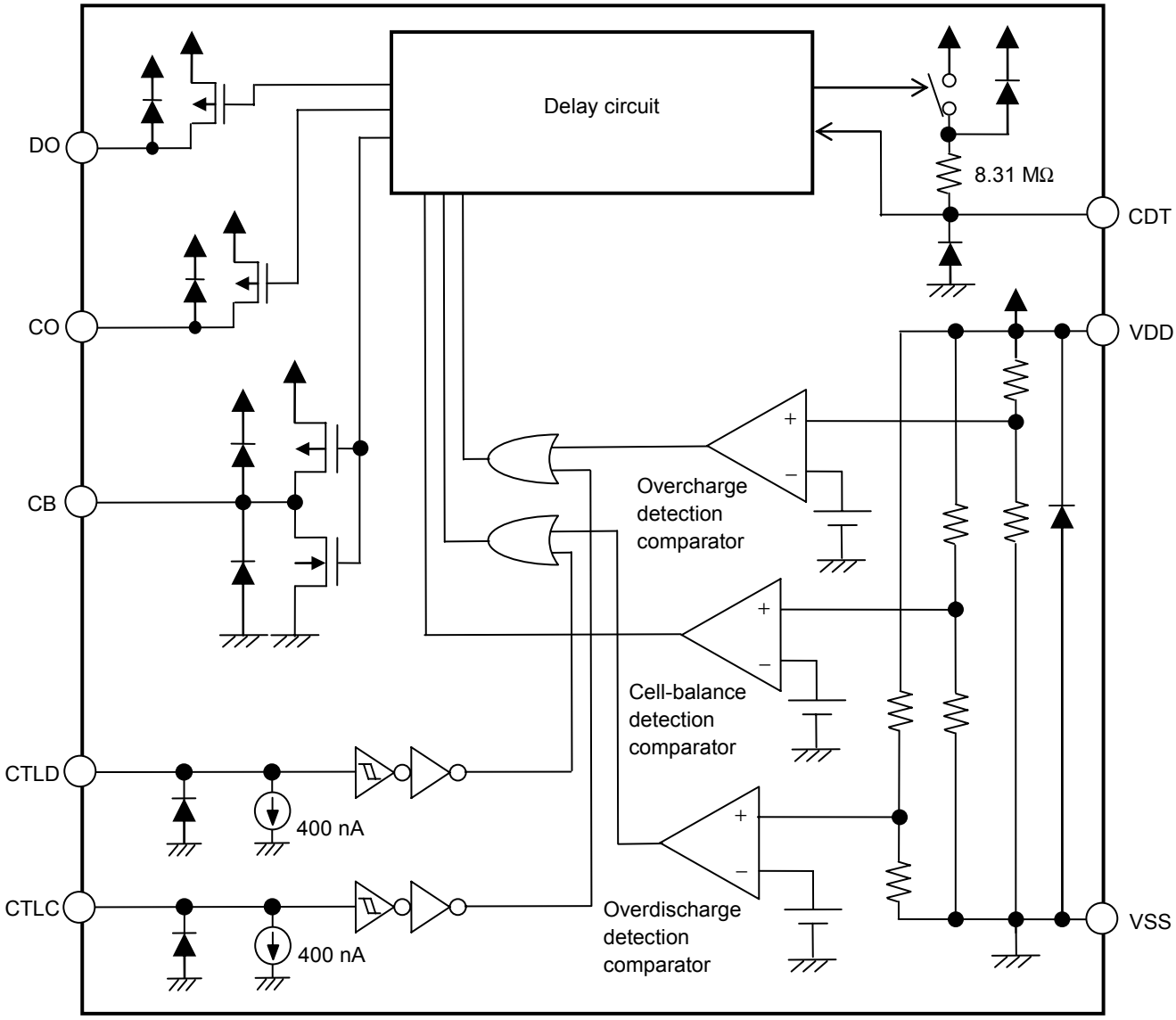
■ Applications

- Lithium-ion rechargeable battery packs
- Lithium polymer rechargeable battery packs

■ Packages

Package Name	Drawing Code			
	Package	Tape	Reel	Land
SNT-8A	PH008-A	PH008-A	PH008-A	PH008-A
8-Pin TSSOP	FT008-A	FT008-E	FT008-E	−

■ Block Diagram



Remark The diodes in the IC are parasitic diodes.

Figure 1

■ Product Name Structure

1. Product Name

(1) SNT-8A

S-8209B XX - I8T1 G

- XX: Serial code — Sequentially set from AA to ZZ
- I8T1: IC direction of tape specifications*1 — I8T1 : SNT-8A, Tape

1. Refer to the tape specifications at the end of this book.

(2) 8-Pin TSSOP

S-8209B XX - T8T1 S

- XX: Serial code — Sequentially set from AA to ZZ
- T8T1: IC direction of tape specifications*1 — T8T1 : 8-Pin TSSOP, Tape

1. Refer to the tape specifications at the end of this book.

2. Product Name List

(1) SNT-8A

Table 1

Product name / Item	Overcharge detection voltage*1 (V_{CU})	Overcharge release voltage (V_{CL})	Cell-balance detection voltage*1 (V_{BU})	Cell-balance release voltage (V_{BL})	Overdischarge detection voltage (V_{DL})	Overdischarge release voltage (V_{DU})	Discharge cell-balance function
S-8209BAA-I8T1G	4.100 V	4.000 V	4.050 V	4.000 V	2.50 V	2.70 V	Yes

(2) 8-Pin TSSOP

Table 2

Product name / Item	Overcharge detection voltage*1 (V_{CU})	Overcharge release voltage (V_{CL})	Cell-balance detection voltage*1 (V_{BU})	Cell-balance release voltage (V_{BL})	Overdischarge detection Voltage (V_{DL})	Overdischarge release voltage (V_{DU})	Discharge cell-balance function
S-8209BAA-T8T1S	4.100 V	4.000 V	4.050 V	4.000 V	2.50 V	2.70 V	Yes

Remark Please contact our sales office for the products with detection voltage value other than those specified above.
Users are able to select the overcharge detection voltage, overcharge release voltage, cell-balance detection voltage and cell-balance release voltage from the range shown in **Figure 2** and **3**.
Users are able to select how to combine the overcharge detection voltage (V_{CU}) and the overcharge release voltage (V_{CL}) from the range A or B shown in **Figure 2**[*1].
Similarly, select how to combine the cell-balance detection voltage (V_{BU}) and the cell-balance release voltage (V_{BL}) from the range of C or D in **Figure 3**[*2].
In selecting the combination of V_{CU} and V_{CL} from the range A, select the combination of V_{BU} and V_{BL} from the range C. Similarly, in selecting the combination of V_{CU} and V_{CL} from the B range, select the combination of V_{BU} and V_{BL} from the range D[*3].

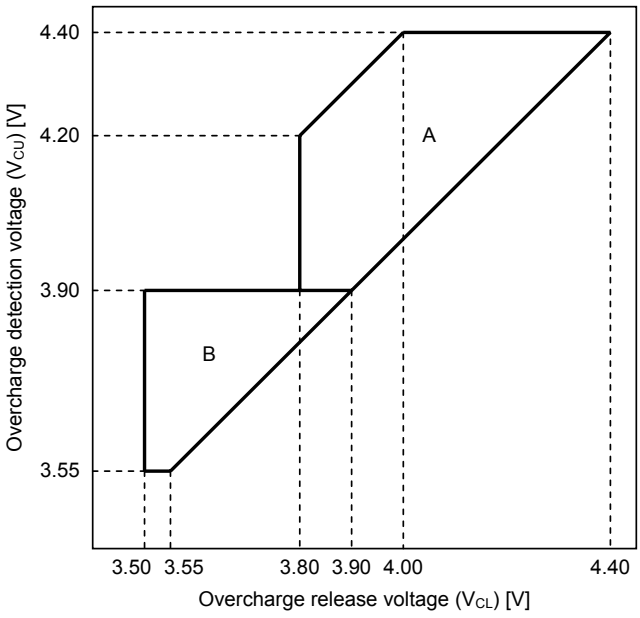


Figure 2

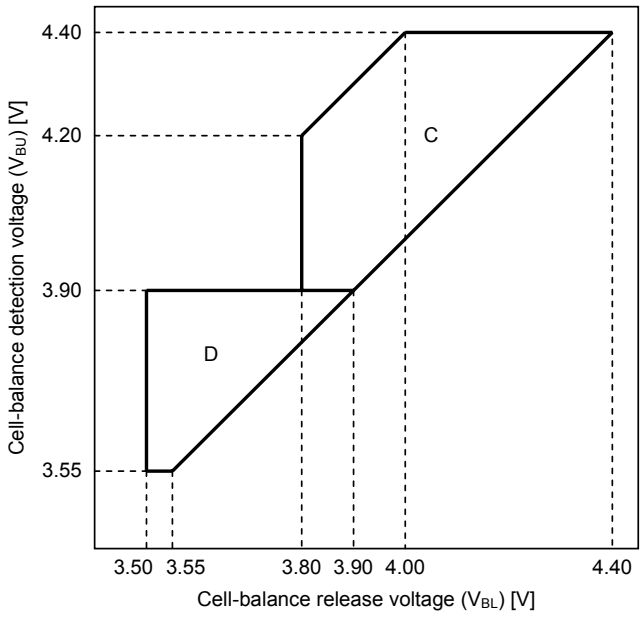


Figure 3

***1.** Users are able to select the overcharge hysteresis voltage ($V_{CU} - V_{CL}$) in 0 V to 0.4 V, in 50 mV step.
***2.** Users are able to select the cell-balancce hysteresis voltage ($V_{BU} - V_{BL}$) in 0 V to 0.4 V, in 50 mV step.
***3.** Select as to set $V_{CU} > V_{BU}$.

■ Pin Configurations

SNT-8A
Top view

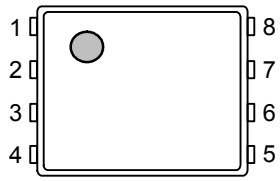


Figure 4

Table 3

Pin No.	Symbol	Description
1	CTLC	Pin for charge control
2	CTLD	Pin for dischage control
3	VDD	Connection pin for input positive power supply, for battery's positive voltage
4	CDT	Connection pin to capacitor for overcharge detection delay, for overdischarge detection delay
5	VSS	Input pin for negative power supply, Connection pin for battery's negative voltage
6	DO	Output pin for discharge control (Pch open drain output)
7	CO	Output pin for charge control (Pch open drain output)
8	CB	Output pin for cell-balance control (CMOS output)

Remark For the external views, refer to the package drawings.

8-Pin TSSOP
Top view

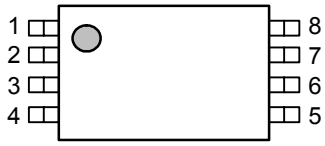


Figure 5

Table 4

Pin No.	Symbol	Description
1	CTLC	Pin for charge control
2	CTLD	Pin for dischage control
3	VDD	Connection pin for input positive power supply, for battery's positive voltage
4	CDT	Connection pin to capacitor for overcharge detection delay, for overdischarge detection delay
5	VSS	Input pin for negative power supply, Connection pin for battery's negative voltage
6	DO	Output pin for discharge control (Pch open drain output)
7	CO	Output pin for charge control (Pch open drain output)
8	CB	Output pin for cell-balance control (CMOS output)

Remark For the external views, refer to the package drawings.

■ Absolute Maximum Ratings

Table 5

(Ta = 25°C unless otherwise specified)

Item		Symbol	Applied pin	Absolute Maximum Ratings	Unit
Input voltage between VDD and VSS		V_{DS}	VDD	V_{SS}–0.3 to V_{SS}+12	V
CB pin output voltage		V_{CB}	CB	V_{SS}–0.3 to V_{DD}+0.3	V
CDT pin voltage		V_{CDT}	CDT	V_{SS}–0.3 to V_{DD}+0.3	V
DO pin output voltage		V_{DO}	DO	V_{DD}–24 to V_{DD}+0.3	V
CO pin output voltage		V_{CO}	CO	V_{DD}–24 to V_{DD}+0.3	V
CTLC pin input voltage		V_{CTLC}	CTLC	V_{SS}–0.3 to V_{SS}+24	V
CTLD pin input voltage		V_{CTLD}	CTLD	V_{SS}–0.3 to V_{SS}+24	V
Power dissipation	SNT-8A	P_D	–	450[*1]	mW
	8-Pin TSSOP			700[*1]	mW
Operating ambient temperature		T_{opr}	–	–40 to +85	°C
Storage temperature		T_{stg}	–	–55 to +125	°C

***1.** When mounted on board

[Mounted board]

(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm

(2) Board name: JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

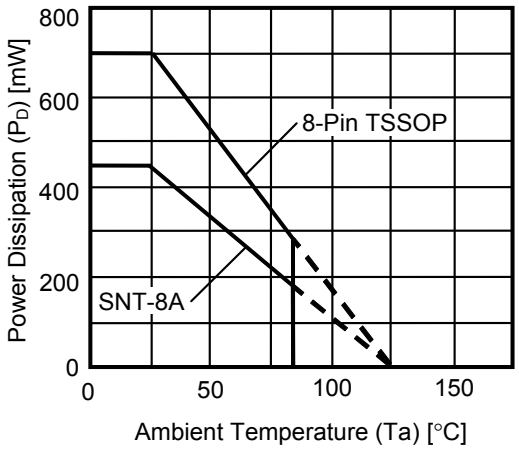


Figure 6 Power Dissipation of Package (When mounted on board)

■ Electrical Characteristics

Table 6

(Ta = 25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test circuit
Overcharge detection voltage	V_{CU}	–	V_{CU} −0.025	V_{CU}	V_{CU} +0.025	V	1
Overcharge release voltage	V_{CL}	–	V_{CL} −0.05	V_{CL}	V_{CL} +0.05	V	1
Cell-balance detection voltage	V_{BU}	–	V_{BU} −0.025	V_{BU}	V_{BU} +0.025	V	1
Cell-balance release voltage	V_{BL}	–	V_{BL} −0.05	V_{BL}	V_{BL} +0.05	V	1
Overdischarge detection voltage	V_{DL}	–	V_{DL} −0.05	V_{DL}	V_{DL} +0.05	V	1
Overdischarge release voltage	V_{DU}	–	V_{DU} −0.10	V_{DU}	V_{DU} +0.10	V	1
CDT pin resistance*1	R_{CDT}	V_{DS} = 3.5 V, V_{CDT} = 0 V	4.76	8.31	10.9	MΩ	2
CDT pin detection voltage*1	V_{CDET}	V_{DS} = 3.5 V	V_{DS} ×0.65	V_{DS} ×0.70	V_{DS} ×0.75	V	3
Operating voltage between VDD and VSS	V_{DSOP}	Output voltage of CO, DO, CB fixed	1.5	–	8.0	V	–
CTLC pin H voltage	V_{CTLCH}	V_{DS} = 3.5 V	V_{DS} ×0.55	–	V_{DS} ×0.90	V	4
CTLD pin H voltage	V_{CTLDH}	V_{DS} = 3.5 V	V_{DS} ×0.55	–	V_{DS} ×0.90	V	4
CTLC pin L voltage	V_{CTLCL}	V_{DS} = 3.5 V	V_{DS} ×0.10	–	V_{DS} ×0.45	V	4
CTLD pin L voltage	V_{CTLDL}	V_{DS} = 3.5 V	V_{DS} ×0.10	–	V_{DS} ×0.45	V	4
Current consumption during operation*2	I_{OPE}	V_{DS} = 3.5 V	–	3.5	7.0	μA	5
Sink current CTLC*2	I_{CTLCL}	V_{DS} = 3.5 V, V_{CTLC} = 3.5 V	320	400	480	nA	6
Sink current CTLD*2	I_{CTLDL}	V_{DS} = 3.5 V, V_{CTLD} = 3.5 V	320	400	480	nA	6
Source current CB	I_{CBH}	V_{CB} = 4.0 V, V_{DS} = 4.5 V	30	–	–	μA	7
Sink current CB	I_{CBL}	V_{CB} = 0.5 V, V_{DS} = 3.5 V	30	–	–	μA	7
Source current CO	I_{COH}	V_{CO} = 3.0 V, V_{DS} = 3.5 V	30	–	–	μA	7
Leakage current CO	I_{COL}	V_{CO} = 24 V, V_{DS} = 4.5 V	–	–	0.1	μA	8
Source current DO	I_{DOH}	V_{DO} = 3.0 V, V_{DS} = 3.5 V	30	–	–	μA	7
Leakage current DO	I_{DOL}	V_{DO} = 24 V, V_{DS} = 1.8 V	–	–	0.1	μA	8

***1.** In the S-8209B Series, users are able to set delay time for the output pins. By using the following formula, delay time is calculated with the value of CDT pin's resistance in the IC (R_{CDT}) and the value of capacitor set externally at the CDT pin (C_{CDT}).

t_D [s] = –ln (1–V_{CDET} / V_{DS}) × C_{CDT} [μF] × R_{CDT} [MΩ]
= –ln (1–0.7 (Typ.)) × C_{CDT} [μF] × 8.31 MΩ (Typ.)
= 10.0 MΩ (Typ.) × C_{CDT} [μF]

In case of the capacitance of CDT pin C_{CDT} = 0.01 μF, the output pin delay time t_D is calculated by using the above formula and as follows.

t_D [s] = 10.0 MΩ (Typ.) × 0.01 μF = 0.1 s (Typ.)

Test R_{CDT} and the CDT pin detection voltage (V_{CDET}) by test circuits shown in this datasheet after applying the power supply while pulling-up the CTLC, CTLD pins to the level of VDD pin outside the IC.

***2.** In case of using CTLC, CTLD pins pulled-up to the level of VDD pin externally, the current flows from the VSS pin (I_{SS}) is calculated by the following formula.

I_{SS} = I_{OPE} + I_{CTLCL} + I_{CTLDL}

■ Test Circuits

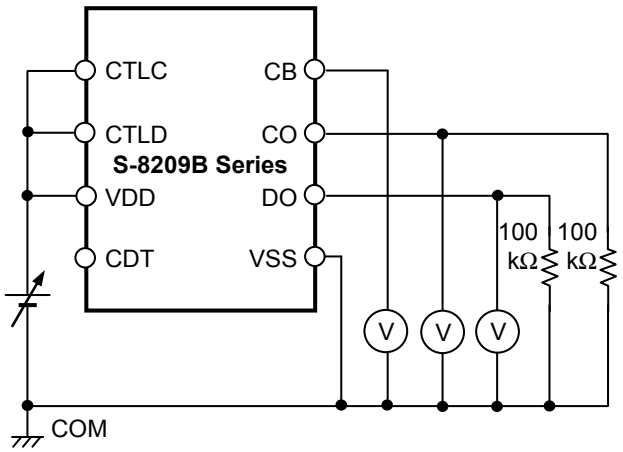


Figure 7 Test circuit 1

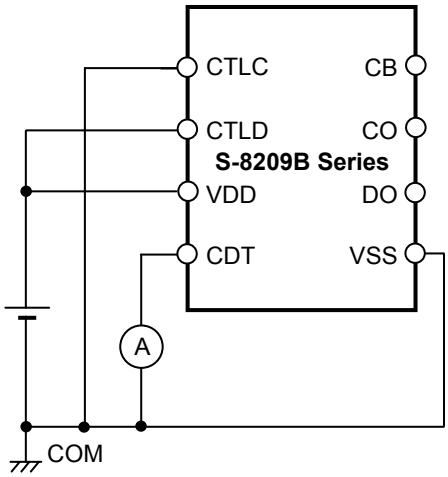


Figure 8 Test circuit 2

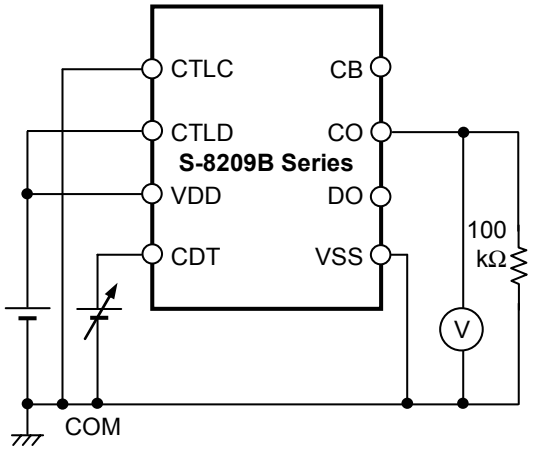


Figure 9 Test circuit 3

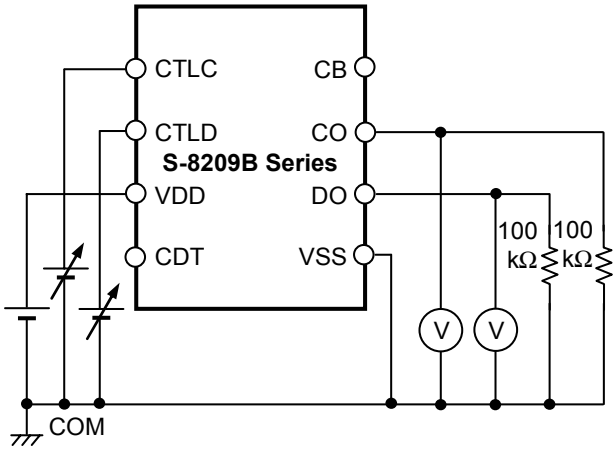


Figure 10 Test circuit 4

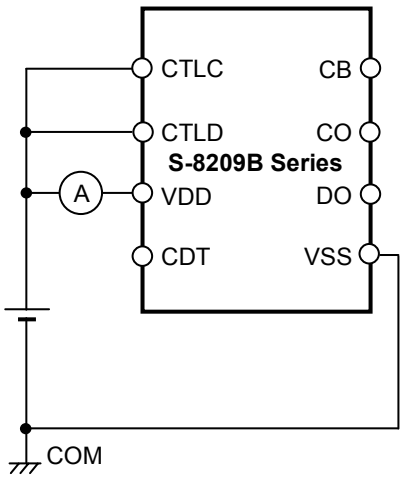


Figure 11 Test circuit 5

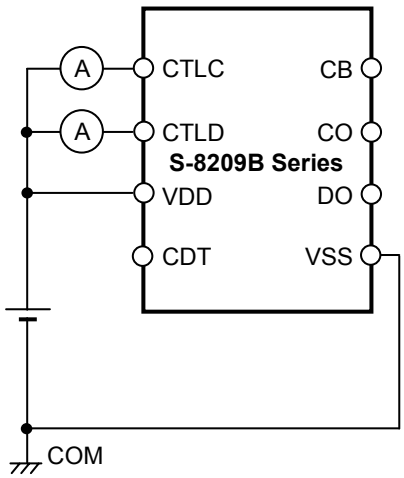


Figure 12 Test circuit 6

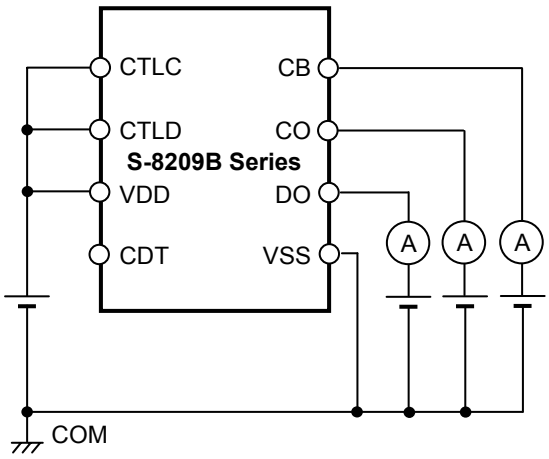


Figure 13 Test circuit 7

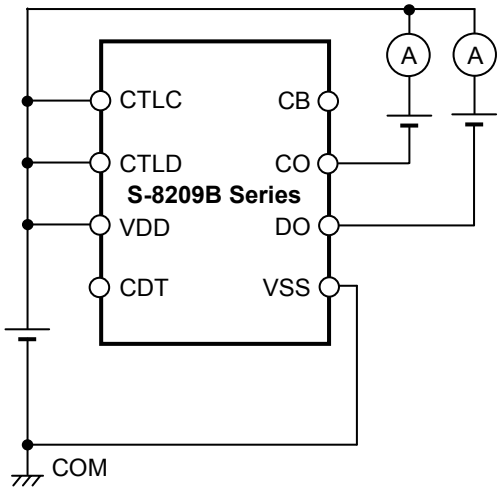
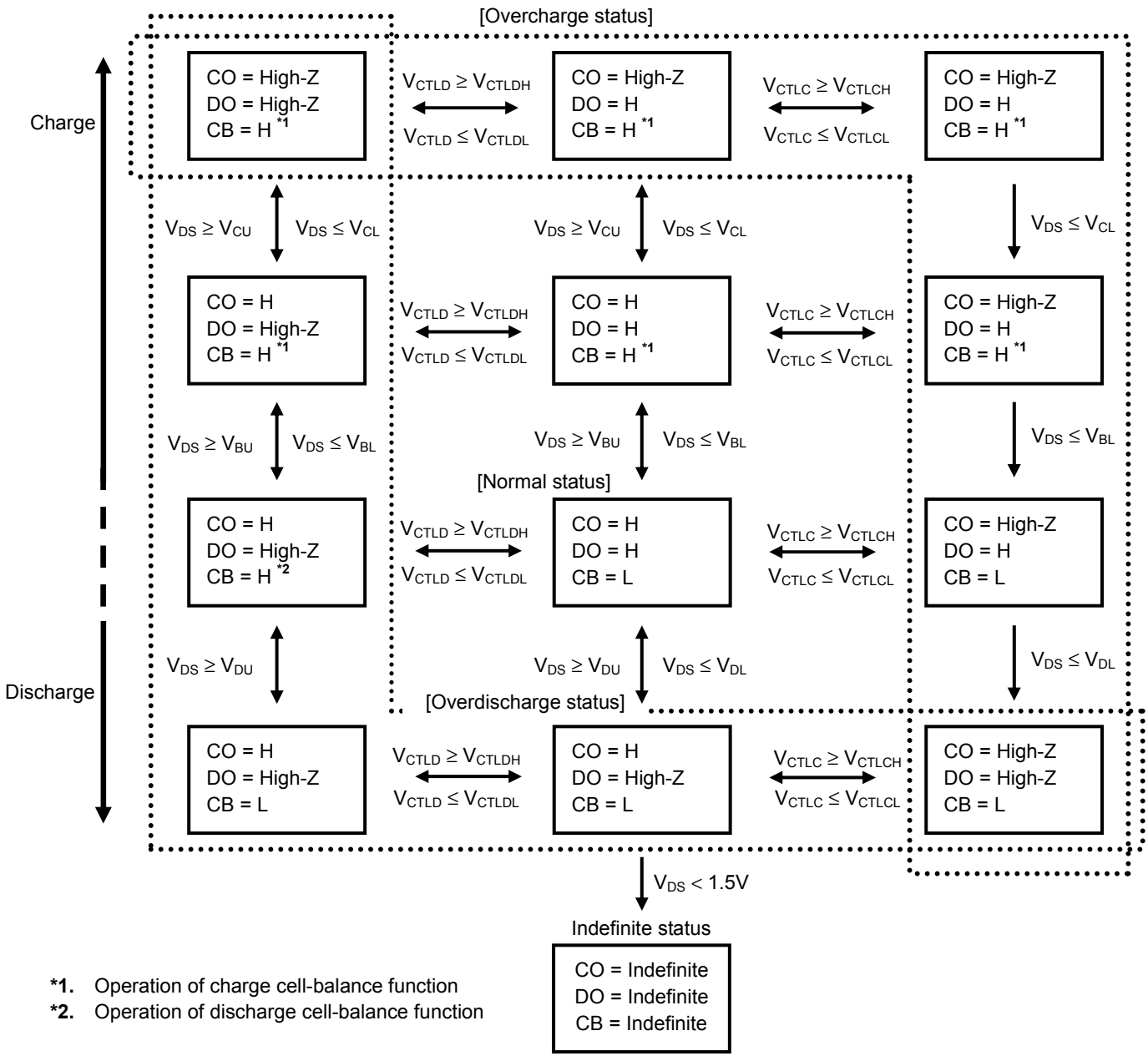


Figure 14 Test circuit 8

■ Operation

Figure 15 shows the operation transition of S-8209B.



***1.** Operation of charge cell-balance function
***2.** Operation of discharge cell-balance function

Figure 15 Operation Transition

1. Normal Status

In the S-8209B Series, both of CO and DO pin get the V_{DD} level; the voltage between VDD and VSS (V_{DS}) is more than the overdischarge detection voltage (V_{DL}), and is less than the overcharge detection voltage (V_{CU}) and respectively, the CTLC pin input voltage (V_{CTLC}) > the CTLC pin voltage "L" (V_{CTLCL}), the CTLD pin input voltage (V_{CTLD}) > the CTLD pin voltage "L" (V_{CTLDL}). This is the normal status.

2. Overcharge Status

In the S-8209B Series, the CO pin is in high impedance; when V_{DS} gets V_{CU} or more, or V_{CTLC} gets V_{CTLCL} or less. This is the overcharge status.

If V_{DS} gets the overcharge release voltage (V_{CL}) or less, and V_{CTLC} gets the CTLC pin voltage "H" (V_{CTLCH}) or more, the S-8209B Series releases the overcharge status to return to the normal status.

3. Overdischarge Status

In the S-8209B Series, the DO pin is in high impedance; when V_{DS} gets V_{DL} or less, or V_{CTLD} gets V_{CTLDL} or less. This is the overdischarge status.

If V_{DS} gets the overdischarge release voltage (V_{DU}) or more, and V_{CTLD} gets the CTLD pin voltage "H" (V_{CTLDH}) or more, the S-8209B Series releases the overdischarge status to return to the normal status.

4. Cell-balance Function

In the S-8209B Series, the CB pin gets the level of VDD pin; when V_{DS} gets the cell-balance detection voltage (V_{BU}) or more. This is the charge cell-balance function.
If V_{DS} gets the cell-balance release voltage (V_{BL}) or less again, the S-8209B Series sets the CB pin the level of VSS pin.

In addition, the CB pin gets the level of VDD pin; when V_{DS} is more than V_{DL}, and V_{CTLD} is V_{CTLDL} or less. This is the discharge cell-balance function.
If V_{CTLD} gets V_{CTLDH} or more, or V_{DS} is V_{DL} or less again, the S-8209B Series sets the CB pin the level of VSS pin.

5. Delay Circuit

In the S-8209B Series, users are able to set delay time which is from detection of changes in V_{DS}, V_{CTLC}, V_{CTLD} to output to the CO, DO, CB pin.

For example in the detection of overcharge status, when V_{DS} exceeds V_{CU}, or V_{CTLC} gets V_{CTLCH} or less, charging to C_{CDT} starts via R_{CDT}. If the voltage between CDT and VSS (V_{CDT}) reaches the CDT pin detection voltage (V_{CDET}), the CO pin is in high impedance. The output pin delay time t_D is calculated by the following formula.

$$t_D\,[s] = 10.0\ M\Omega\ (Typ.) \times C_{CDT}\,[\mu F]$$

The electric charge in C_{CDT} starts to be discharged when the delay time has finished.
The delay time that users have set for the CO pin, as seen above, is settable for each output pin DO, CB.

■ Example of Protection Circuit with S-8209B for Series Multi-Cells

Figure 16 shows the example of protection circuit with the S-8209B for series multi-cells.
Regarding the operation of protection circuit with the S-8209B for series-connected batteries, refer to the application note "S-8209B Series Usage Guidelines".

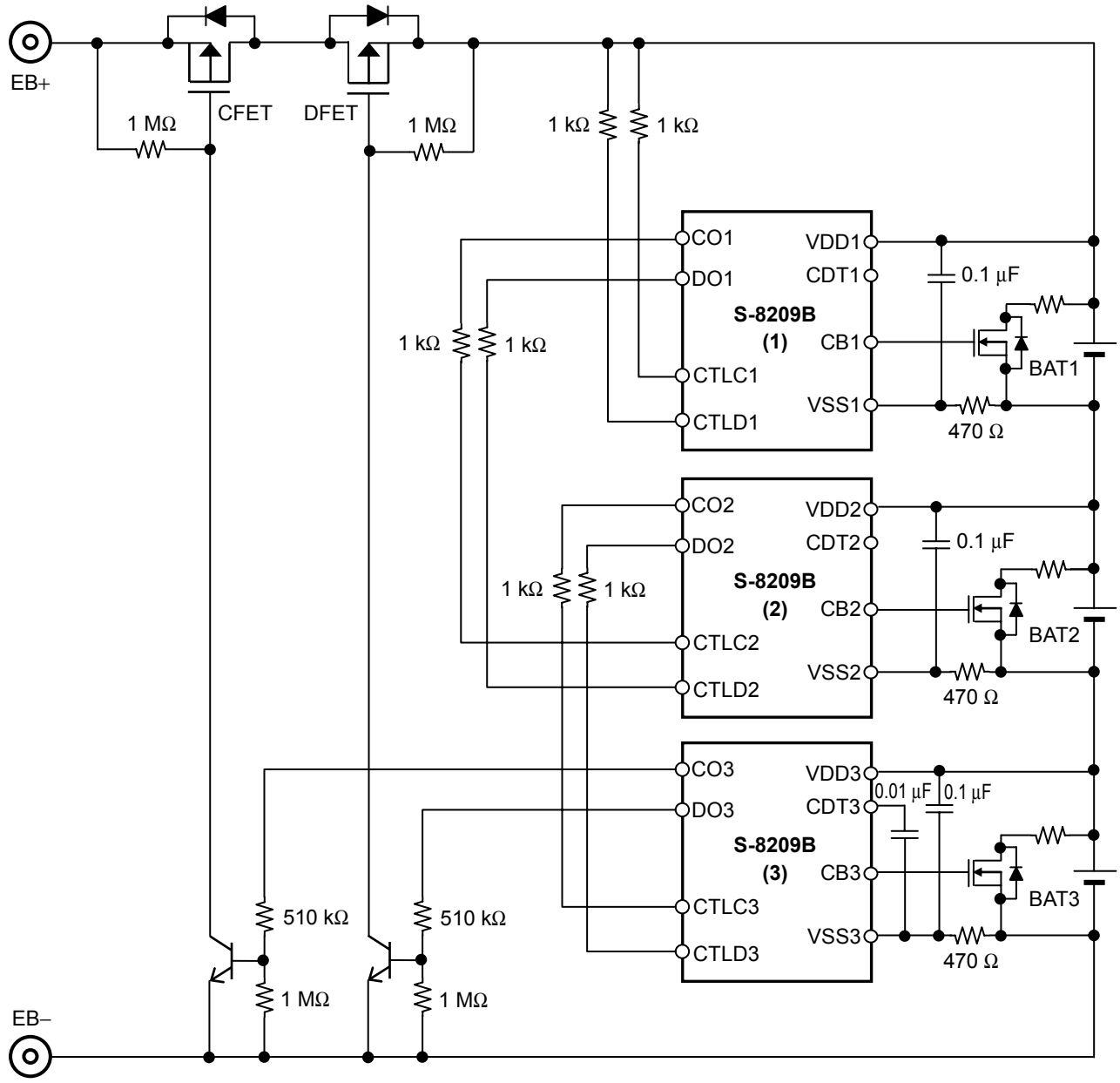


Figure 16

Caution 1. The above constants may be changed without notice.
2. The example of connection shown above and the constant do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constant.

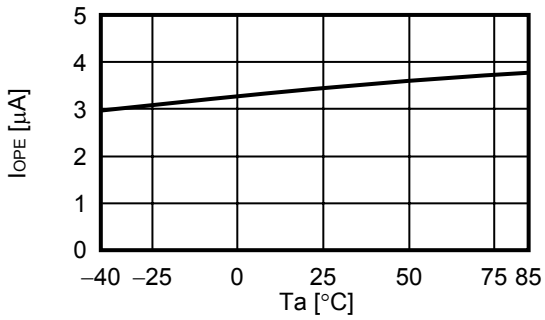
■ Precautions

- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- SII claims no responsibility for any and all disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

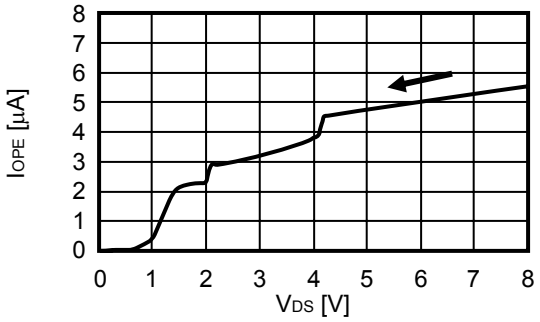
■ Characteristics (Typical Data)

1. Current consumption

(1) I_{OPE} – Ta

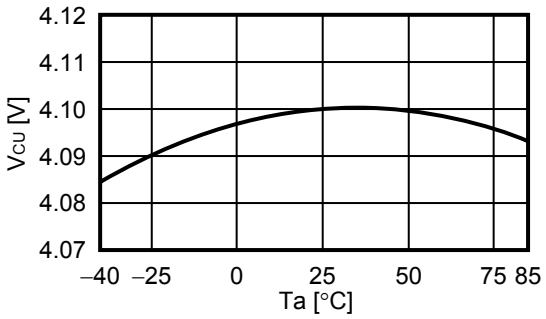


(2) I_{OPE} – V_{DS}

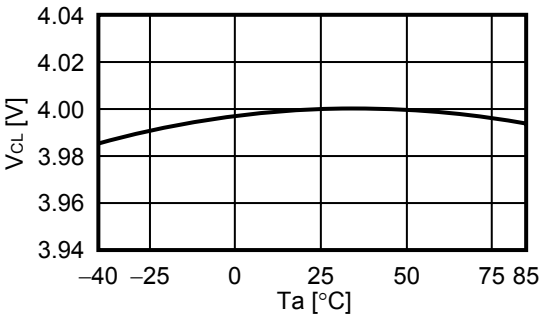


2. Overcharge detection / release voltages, Cell-balance detection / release voltages, Overdischarge detection / release voltages

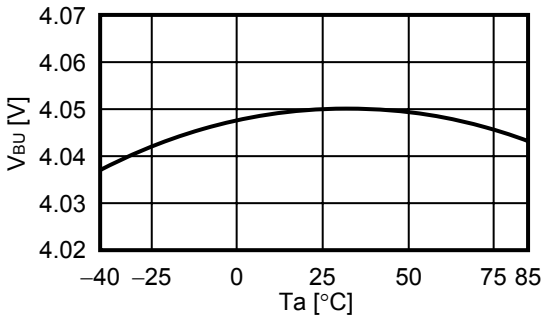
(1) V_{CU} – Ta



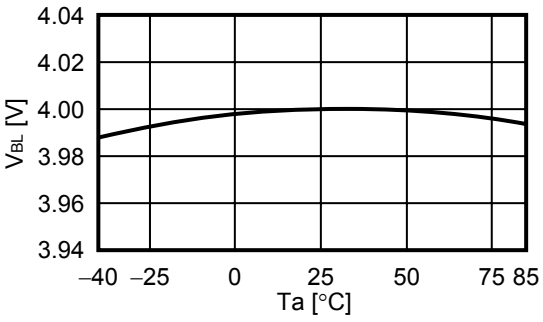
(2) V_{CL} – Ta



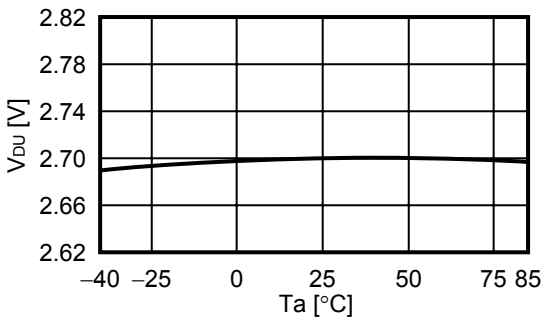
(3) V_{BU} – Ta



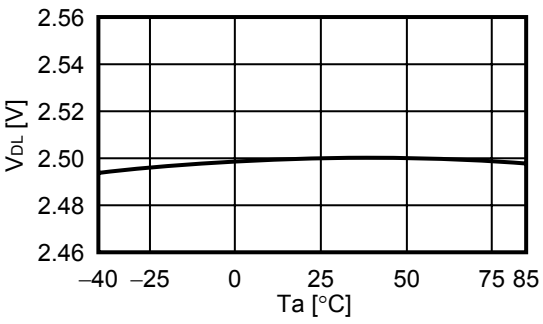
(4) V_{BL} – Ta



(5) V_{DU} – Ta

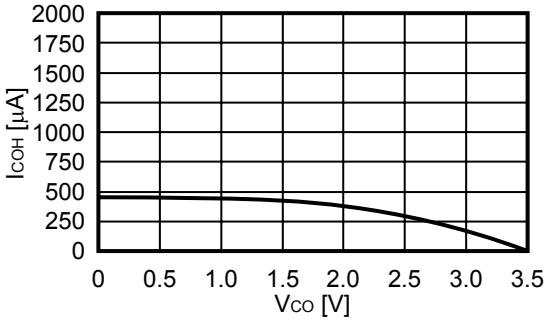


(6) V_{DL} – Ta

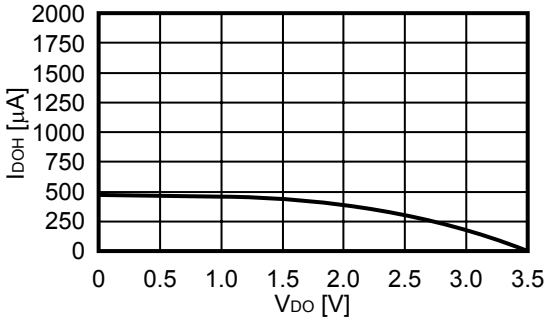


3. CO / DO / CB pin current

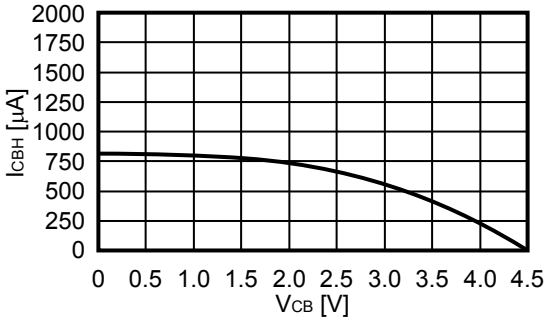
(1) I_{COH} – V_{CO} (V_{DS} = 3.5 V)



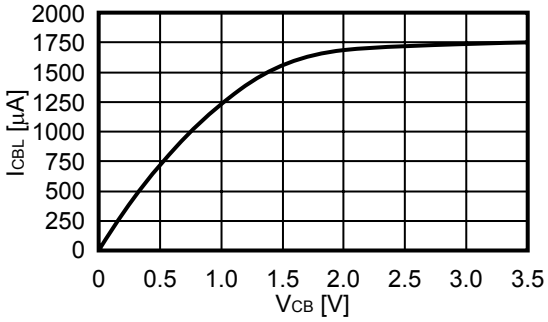
(2) I_{DOH} – V_{DO} (V_{DS} = 3.5 V)



(3) I_{CBH} – V_{CB} (V_{DS} = 4.5 V)

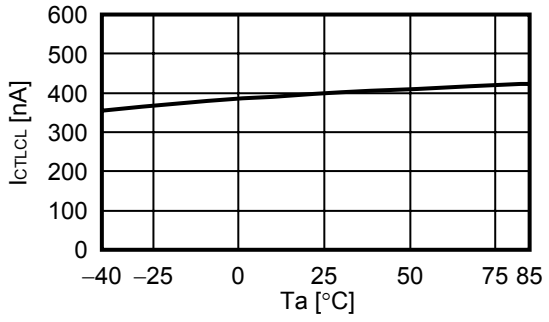


(4) I_{CBL} – V_{CB} (V_{DS} = 3.5 V)

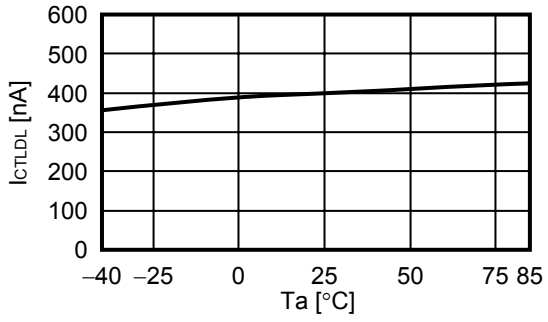


4. CTLC / CTLD pin current

(1) I_{CTLCL} – Ta (V_{DS} = 3.5 V)

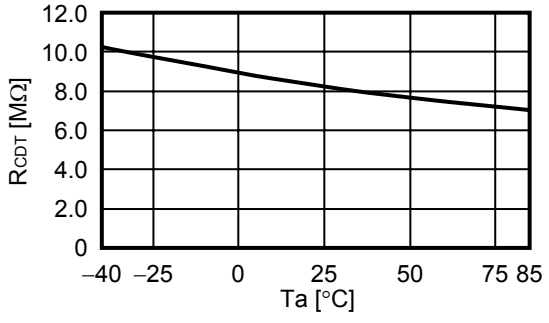


(2) I_{CTLDL} – Ta (V_{DS} = 3.5 V)

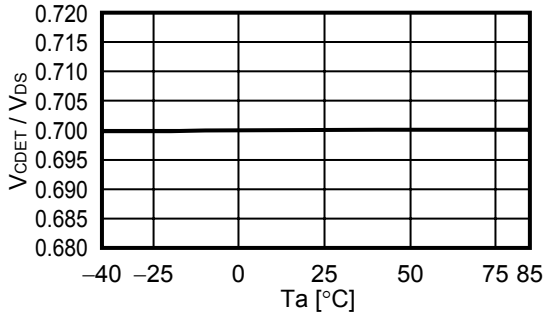


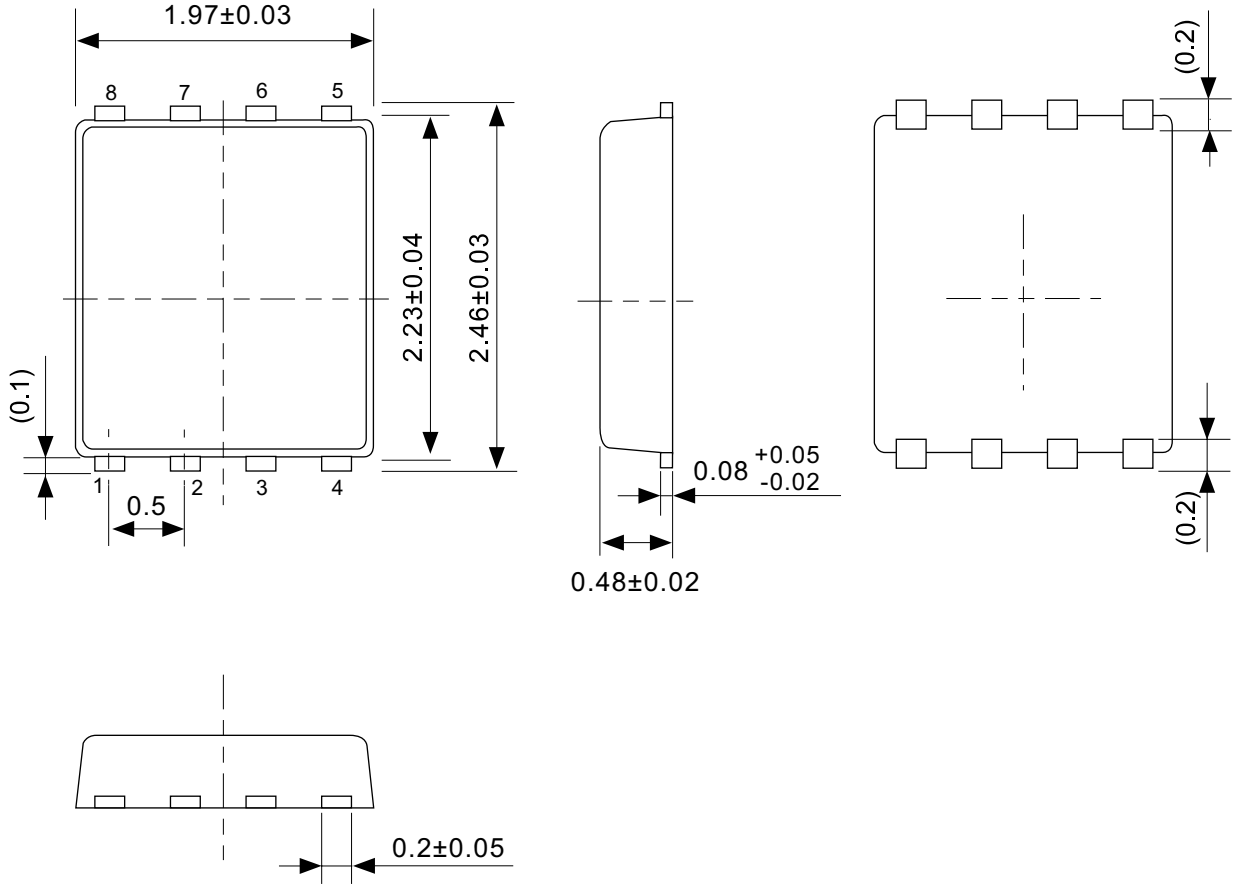
5. CDT pin resistance / CDT pin detection voltage

(1) R_{CDT} – Ta



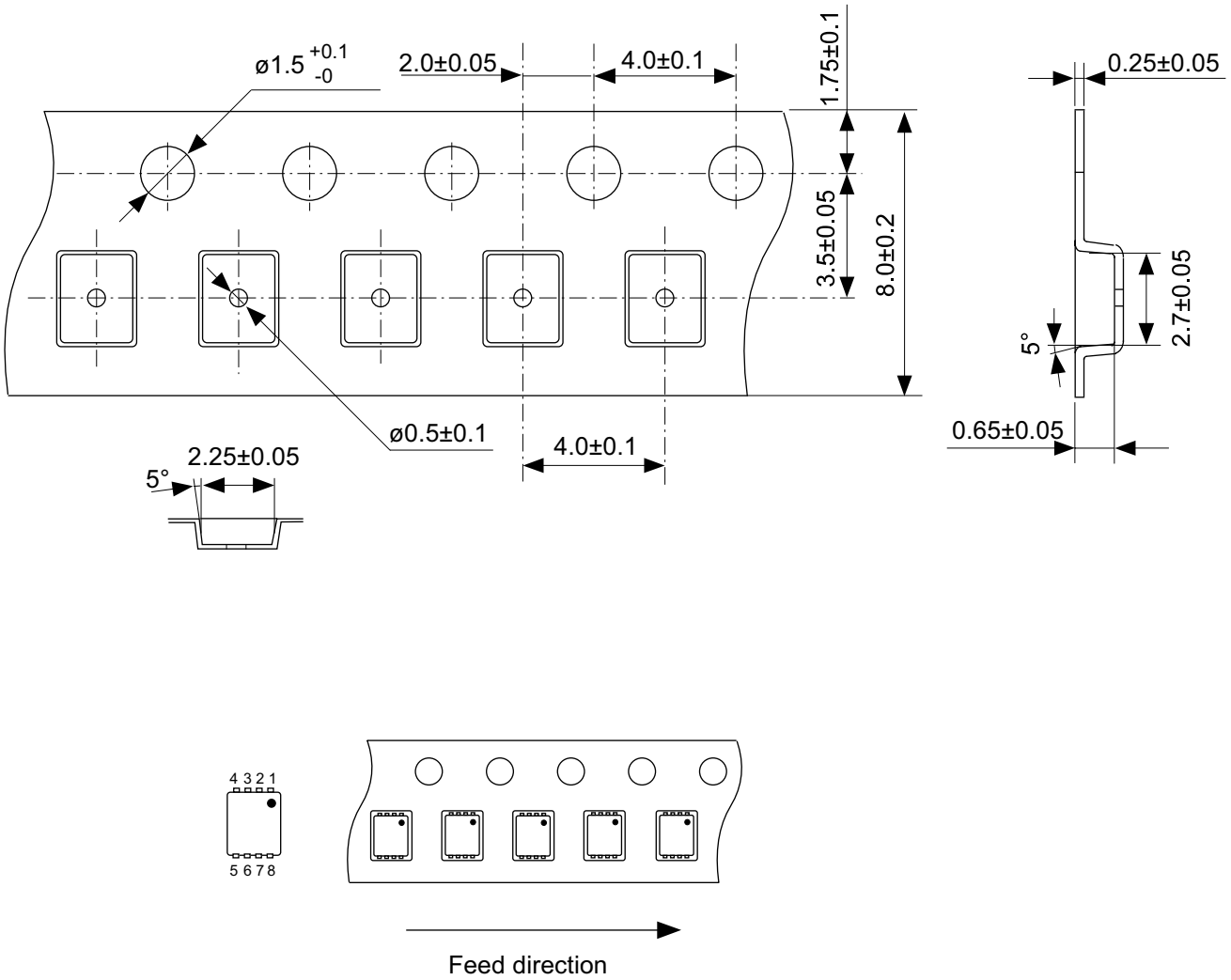
(2) V_{CDET} / V_{DS} – Ta





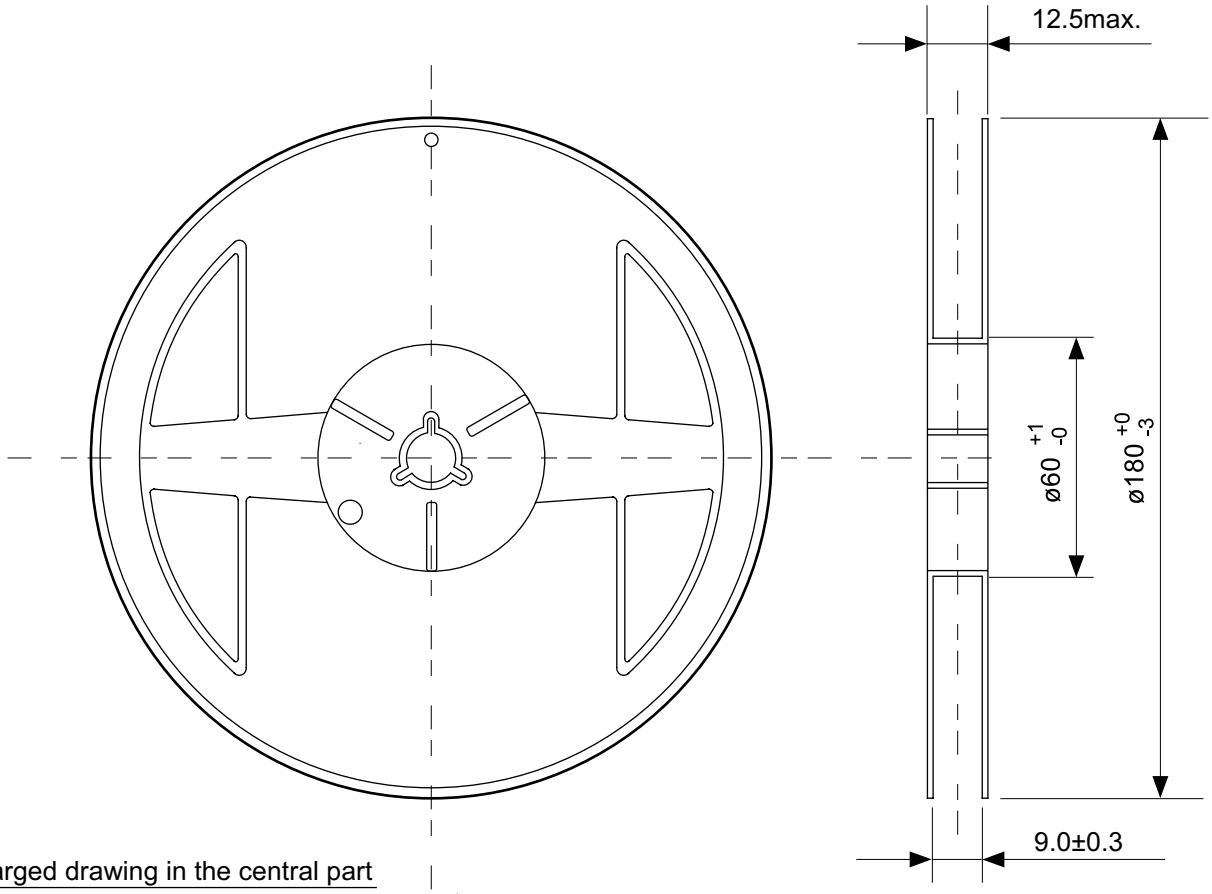
No. PH008-A-P-SD-2.0

TITLE	SNT-8A-A-PKG Dimensions
No.	PH008-A-P-SD-2.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	

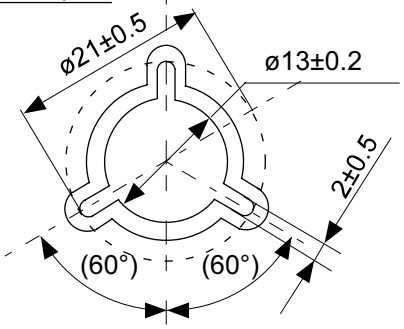


No. PH008-A-C-SD-1.0

TITLE	SNT-8A-A-Carrier Tape
No.	PH008-A-C-SD-1.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	

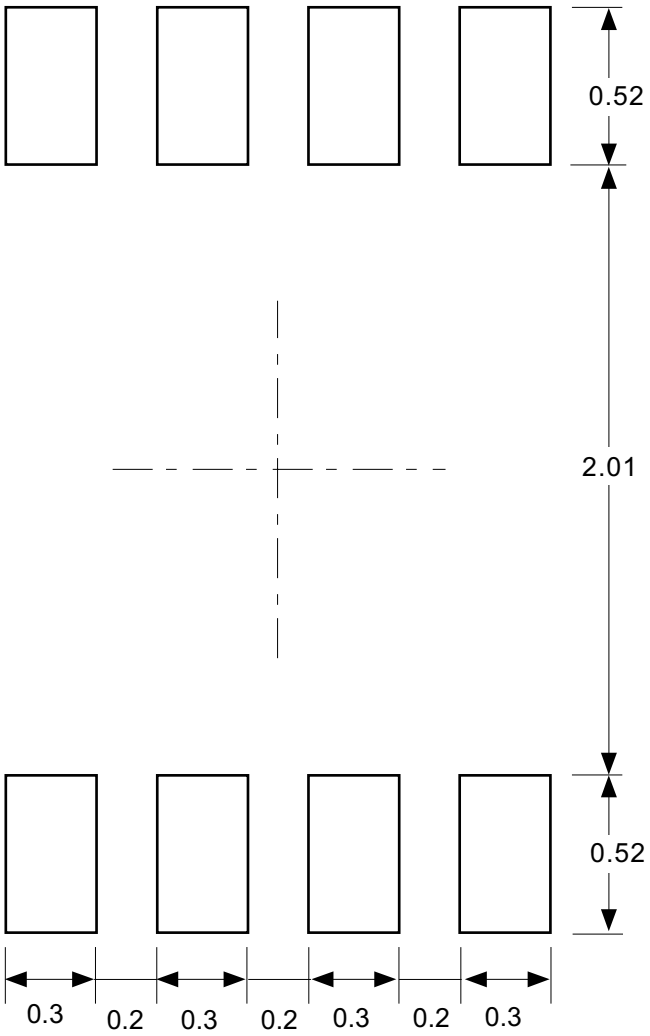


Enlarged drawing in the central part



No. PH008-A-R-SD-1.0

TITLE	SNT-8A-A-Reel		
No.	PH008-A-R-SD-1.0		
SCALE		QTY.	5,000
UNIT	mm		
Seiko Instruments Inc.			

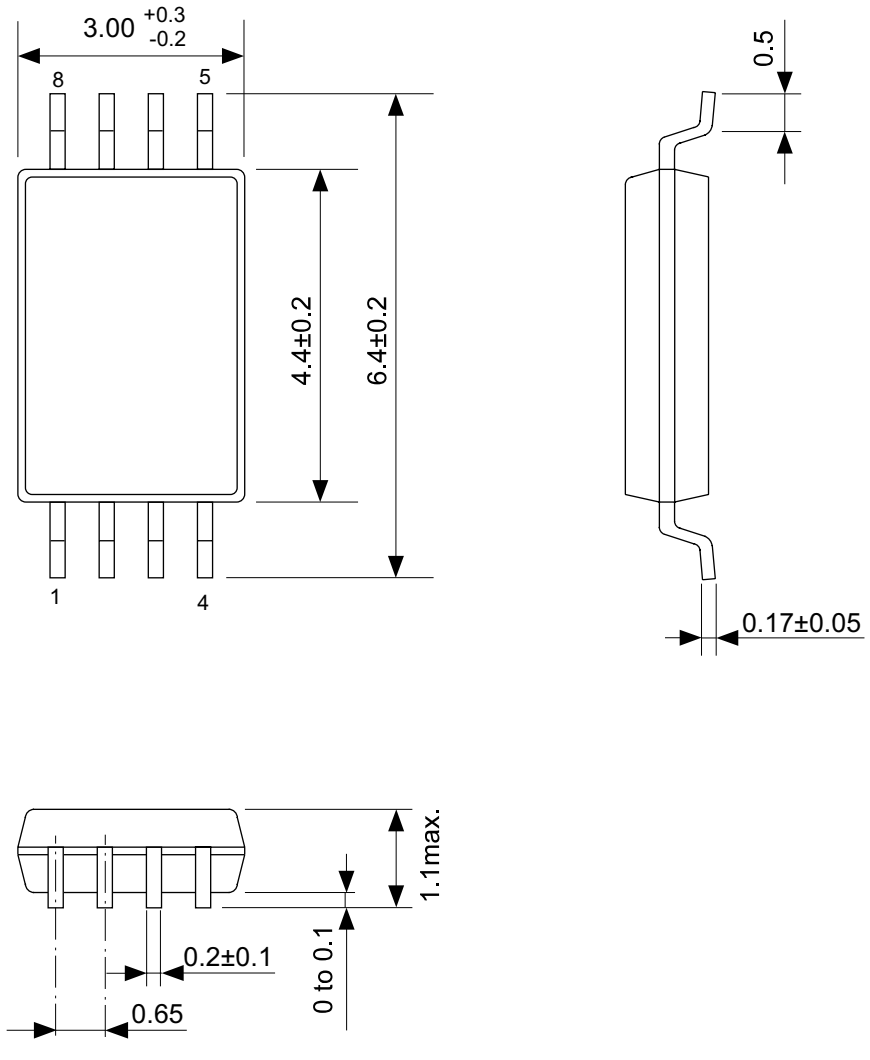


Caution Making the wire pattern under the package is possible. However, note that the package may be upraised due to the thickness made by the silk screen printing and of a solder resist on the pattern because this package does not have the standoff.

注意 パッケージ下への配線パターン形成は可能ですが、本パッケージはスタンドオフが無いので、パターン上のレジスト厚み、シルク印刷の厚みによってパッケージが持ち上がることがありますのでご配慮ください。

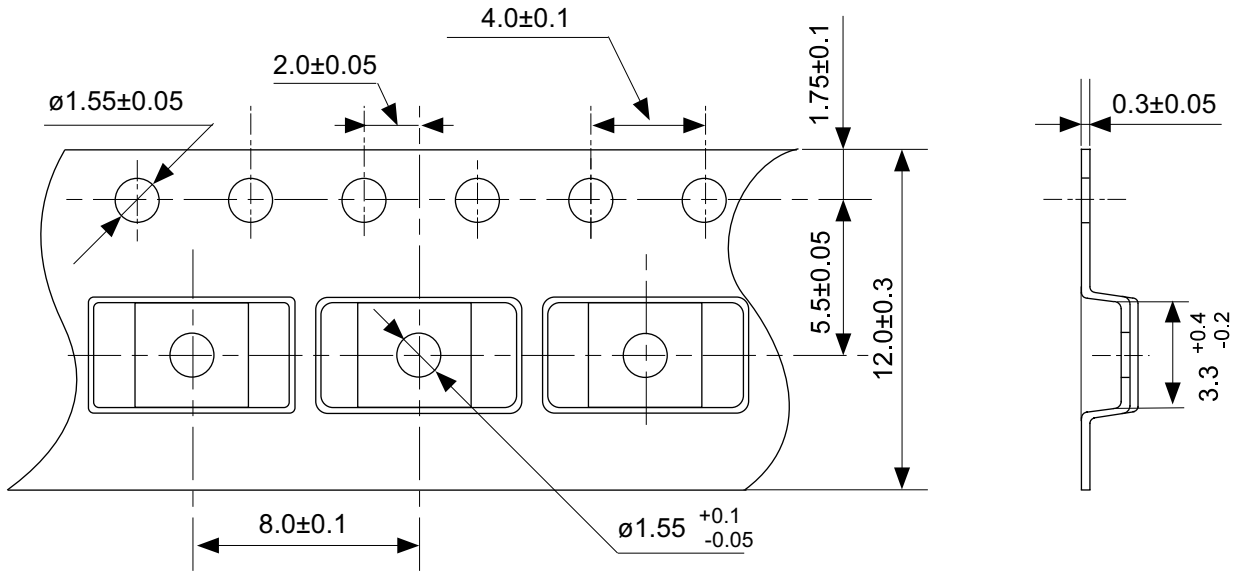
No. PH008-A-L-SD-3.0

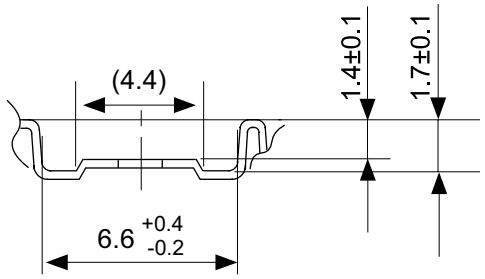
TITLE	SNT-8A-A-Land Recommendation
No.	PH008-A-L-SD-3.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	

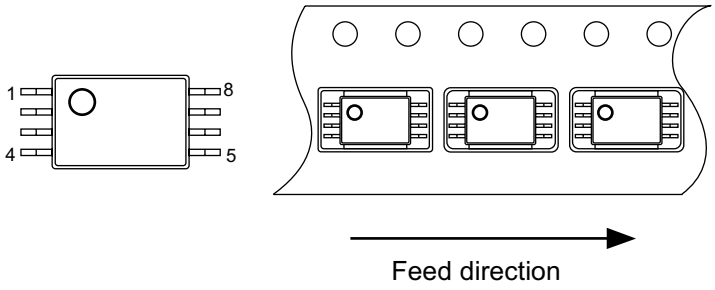


No. FT008-A-P-SD-1.1

TITLE	TSSOP8-E-PKG Dimensions
No.	FT008-A-P-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	

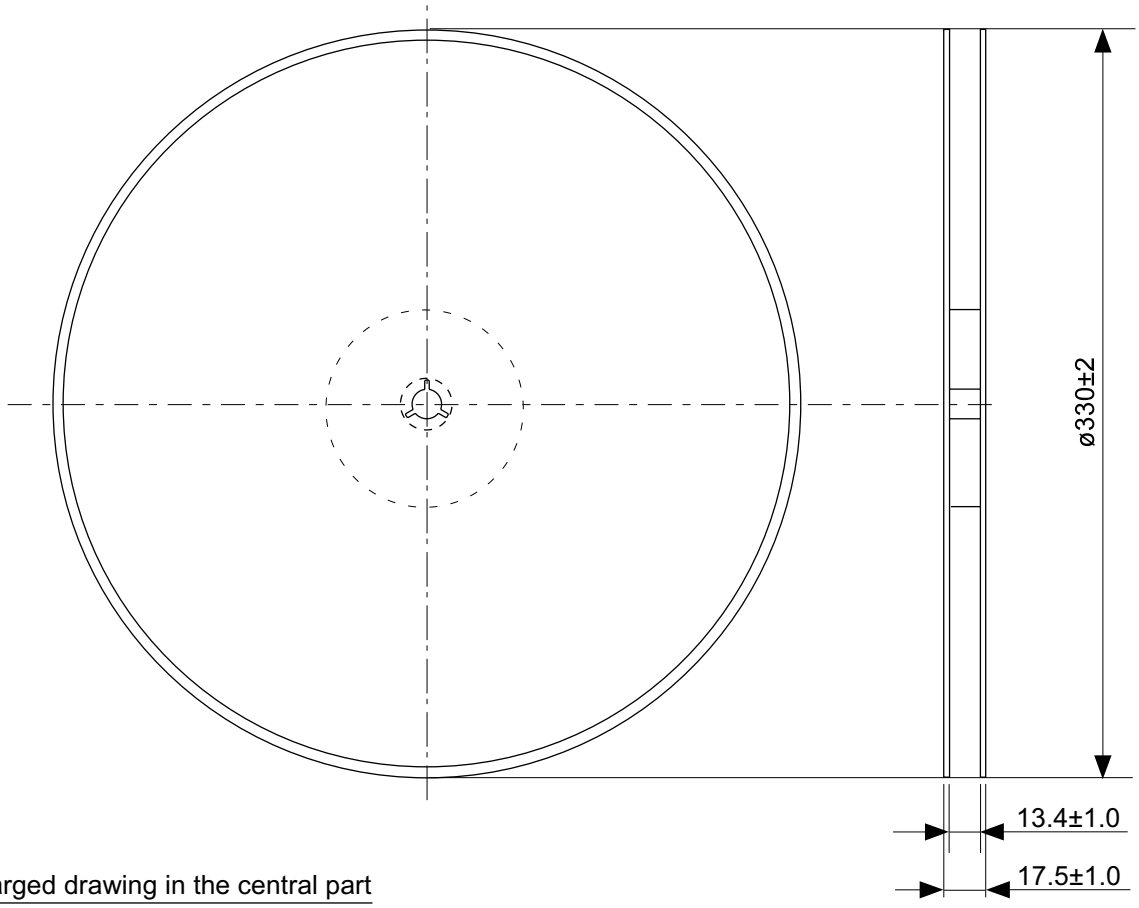




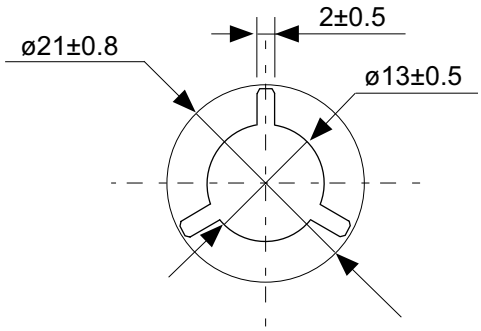


No. FT008-E-C-SD-1.0

TITLE	TSSOP8-E-Carrier Tape
No.	FT008-E-C-SD-1.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	



Enlarged drawing in the central part



No. FT008-E-R-SD-1.0

TITLE	TSSOP8-E-Reel		
No.	FT008-E-R-SD-1.0		
SCALE		QTY.	3,000
UNIT	mm		
Seiko Instruments Inc.			

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