TENTATIVE

LOW-VOLTAGE HIGH-PRECISION VOLTAGE DETECTOR

S-808 Series

The S-808 Series is a high-precision voltage detector developed using CMOS process. The detection voltage is fixed internally, with an accuracy of ±2.0%. Two output types, Nch open-drain and CMOS output, are available.

■ Features

- Ultra-low current consumption
  1.3 μA typ. (V_{DD}=1.5 V)
- High-precision detection voltage ±2.0%
- Low operating voltage 0.7 to 5.0 V
- Hysteresis characteristics 5% typ.
- Detection voltage 0.8 to 1.4 V
  (0.1V step)
- Nch open-drain active low and CMOS active low output
- SC-82AB ultra-small package

■ Applications

- Battery checker
- Power failure detector
- Reset for microcomputer

■ Pin Assignment

SC-82AB

Top view

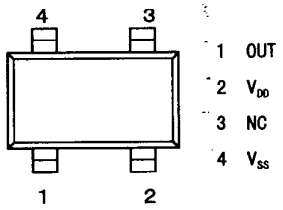
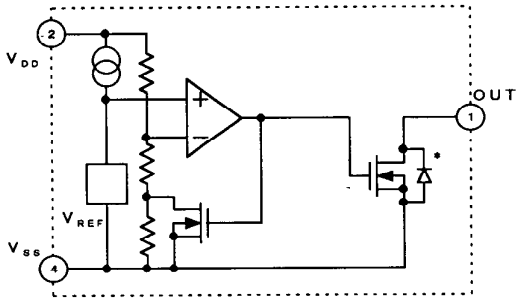


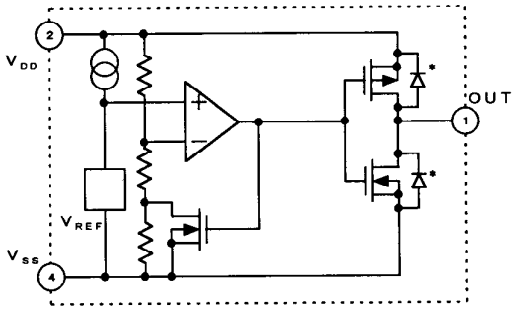
Figure 1

■ Block Diagram

(1) Nch open-drain active low output



(2) CMOS active low output



*Parasitic diode

Figure 2

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■ Selection Guide

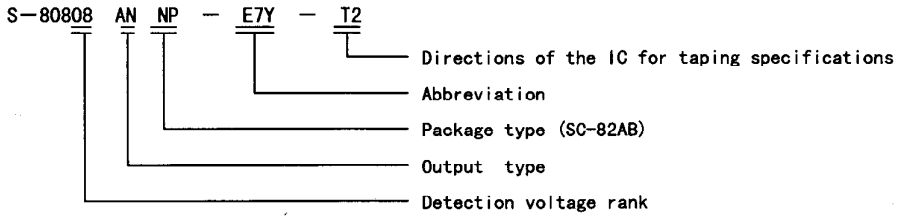


Table 1

Detection voltage range (V)	Hysteresis width V_{HYS} typ. (V)	Nch Open Drain(Low)	CMOS Output(Low)
0.8V±2.0%	0.034	S-80808ANNP-E7Y-T2	S-80808ALNP-E5Y-T2
0.9V±2.0%	0.044	S-80809ANNP-E7Z-T2	S-80809ALNP-E5Z-T2
1.0V±2.0%	0.054	S-80810ANNP-E70-T2	S-80810ALNP-E50-T2
1.1V±2.0%	0.064	S-80811ANNP-E71-T2	S-80811ALNP-E51-T2
1.2V±2.0%	0.073	S-80812ANNP-E72-T2	S-80812ALNP-E52-T2
1.3V±2.0%	0.083	S-80813ANNP-EDA-T2	S-80813ALNP-EAA-T2
1.4V±2.0%	0.093	S-80814ANNP-EDB-T2	S-80814ALNP-EAB-T2
1.5V±2.0%	0.075	S-80815ANNP-EDC-T2	S-80815ALNP-EAC-T2
1.6V±2.0%	0.080	S-80816ANNP-EDD-T2	S-80816ALNP-EAD-T2
1.7V±2.0%	0.085	S-80817ANNP-EDE-T2	S-80817ALNP-EAE-T2
1.8V±2.0%	0.090	S-80818ANNP-EDF-T2	S-80818ALNP-EAF-T2
1.9V±2.0%	0.095	S-80819ANNP-EDG-T2	S-80819ALNP-EAG-T2
2.0V±2.0%	0.100	S-80820ANNP-EDH-T2	S-80820ALNP-EAH-T2
2.1V±2.0%	0.105	S-80821ANNP-EDJ-T2	S-80821ALNP-EAJ-T2
2.2V±2.0%	0.110	S-80822ANNP-EDK-T2	S-80822ALNP-EAK-T2
2.3V±2.0%	0.115	S-80823ANNP-EDL-T2	S-80823ALNP-EAL-T2
2.4V±2.0%	0.120	S-80824ANNP-EDM-T2	S-80824ALNP-EAM-T2
2.5V±2.0%	0.125	S-80825ANNP-EDN-T2	S-80825ALNP-EAN-T2
2.6V±2.0%	0.130	S-80826ANNP-EDP-T2	S-80826ALNP-EAP-T2
2.7V±2.0%	0.135	S-80827ANNP-EDQ-T2	S-80827ALNP-EAQ-T2
2.8V±2.0%	0.140	S-80828ANNP-EDR-T2	S-80828ALNP-EAR-T2
2.9V±2.0%	0.145	S-80829ANNP-EDS-T2	S-80829ALNP-EAS-T2
3.0V±2.0%	0.150	S-80830ANNP-EDT-T2	S-80830ALNP-EAT-T2
3.1V±2.0%	0.155	S-80831ANNP-EDV-T2	S-80831ALNP-EAV-T2
3.2V±2.0%	0.160	S-80832ANNP-EDW-T2	S-80832ALNP-EAW-T2
3.3V±2.0%	0.165	S-80833ANNP-EDX-T2	S-80833ALNP-EAX-T2
3.4V±2.0%	0.170	S-80834ANNP-EDY-T2	S-80834ALNP-EAY-T2
3.5V±2.0%	0.175	S-80835ANNP-EDZ-T2	S-80835ALNP-EAZ-T2
3.6V±2.0%	0.180	S-80836ANNP-ED0-T2	S-80836ALNP-EA0-T2
3.7V±2.0%	0.185	S-80837ANNP-ED1-T2	S-80837ALNP-EA1-T2
3.8V±2.0%	0.190	S-80838ANNP-ED2-T2	S-80838ALNP-EA2-T2
3.9V±2.0%	0.195	S-80839ANNP-ED3-T2	S-80839ALNP-EA3-T2
4.0V±2.0%	0.200	S-80840ANNP-ED4-T2	S-80840ALNP-EA4-T2
4.1V±2.0%	0.205	S-80841ANNP-ED5-T2	S-80841ALNP-EA5-T2
4.2V±2.0%	0.210	S-80842ANNP-ED6-T2	S-80842ALNP-EA6-T2
4.3V±2.0%	0.215	S-80843ANNP-ED7-T2	S-80843ALNP-EA7-T2
4.4V±2.0%	0.220	S-80844ANNP-ED8-T2	S-80844ALNP-EA8-T2
4.5V±2.0%	0.225	S-80845ANNP-ED9-T2	S-80845ALNP-EA9-T2
4.6V±2.0%	0.230	S-80846ANNP-EJA-T2	S-80846ALNP-EEA-T2
4.7V±2.0%	0.235	S-80847ANNP-EJB-T2	S-80847ALNP-EEB-T2
4.8V±2.0%	0.240	S-80848ANNP-EJC-T2	S-80848ALNP-EEC-T2
4.9V±2.0%	0.245	S-80849ANNP-EJD-T2	S-80849ALNP-EED-T2
5.0V±2.0%	0.250	S-80850ANNP-EJE-T2	S-80850ALNP-EEE-T2
5.1V±2.0%	0.255	S-80851ANNP-EJF-T2	S-80851ALNP-EEF-T2
5.2V±2.0%	0.260	S-80852ANNP-EJG-T2	S-80852ALNP-EEG-T2
5.3V±2.0%	0.265	S-80853ANNP-EJH-T2	S-80853ALNP-EEH-T2
5.4V±2.0%	0.270	S-80854ANNP-EJJ-T2	S-80854ALNP-EEJ-T2
5.5V±2.0%	0.275	S-80855ANNP-EJK-T2	S-80855ALNP-EEK-T2
5.6V±2.0%	0.280	S-80856ANNP-EJL-T2	S-80856ALNP-EEL-T2
5.7V±2.0%	0.285	S-80857ANNP-EJM-T2	S-80857ALNP-EEM-T2
5.8V±2.0%	0.290	S-80858ANNP-EJN-T2	S-80858ALNP-EEN-T2
5.9V±2.0%	0.295	S-80859ANNP-EJP-T2	S-80859ALNP-EEP-T2
6.0V±2.0%	0.300	S-80860ANNP-EJQ-T2	S-80860ALNP-EEQ-T2

■ Output Configurations

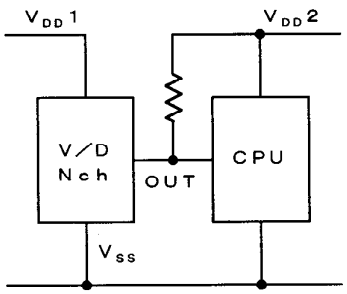
1. S-808 Series model numbering system

	Nch open-drain ("L" reset type)	CMOS output ("L" reset type)
S-808 Series	"N" is the last letter of the model number. e.g. S-80808AN	"L" is the last letter of the model number. e.g. S-80808AL

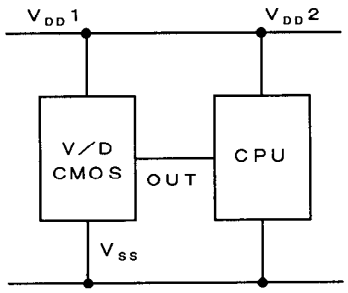
2. Output configurations and their implementation

Implementation	Nch ("L")	CMOS ("L")
With different power supplies	Yes	No
With different power supplies	Yes	Yes
With active high reset CPUs	No	No
With voltage divider variable resistors	Yes	No

• Example with two power supplies



• Examples with one power supply



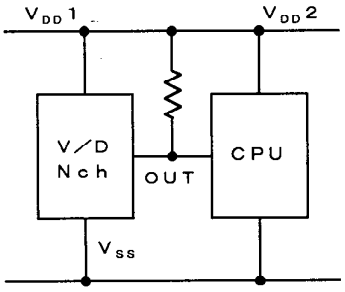


Figure 3

■ Advantage over the S-807 Series

The S-808 Series, in comparison with conventional reset ICs such as the S-807 Series, offers greater detection voltage precision (S-808 Series: ±2.0%; S-807 Series: ±2.4%) and lower operating voltage (S-808 Series: 0.7 V min.; S-807 Series: 1.0 V min.). These characteristics result in the following advantages over conventional products.

1. Advantages of greater detection voltage precision

1.1 Detecting battery service life

Typical discharge characteristics of batteries are shown in Figure 4. When using the S-807 Series, the service life can be detected over t1. When using the S-808 Series, it can be detected over t2. This improvement in detection precision of the S-808 Series allows batteries to be used to the full of their service life.

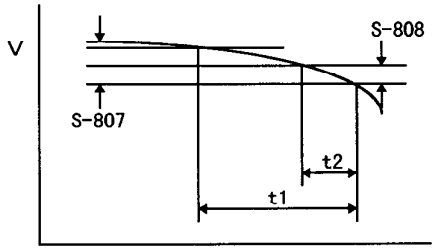


Figure 4

1.2 Detecting a power voltage at two points

It is usual for the CPU to detect the power voltage at two points, one to caution and the other to reset. The service life of the battery may also need to be detected at two points, one to caution and the other to request immediate replacement. In such cases, two detection voltage values (No. 1 and No. 2) should be set as close to the minimum operating voltage as possible, while keeping the two points as close to each other as possible. Since the S-808 Series offers higher precision in detecting voltage, No. 1 and No. 2 detections do not cross and can be effectuated correctly.

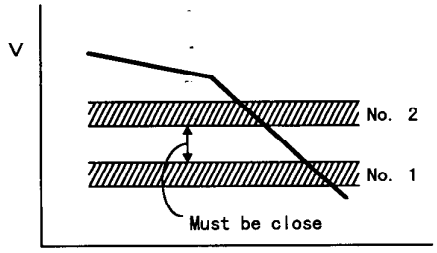


Figure 5

1.3 Operating margins of power and minimum operating voltage of CPU are close

Reset voltage is so designed that CPU will be reset between the power voltage and the minimum operating voltage of the CPU. Thus, if the two voltage are very close, the reset voltage must be detected correctly between them. Since the S-808 Series offers excellent detection voltage precision, the voltage between narrow limits can be detected correctly.

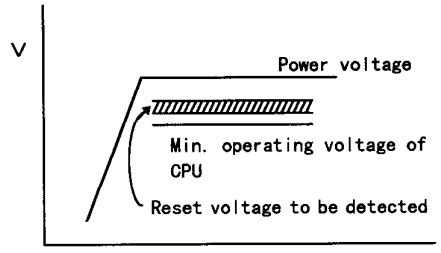


Figure 6

2. Advantage of lowered operating voltage

2.1 Low voltage detection

Voltages as low as 1.5 V, such as the power voltage of a single battery, can be detected using the S-808 Series which offers detection voltage in the range starting from 0.8 V.

■ Absolute Maximum Ratings

1. Products with a Detection voltage of 1. 4 or less.

(Unless otherwise specified: Ta=25°C)

Parameter		Symbol	Ratings	Unit
Power supply voltage		$V_{DD}-V_{SS}$	7	V
Output voltage	Nch open-drain	V_{OUT}	V_{SS}-0.3 to 7	V
	CMOS		V_{SS}-0.3 to V_{DD}+0.3	V
Output current		I_{OUT}	50	mA
Power dissipation		Pd	150	mW
Operating temperature		Topr	-20 to +70	°C
Storage temperature		Tstg	-40 to +125	°C

2. Products with a Detection voltage of 1. 5 or more.

(Unless otherwise specified: Ta=25)

Parameter		Symbol	Ratings	Unit
Power supply voltage		$V_{DD}-V_{SS}$	12	V
Output voltage	Nch open-drain	V_{OUT}	V_{SS}-0.3 to 12	V
	CMOS		V_{SS}-0.3 to V_{DD}+0.3	V
Output current		I_{OUT}	50	mA
Power dissipation		Pd	150	mW
Operating temperature		Topr	-40 to +85	°C
Storage temperature		Tstg	-40 to +125	°C

Note: This IC has a built-in protection circuit forstatic electricity, however, prevent contact with a largestatic electricity or electrostatic voltage which exceeds the efficiency of the protection circuit.

■ Electrical Characteristics

1. Detection voltage (0.8V to 1.4V)

(Unless otherwise specified: Ta=25℃)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test circuit
Detection voltage	$-V_{DET}$		S-80808AXXP	0.784	0.800	0.816	V	1
			S-80809AXXP	0.882	0.900	0.918		
			S-80810AXXP	0.980	1.000	1.020		
			S-80811AXXP	1.078	1.100	1.122		
			S-80812AXXP	1.176	1.200	1.224		
			S-80813AXXP	1.274	1.300	1.326		
			S-80814AXXP	1.372	1.400	1.428		
Release voltage	$+V_{DET}$		S-80808AXXP	0.802	0.900	0.918	V	1
			S-80809AXXP	0.910	0.944	0.979		
			S-80810AXXP	1.017	1.054	1.091		
			S-80811AXXP	1.125	1.164	1.203		
			S-80812AXXP	1.232	1.273	1.315		
			S-80813AXXP	1.340	1.383	1.427		
			S-80814AXXP	1.448	1.493	1.538		
Hysteresis width	V_{HYS}		S-80808AXXP	0.018	0.034	0.051	V	1
			S-80809AXXP	0.028	0.044	0.061		
			S-80810AXXP	0.037	0.054	0.071		
			S-80811AXXP	0.047	0.064	0.081		
			S-80812AXXP	0.056	0.073	0.091		
			S-80813AXXP	0.066	0.083	0.101		
			S-80814AXXP	0.076	0.093	0.110		
Current consumption	I_{SS}	V_{DD}=1.5V	S-80808AXXP	—	1.3	3.7	μA	2
			S-80809AXXP					
		V_{DD}=2.0V	S-80810AXXP					
			S-80811AXXP					
			S-80812AXXP					
			S-80813AXXP					
			S-80814AXXP					
Operating voltage	V_{DD}			0.7	—	5.0	V	1
Output current	I_{OUT}	Nch	V_{DS}=0.5V, V_{DD}=0.7V	0.04	0.2	—	mA	3
		Pch (CMOS output)	V_{DS}=2.1V, V_{DD}=4.5V	2.9	5.8	—		4
Leak current of output transistor	I_{LEAK}	Nch (Nch open drain)	V_{DS}=5.0V, V_{DD}=5.0V	—	—	60	nA	3
Temperature characteristic of $-V_{DET}$	$\frac{\Delta -V_{DET}}{\Delta Ta}$	Ta=-20℃ to +70℃	S-80808AXXP	—	±0.18	—	mV/℃	1
			S-80809AXXP	—	±0.20	—		
			S-80810AXXP	—	±0.22	—		
			S-80811AXXP	—	±0.24	—		
			S-80812AXXP	—	±0.27	—		
			S-80813AXXP	—	±0.29	—		
			S-80814AXXP	—	±0.31	—		

2. Detection voltage (1.5V to 2.6V)

(Unless otherwise specified: Ta=25°C)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test circuit
Detection voltage	$-V_{DET}$	S-80815AXXP		1.470	1.500	1.530	V	1
		S-80816AXXP		1.568	1.600	1.632		
		S-80817AXXP		1.666	1.700	1.734		
		S-80818AXXP		1.764	1.800	1.836		
		S-80819AXXP		1.862	1.900	1.938		
		S-80820AXXP		1.960	2.000	2.040		
		S-80821AXXP		2.058	2.100	2.142		
		S-80822AXXP		2.156	2.200	2.244		
		S-80823AXXP		2.254	2.300	2.346		
		S-80824AXXP		2.352	2.400	2.448		
		S-80825AXXP		2.450	2.500	2.550		
		S-80826AXXP		2.548	2.600	2.652		
Hysteresis width	V_{HYS}			$-V_{DET}$ ×0.03	$-V_{DET}$ ×0.05	$-V_{DET}$ ×0.08	V	1
Current consumption	I_{SS}	V_{DD}=3.5V		—	0.8	2.4	μA	2
Operating voltage	V_{DD}			0.95	—	10.0	V	1
Output current	I_{OUT}	Nch V_{DS}=0.5V	V_{DD}=1.2V	0.23	0.50	—	mA	3
		Pch (CMOS output) V_{DS}=0.5V	V_{DD}=4.8V	0.36	0.62	—		4
Leak current of output transistor	I_{LEAK}	Nch (Nch open drain)	V_{DS}=10.0V V_{DD}=10.0V	—	—	0.1	μA	3
Temperature characteristic of $-V_{DET}$	$\frac{\Delta -V_{DET}}{\Delta Ta}$	Ta=−40°C to +85°C	S-80815AXXP	—	±0.18	—	mV/°C	1
			S-80816AXXP	—	±0.19	—		
			S-80817AXXP	—	±0.20	—		
			S-80818AXXP	—	±0.21	—		
			S-80819AXXP	—	±0.22	—		
			S-80820AXXP	—	±0.24	—		
			S-80821AXXP	—	±0.25	—		
			S-80822AXXP	—	±0.26	—		
			S-80823AXXP	—	±0.27	—		
			S-80824AXXP	—	±0.28	—		
			S-80825AXXP	—	±0.29	—		
			S-80826AXXP	—	±0.31	—		

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3. Detection voltage (2.7V to 3.9V)

(Unless otherwise specified: Ta=25°C)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test circuit
Detection voltage	$-V_{DET}$	S-80827AXXP		2.646	2.700	2.754	V	1
		S-80828AXXP		2.744	2.800	2.856		
		S-80829AXXP		2.842	2.900	2.958		
		S-80830AXXP		2.940	3.000	3.060		
		S-80831AXXP		3.038	3.100	3.162		
		S-80832AXXP		3.136	3.200	3.264		
		S-80833AXXP		3.234	3.300	3.366		
		S-80834AXXP		3.332	3.400	3.468		
		S-80835AXXP		3.430	3.500	3.570		
		S-80836AXXP		3.528	3.600	3.672		
		S-80837AXXP		3.626	3.700	3.774		
		S-80838AXXP		3.724	3.800	3.876		
		S-80839AXXP		3.822	3.900	3.978		
Hysteresis width	V_{HYS}			$-V_{DET}$ 0.03	$-V_{DET}$ ×0.05	$-V_{DET}$ ×0.08	V	1
Current consumption	I_{SS}	V_{DD}=4.5V		—	0.9	2.7	μA	2
Operating voltage	V_{DD}			0.95	—	10.0	V	1
Output current	I_{OUT}	Nch V_{DS}=0.5V	V_{DD}=1.2V	0.23	0.50	—	mA	3
			V_{DD}=2.4V	1.60	3.70	—		
		Pch (CMOS output) V_{DS}=0.5V	V_{DD}=4.8V	0.36	0.62	—		4
Leak current of output transistor	I_{LEAK}	Nch (Nch open drain)	V_{DS}=10.0V V_{DD}=10.0V	—	—	0.1	μA	3
Temperature characteristic of $-V_{DET}$	$\frac{\Delta -V_{DET}}{\Delta Ta}$	Ta=−40°C to +85°C	S-80827AXXP	—	±0.32	—	mV/°C	1
			S-80828AXXP	—	±0.33	—		
			S-80829AXXP	—	±0.34	—		
			S-80830AXXP	—	±0.35	—		
			S-80831AXXP	—	±0.36	—		
			S-80832AXXP	—	±0.38	—		
			S-80833AXXP	—	±0.39	—		
			S-80834AXXP	—	±0.40	—		
			S-80835AXXP	—	±0.41	—		
			S-80836AXXP	—	±0.42	—		
			S-80837AXXP	—	±0.44	—		
			S-80838AXXP	—	±0.45	—		
			S-80839AXXP	—	±0.46	—		

4. Detection voltage (4.0V to 5.6V)

(Unless otherwise specified: Ta=25°C)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test circuit
Detection voltage	$-V_{DET}$	S-80840AXXP		3.920	4.000	4.080	V	1
		S-80841AXXP		4.018	4.100	4.182		
		S-80842AXXP		4.116	4.200	4.284		
		S-80843AXXP		4.214	4.300	4.386		
		S-80844AXXP		4.312	4.400	4.488		
		S-80845AXXP		4.410	4.500	4.590		
		S-80846AXXP		4.508	4.600	4.692		
		S-80847AXXP		4.606	4.700	4.794		
		S-80848AXXP		4.704	4.800	4.896		
		S-80849AXXP		4.802	4.900	4.998		
		S-80850AXXP		4.900	5.000	5.100		
		S-80851AXXP		4.998	5.100	5.202		
		S-80852AXXP		5.096	5.200	5.304		
		S-80853AXXP		5.194	5.300	5.406		
		S-80854AXXP		5.292	5.400	5.508		
		S-80855AXXP		5.390	5.500	5.610		
		S-80856AXXP		5.488	5.600	5.712		
Hysteresis width	V_{HYS}			$-V_{DET}$ ×0.03	$-V_{DET}$ ×0.05	$-V_{DET}$ ×0.08	V	1
Current consumption	I_{SS}	V_{DD}=6.0V		—	1.0	3.0	μA	2
Operating voltage	V_{DD}			0.95	—	10.0	V	1
Output current	I_{OUT}	Nch	V_{DD}=1.2V	0.23	0.50	—	mA	3
		V_{DS}=0.5V	V_{DD}=2.4V	1.60	3.70	—		
		Pch (CMOS output) V_{DS}=0.5V	V_{DD}=6.0V	0.46	0.75	—		4
Leak current of output transistor	I_{LEAK}	Nch (Nch open drain)	V_{DS}=10.0V V_{DD}=10.0V	—	—	0.1	μA	3
Temperature characteristic of $-V_{DET}$	$\frac{\Delta -V_{DET}}{\Delta Ta}$	Ta=-40°C to +85°C	S-80840AXXP	—	±0.47	—	mV/°C	1
			S-80841AXXP	—	±0.48	—		
			S-80842AXXP	—	±0.49	—		
			S-80843AXXP	—	±0.51	—		
			S-80844AXXP	—	±0.52	—		
			S-80845AXXP	—	±0.53	—		
			S-80846AXXP	—	±0.54	—		
			S-80847AXXP	—	±0.55	—		
			S-80848AXXP	—	±0.56	—		
			S-80849AXXP	—	±0.58	—		
			S-80850AXXP	—	±0.59	—		
			S-80851AXXP	—	±0.60	—		
			S-80852AXXP	—	±0.61	—		
			S-80853AXXP	—	±0.62	—		
			S-80854AXXP	—	±0.64	—		
			S-80855AXXP	—	±0.65	—		
			S-80856AXXP	—	±0.66	—		

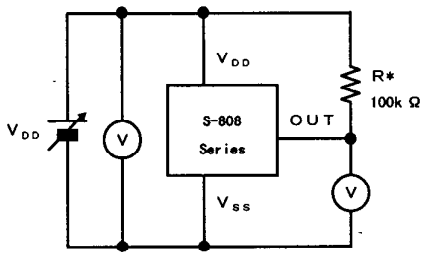
5. Detection voltage (5.7V to 6.0V)

(Unless otherwise specified: Ta=25℃)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test circuit
Detection voltage	$-V_{DET}$	S-80857AXXP		5.586	5.700	5.814	V	1
		S-80858AXXP		5.684	5.800	5.916		
		S-80859AXXP		5.782	5.900	6.018		
		S-80860AXXP		5.880	6.000	6.120		
Hysteresis width	V_{HYS}			$-V_{DET}$ ×0.03	$-V_{DET}$ ×0.05	$-V_{DET}$ ×0.08	V	1
Current consumption	I_{SS}	V_{DD}=7.5V		—	1.0	3.0	μA	2
Operating voltage	V_{DD}			0.95	—	10.0	V	1
Output current	I_{OUT}	Nch	V_{DD}=1.2V	0.23	0.50	—	mA	3
		V_{DS}=0.5V	V_{DD}=2.4V	1.60	3.70	—		
		Pch (CMOS output) V_{DS}=0.5V	V_{DD}=8.4V	0.59	0.96	—		4
Leak current of output transistor	I_{LEAK}	Nch (Nch open drain)	V_{DS}=10.0V V_{DD}=10.0V	—	—	0.1	μA	3
Temperature characteristic of $-V_{DET}$	$\frac{\Delta -V_{DET}}{\Delta Ta}$	Ta=-40℃ to +85℃	S-80857AXXP	—	±0.67	—	mV/℃	1
			S-80858AXXP	—	±0.68	—		
			S-80859AXXP	—	±0.69	—		
			S-80860AXXP	—	±0.71	—		

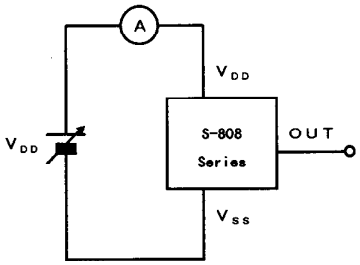
■ Test Circuits

(1)

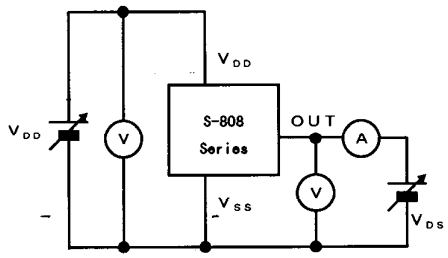


* R is unnecessary for CMOS output products.

(2)



(3)



(4)

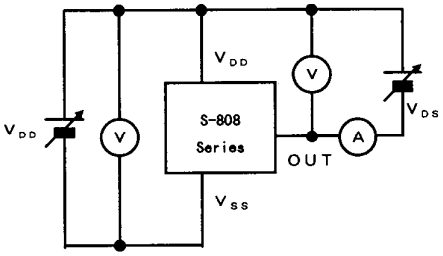


Figure 7

■ Technical Terms

1. Detection voltage ($-V_{DET}$)

The detection voltage $-V_{DET}$ is the voltage at which the detector goes active, and the voltage at which the output goes low in products with Nch open-drain and CMOS active low output types. This detection voltage varies slightly among products of the same type. The variation of voltages between the specified minimum [$(-V_{DET})$min.] and maximum [$(-V_{DET})$max.] values is called the detection voltage range (See Figure 8).

Example : For the S-80808AN, detection voltage lies in the range of $0.784 \leqq (-V_{DET}) \leqq 0.816$.
This means that $-V_{DET}$ is 0.784 in a product while $-V_{DET}$ is 0.816 in another of the same S-80808AN.

2. Release voltage ($+V_{DET}$)

The release voltage $+V_{DET}$ is the voltage at which the output returns (is "released") to high in products with Nch open-drain and CMOS active low output types. This release voltage varies slightly among products of the same type. The variation of voltages between the specified minimum [$(+V_{DET})$min.] and maximum [$(+V_{DET})$max.] values is called the release voltage range (See Figure 9).

Example : For the S-80808AN, the release voltage lies in the range of $0.802 \leqq (+V_{DET}) \leqq 0.867$. This means that $+V_{DET}$ is 0.802 in a product while $+V_{DET}$ is 0.867 in another of the same S-80808AN.

Note: Although the detection voltage and release voltage overlap in the range of 0.802 V to 0.816 V, $+V_{DET}$ will always be larger than $-V_{DET}$.

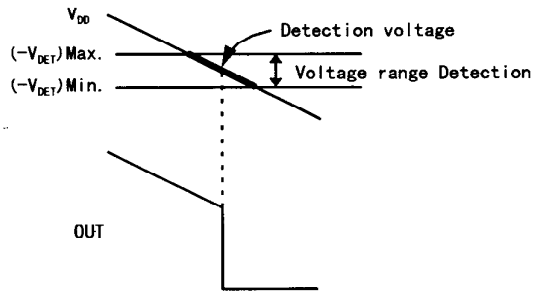


Figure 8

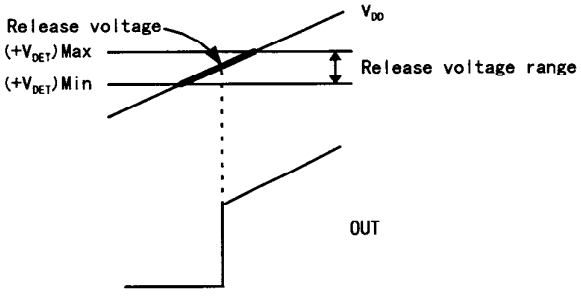


Figure 9

3. Hysteresis width (V_{HYS})

The hysteresis width is the voltage difference between the detection voltage and the release voltage ($B-A=V_{HYS}$ in Figure 13). By giving a device hysteresis, trouble such as noise at the input is avoided.

4. Through-type current

Through-type current refers to the current which flows instantaneously at the time of detection and release of a voltage detector. Through-type current is large in CMOS output devices, and also flows to some extent in Nch open-drain output devices.

5. Oscillation

In applications where a resistor is connected to the voltage detector input (Figure 10), in the CMOS active low products for example, the through-type current generated when the output goes from low to high (release) causes a voltage drop equal to [through-type current] × [input resistance] across the resistor. When the resultant input voltage drops below the detection voltage $-V_{DET}$, the output voltage returns to its low level. In this state, the through-type current — and its resultant voltage drop — have disappeared, and the output goes back from low to high. A through-type current is again generated, a voltage drop appears, and the process repeats. This unstable condition is referred to as oscillation.

- Misimplementation with input voltage divider

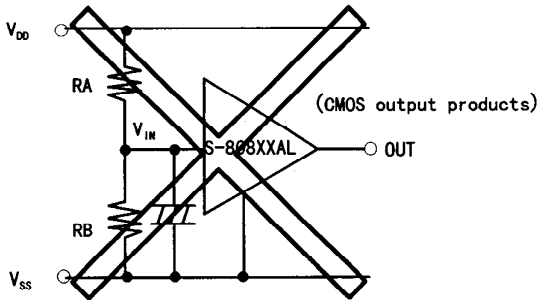
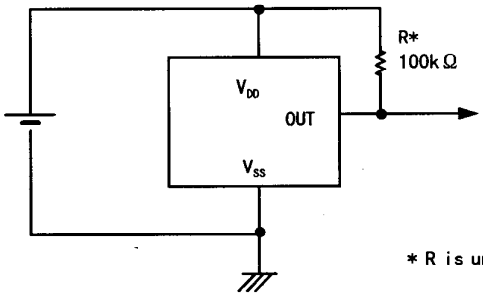


Figure 10

■ Standard Circuit



* R is unnecessary for CMOS output products.

Figure 11

■ Operation

1. Basic operation : CMOS active low output

(1) When power supply voltage V_{DD} is greater than the release voltage $+V_{DET}$, the Nch transistor is OFF and the Pch transistor ON, causing V_{DD} (high) to appear at the output. With the Nch transistor N1 of Figure 12 OFF, the comparator input voltage is $(RB+RC)/(RA+RB+RC) \times V_{DD}$.

(2) When power supply voltage V_{DD} goes below $+V_{DET}$, the output maintains the power supply voltage level, as long as V_{DD} remains above the detection voltage $-V_{DET}$. When V_{DD} does fall below $-V_{DET}$ (A in Figure 13), the Nch transistor goes ON, the Pch transistor goes OFF, and V_{SS} appears at the output. With the Nch transistor N 1 of Figure 12 ON, the comparator input voltage is $RB/(RA+RB) \times V_{DD}$.

(3) When V_{DD} falls below the minimum operating voltage, the output becomes undefined. However, output will revert to V_{DD} if a pull-up has been employed.

(4) V_{SS} will again be output when V_{DD} rises above the minimum operating voltage. V_{SS} will continue to be output even when V_{DD} surpasses $-V_{DET}$, as long as it does not exceed the release voltage $+V_{DET}$.

(5) When V_{DD} rises above $+V_{DET}$ (B in Figure 13), the Nch transistor goes OFF, the Pch transistor goes ON, and V_{DD} appears at the output.

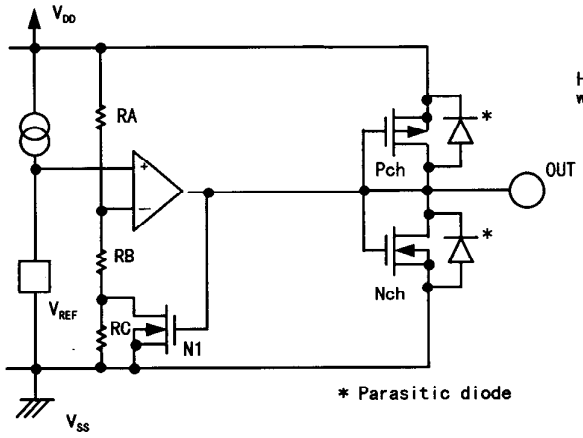


Figure 12

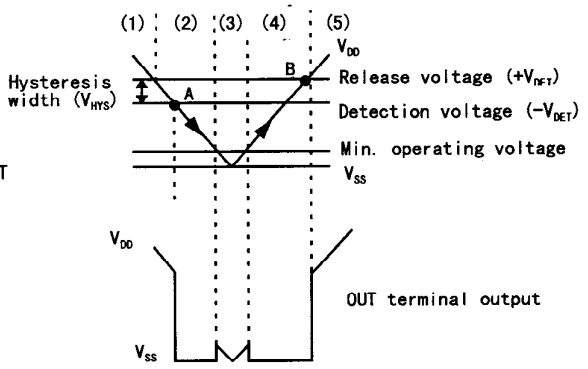


Figure 13

2. Other characteristics

(1) Temperature characteristic of detection voltage

Because of the excellent temperature characteristics of the reference voltage circuit, the temperature characteristics of the detection voltage are expressed by the following formula in the range of -20℃ to +70 C.

$$\frac{-V_{DET}}{V_{REF}} \times (\pm 0.1)\ \text{mV/℃} \quad \text{typ.}$$

* V_{REF} is 0.30 V min., 0.45 V typ., 0.60 V max.
(Products with a Detection voltage of 1. 4 or more.)
0.70 V min., 0.85 V typ., 1.00 V max.
(Products with a Detection voltage of 1. 5 or more.)

(2) Temperature characteristics of release voltage

$$\frac{+V_{DET}}{V_{REF}} \times (\pm 0.1)\ \text{mV/℃} \quad \text{typ.}$$

■ Dimensions

SC-82AB

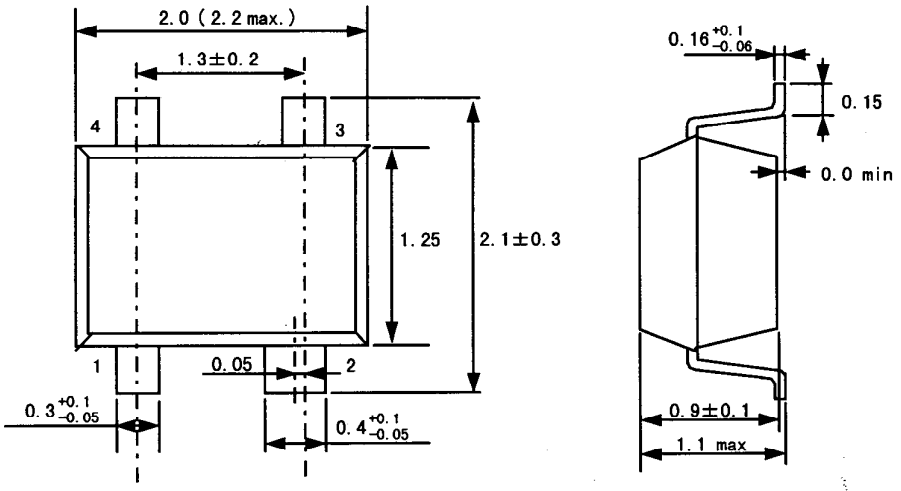


Figure 14

■ Taping

SC-82AB

1. Tape specifications

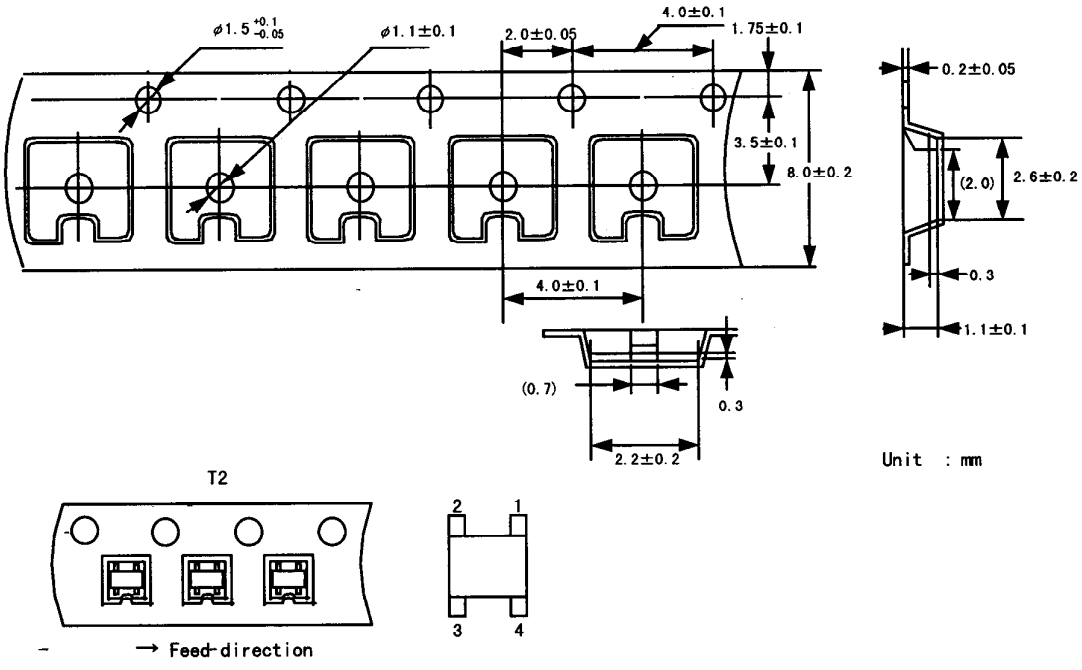


Figure 15

2. Reel specifications

1 reel holds 3000 detectors.

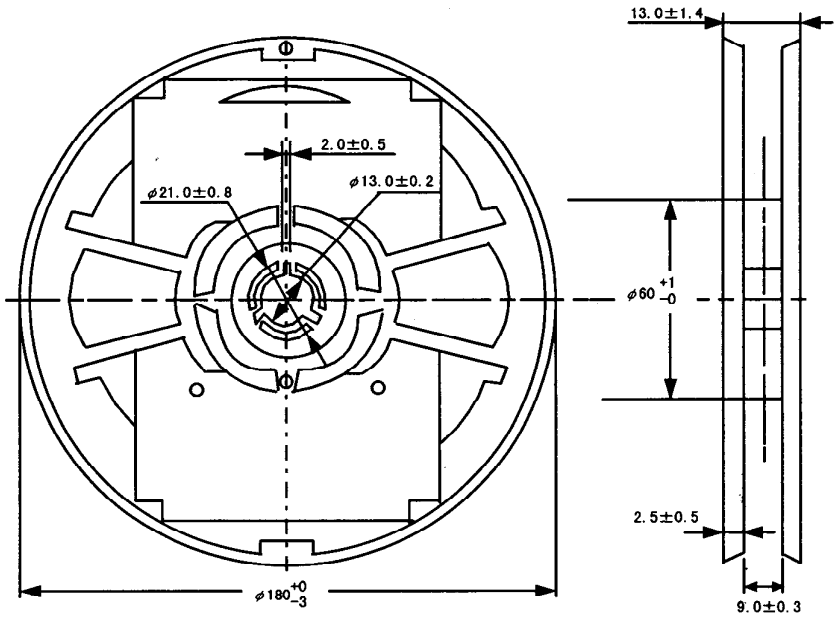
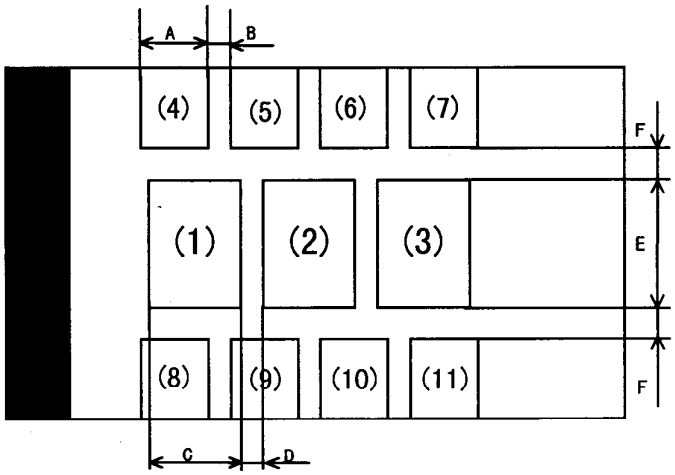


Figure 16

Unit : mm

■ Marking



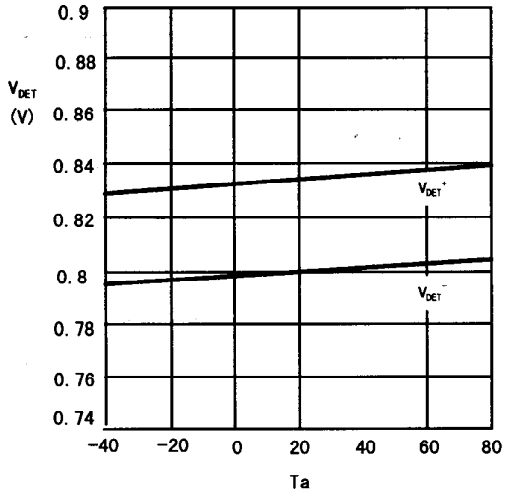
(1) to (3) Product name (abbreviation)
(4) to (11) Lot No. (indicated by dots)

Figure 17

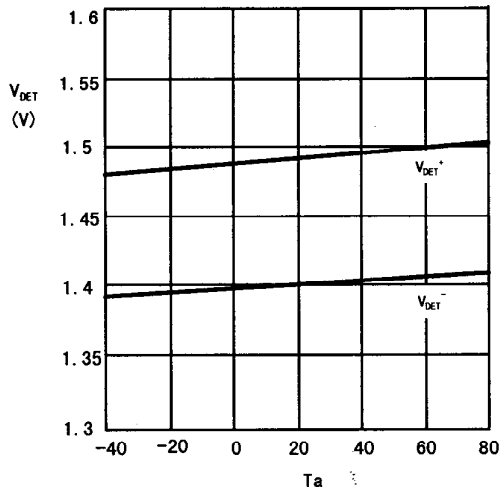
■ Characteristics (typical characteristics)

(1) Detection voltage (V_{DET}) – Temperature (Ta)

(a) S-80808AL

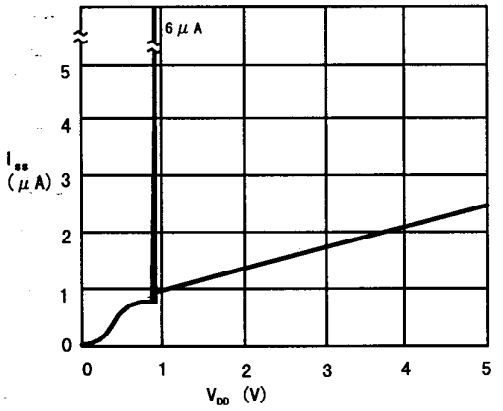


(b) S-80814AL

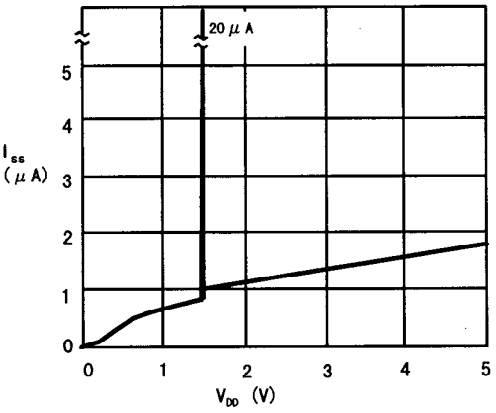


(2) Current consumption (I_{SS}) – Input voltage (V_{DD})

(a) S-80808AL

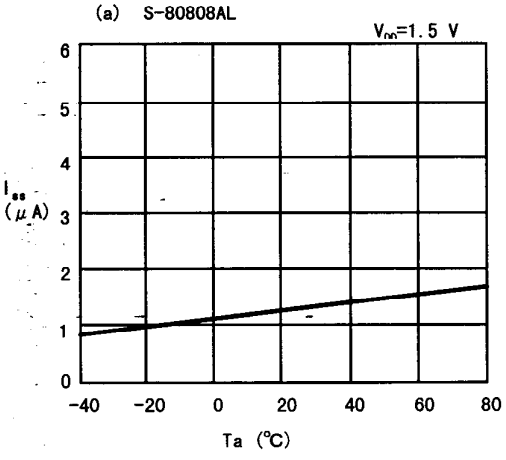


(b) S-80814AL

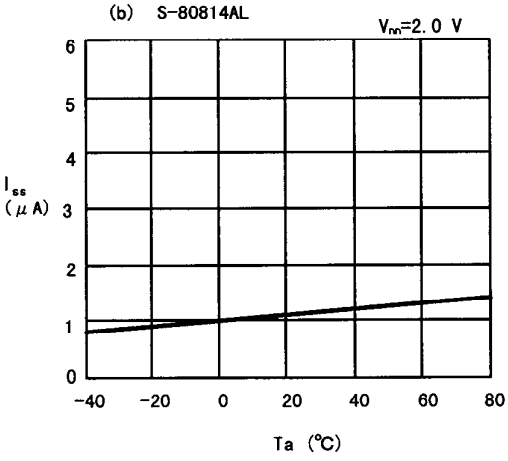


(3) Current consumption (I_{SS}) – Temperature (Ta)

(a) S-80808AL

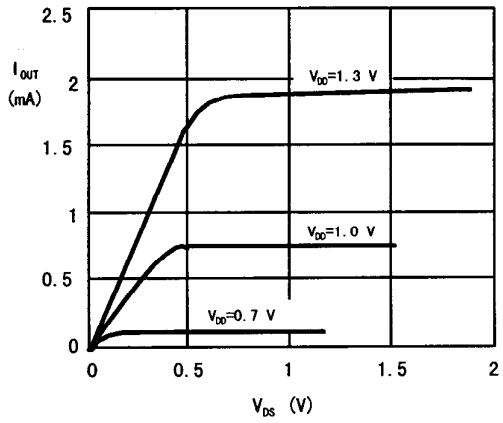


(b) S-80814AL



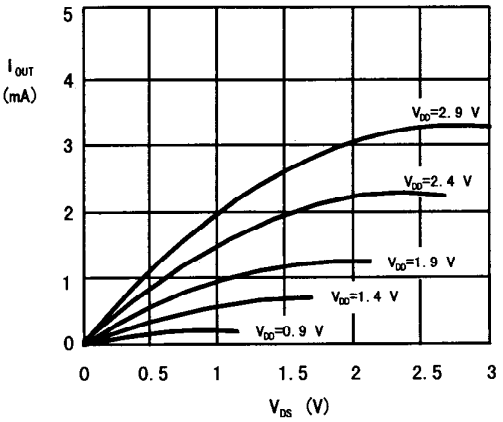
(4) Nch transistor output current (I_{OUT}) - V_{DS}

(a) S-80814AL



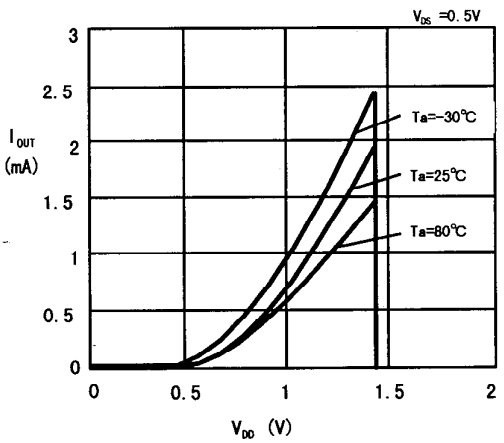
(5) Pch transistor output current (I_{OUT}) - V_{DS}

(b) S-80808AL



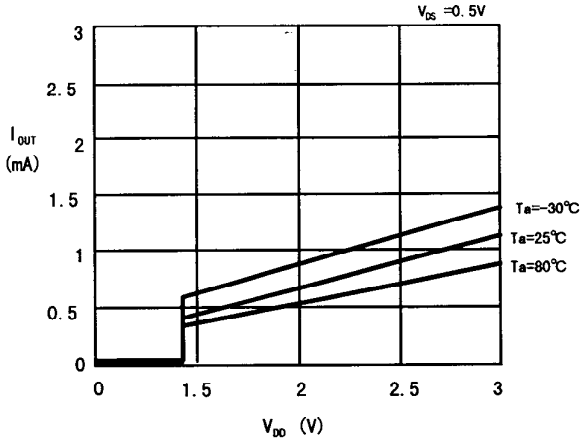
(6) Nch transistor output current (I_{OUT})
- Input voltage (V_{DD})

(a) S -80814AL



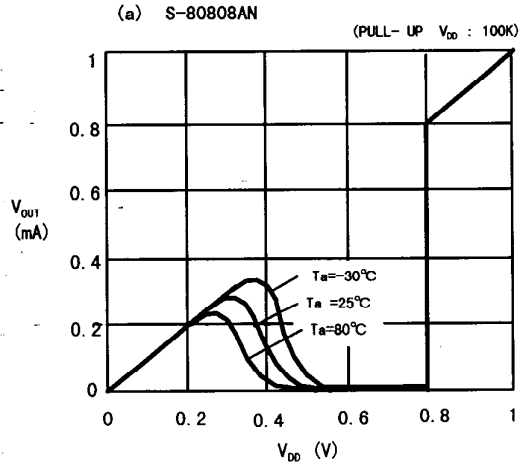
(7) Pch transistor output current (I_{OUT})
- Input voltage (V_{DD})

(b) S-80814AL

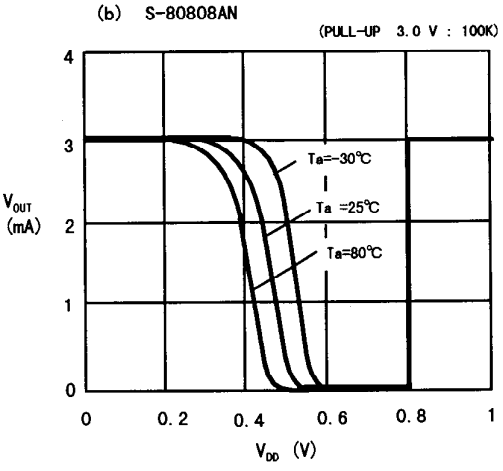


(8) Minimum operating voltage

(a) S-80808AN

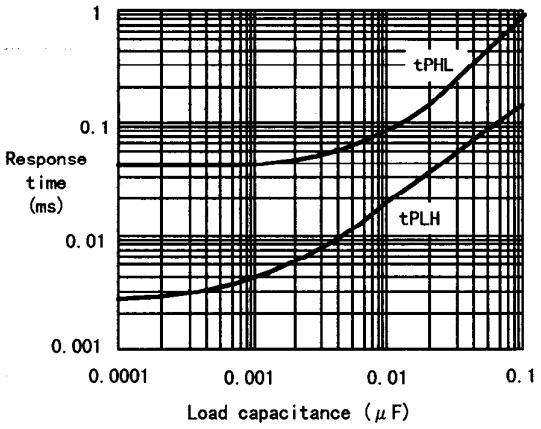


(b) S-80808AN

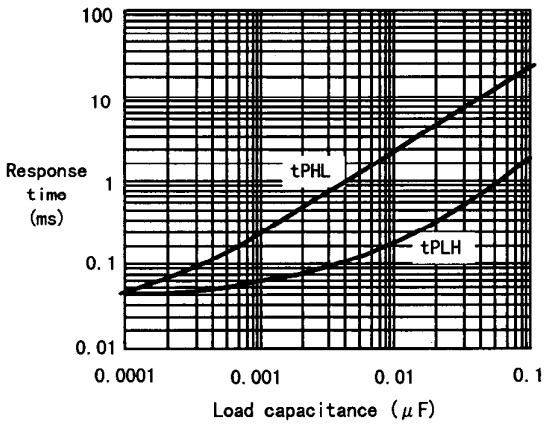


(9) Dynamic response

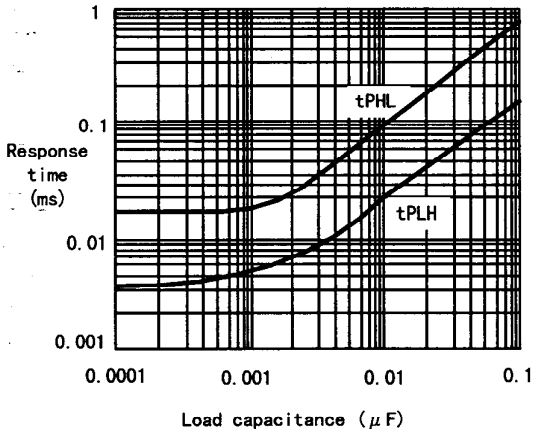
(a) S-80808AL



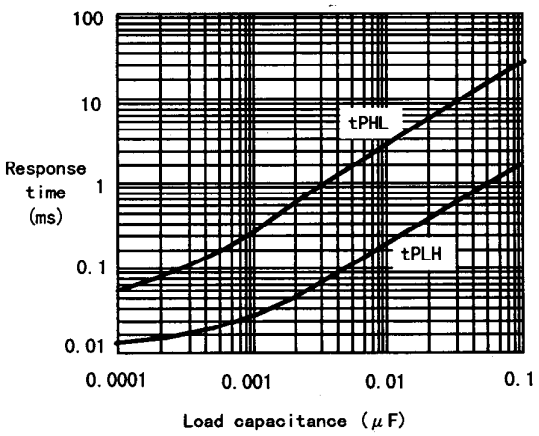
(b) S-80808AN



(c) S-80814AL



(d) S-80814AN



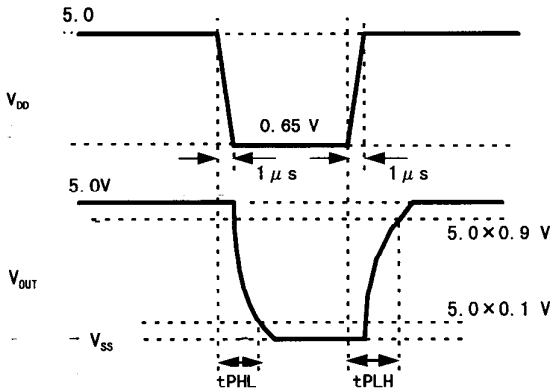
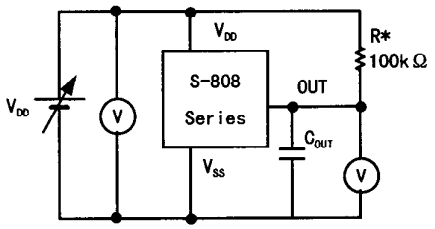


Figure 18 Measuring conditions



* R is unnecessary for CMOS output products.

Figure 19 Measuring circuit

■ Application Circuit Examples

1. Microcomputer reset circuits

If the power supply voltage to a microcomputer falls below the specified level, an unspecified operation may be performed or the contents of the memory register may be lost. When power supply voltage returns to normal, the microcomputer needs to be initialized before normal operations can be done.
Reset circuits protect microcomputers in the event of current being momentarily switched off or lowered.
With the S-808 Series which has a low operating voltage, a high-precision detection voltage and hysteresis characteristic, the reset circuits shown in Figures 20 to 21 can be easily constructed.

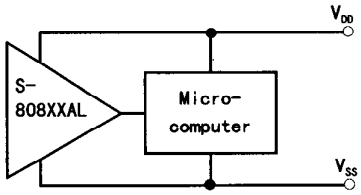
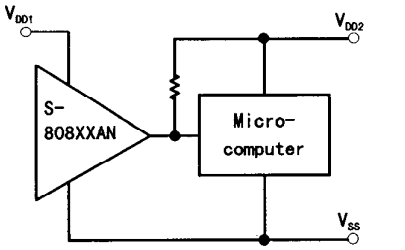


Figure 20

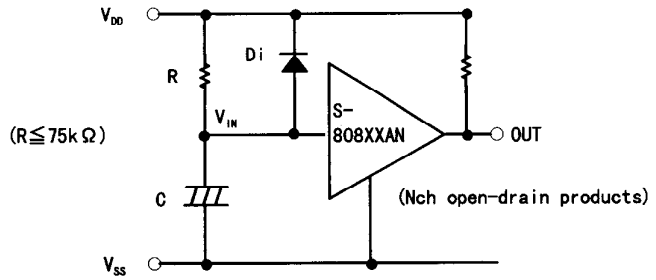


(Nch open-drain output products only)

Figure 21

2. Addition of power-on reset circuit

A power-on reset circuit can be constructed using Nch open-drain product of S-808 Series.



Note 1: R should be 75 kΩ or less for purpose of protection against oscillation.
Note 2: Di instantaneously discharges the electric charge stored by C at the falling of the power.
Di is not necessary if delay in falling time is normal.

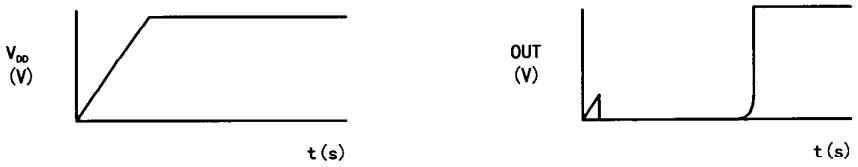


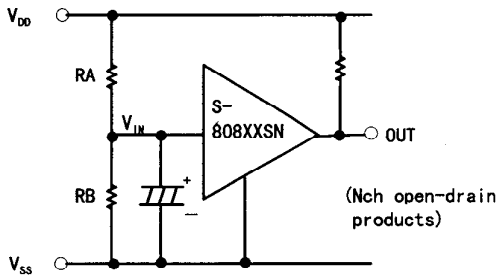
Figure 22

Note 3: When the power steeply rises, output may goes high for a instant due to the IC inconstant region characteristics (output voltage is unstable in the region under minimum operating voltage) as shown in Fig. 23.

Figure 23

3. Change of detection voltege

In Nch open-drain output products of the S-808 Series, detection voltage can be changed using resistance dividers or diodes as shown in Figures 24 and 25. In Figure 24, hysteresis width is also changed.

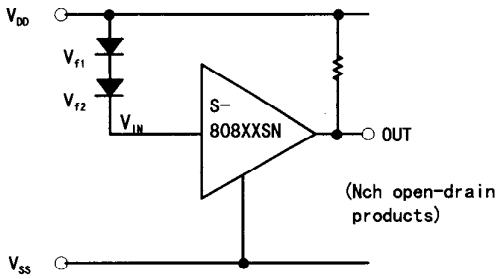


$$\text{Detection voltage} = \frac{RA+RB}{RB} \cdot -V_{DET}$$

$$\text{Hysteresis width} = \frac{RA+RB}{RB} \cdot V_{HYS}$$

Note1: If RA and RB are large, the hysteresis width may be larger than the value given by the formula above due to through type current (which flows slightly in Nch open-drain circuit).
Note2: RA should be 75kΩ or less for purpose of protection against oscillation.

Figure 24



$$\text{Detection voltage} = V_{f1}+V_{f2}+(-V_{DET})$$

Figure 25

■ Notes

- In CMOS output products of the S-808 Series, through type current flows when the device is detecting or releasing. If a high impedance is connected to the input, oscillation may be caused due to the fall of the voltage by the through type current when lowering the voltage during releasing.

- When designing for mass production using an application circuit described herein, take the product deviation and temperature characteristic into consideration.

- Seiko Instruments Inc. shall not bear any responsibility for the patents on the circuits described herein.