

HC4020 14 STAGE BINARY COUNTER
HC4040 12 STAGE BINARY COUNTER

- HIGH SPEED
f_{MAX} = 73 MHz (TYP.) at V_{CC} = 5 V
- LOW POWER DISSIPATION
I_{CC} = 4 μA (MAX.) at T_A = 25 °C
- HIGH NOISE IMMUNITY
V_{NIH} = V_{NIL} = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
|I_{OH}| = I_{OL} = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
V_{CC} (OPR) = 2 V to 6 V
- PIN AND FUNCTION COMPATIBLE WITH
4020B/4040B



DESCRIPTION

The M54/74HC4020/HC4040 are high speed CMOS 14/12-STAGE BINARY COUNTER fabricated in silicon gate C²MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low consumption.

A clear input is used to reset the counter to the all low level state. A high level on CLEAR accomplishes the reset function. A negative transition on the CLOCK input increments the counter by one.

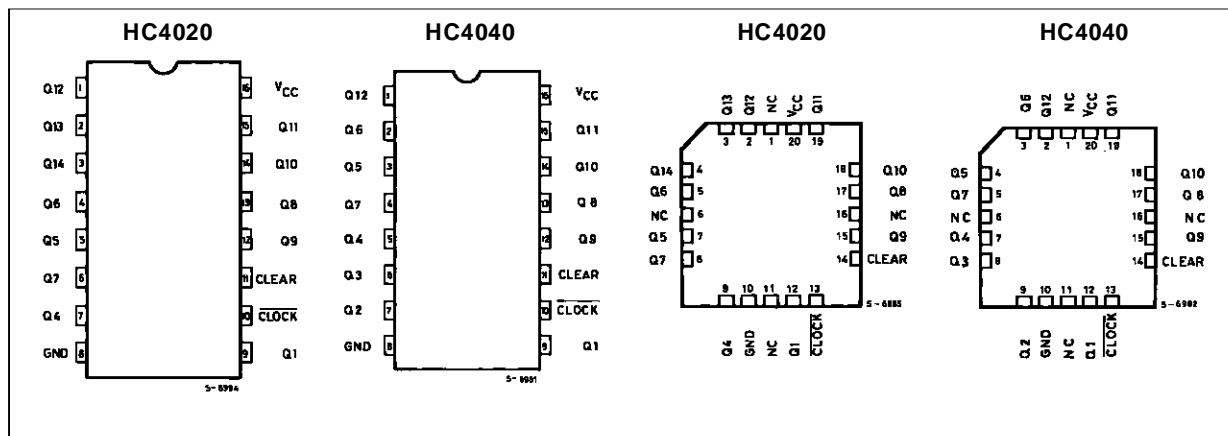
For HC4020 twelve kind of divided output are provided; 1st and 4th stage to 14th stage.

The maximum division available at last stage is 1/16384 x f_{IN} at clock.

For HC4040 each division stage has an output; the final frequency is 1/4096 x f_{IN}.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION (top view)



M54/M74HC4020/4040

INPUT AND OUTPUT EQUIVALENT CIRCUIT



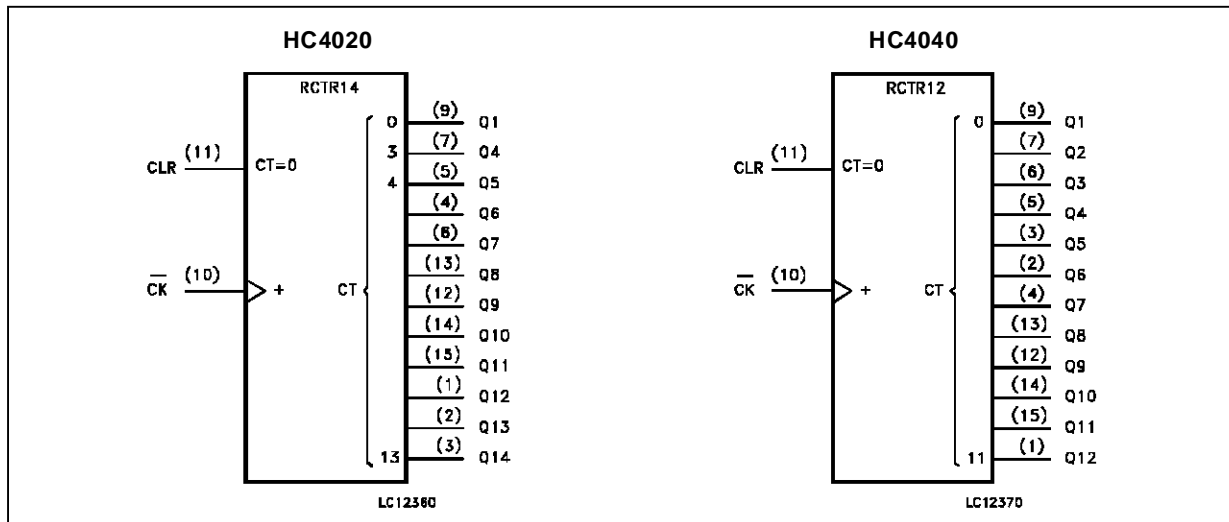
PIN DESCRIPTION (HC4020)

PIN No	SYMBOL	NAME AND FUNCTION
9, 7, 6, 5, 3, 2, 4, 13, 12, 14, 15, 1	Q1, Q4 to Q14	Parallel Outputs
10	$\overline{\text{CLOCK}}$	Clock Input (LOW to HIGH, edge triggered)
11	CLEAR	Reset Inputs
8	GND	Ground (0V)
16	V _{CC}	Positive Supply Voltage

PIN DESCRIPTION (HC4040)

PIN No	SYMBOL	NAME AND FUNCTION
9, 7, 6, 5, 3, 2, 4, 13, 12, 14, 15, 1	Q1 to Q12	Parallel Outputs
10	$\overline{\text{CLOCK}}$	Clock Input (LOW to HIGH, edge triggered)
11	CLEAR	Reset Inputs
8	GND	Ground (0V)
16	V _{CC}	Positive Supply Voltage

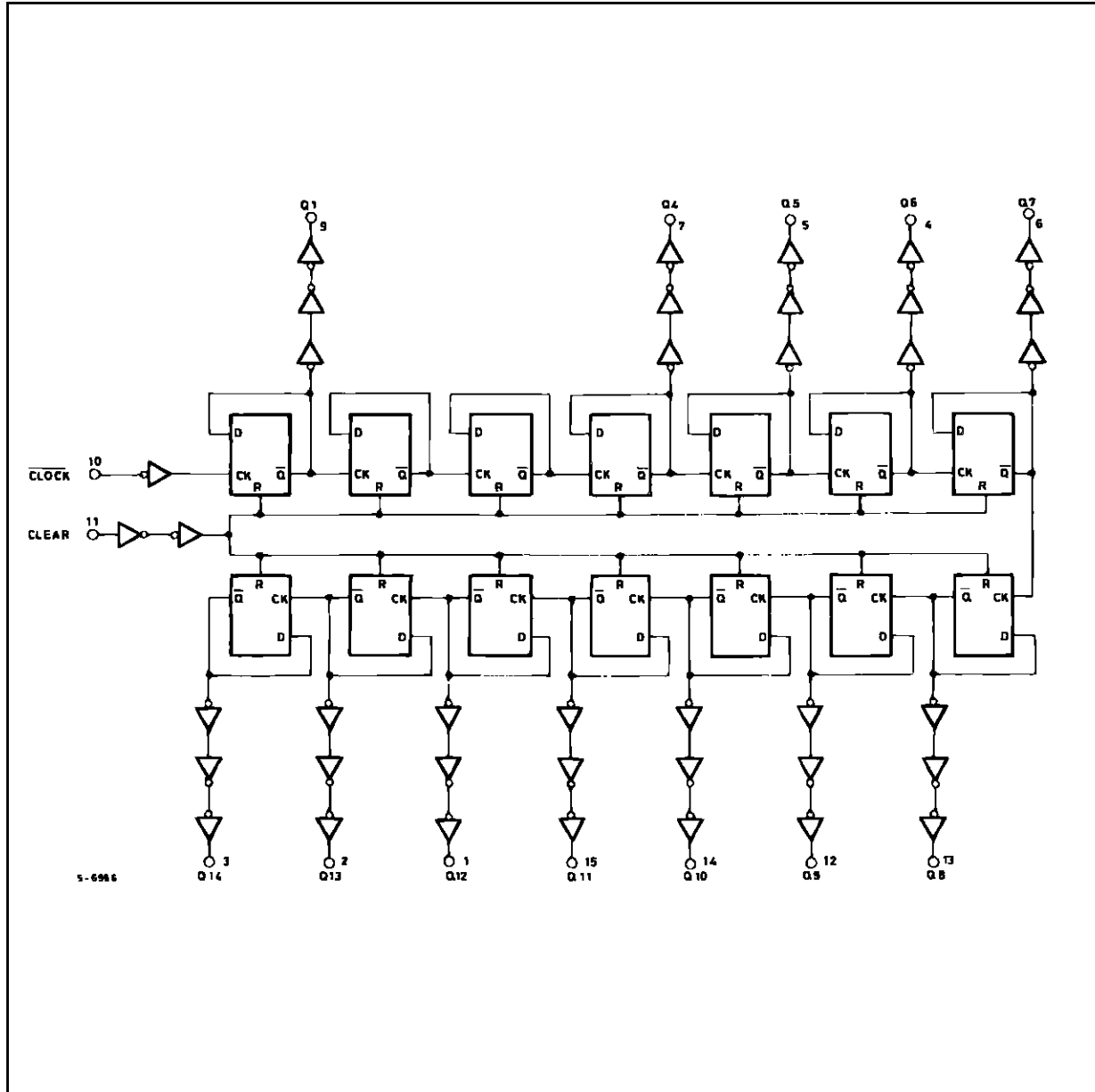
IEC LOGIC SYMBOLS



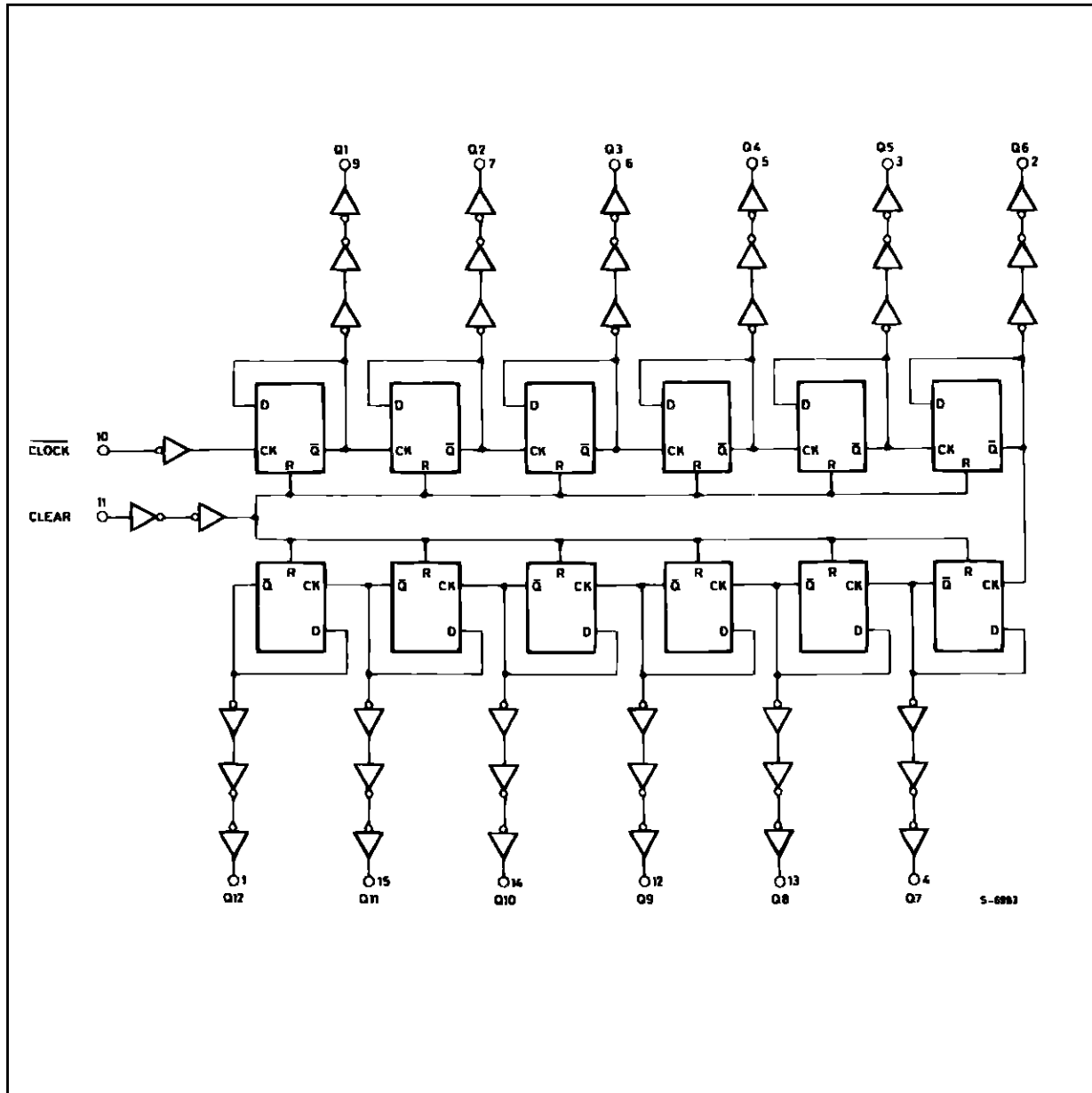
TRUTH TABLE

$\overline{\text{CLOCK}}$	CLEAR	OUTPUT STATE
X	H	ALL OUTPUTS = "L"
	L	NO CHANGE
	L	ADVANCE TO NEXT STATE

LOGIC DIAGRAM (HC4020)



LOGIC DIAGRAM (HC4040)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to +7	V
V _I	DC Input Voltage	-0.5 to V _{CC} + 0.5	V
V _O	DC Output Voltage	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	± 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Source Sink Current Per Output Pin	± 25	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 50	mA
P _D	Power Dissipation	500 (*)	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	2 to 6	V
V _I	Input Voltage	0 to V _{CC}	V
V _O	Output Voltage	0 to V _{CC}	V
T _{op}	Operating Temperature: M54HC Series	-55 to +125	°C
	M74HC Series	-40 to +85	°C
t _r , t _f	Input Rise and Fall Time	V _{CC} = 2 V 0 to 1000	ns
		V _{CC} = 4.5 V 0 to 500	
		V _{CC} = 6 V 0 to 400	

DC SPECIFICATIONS

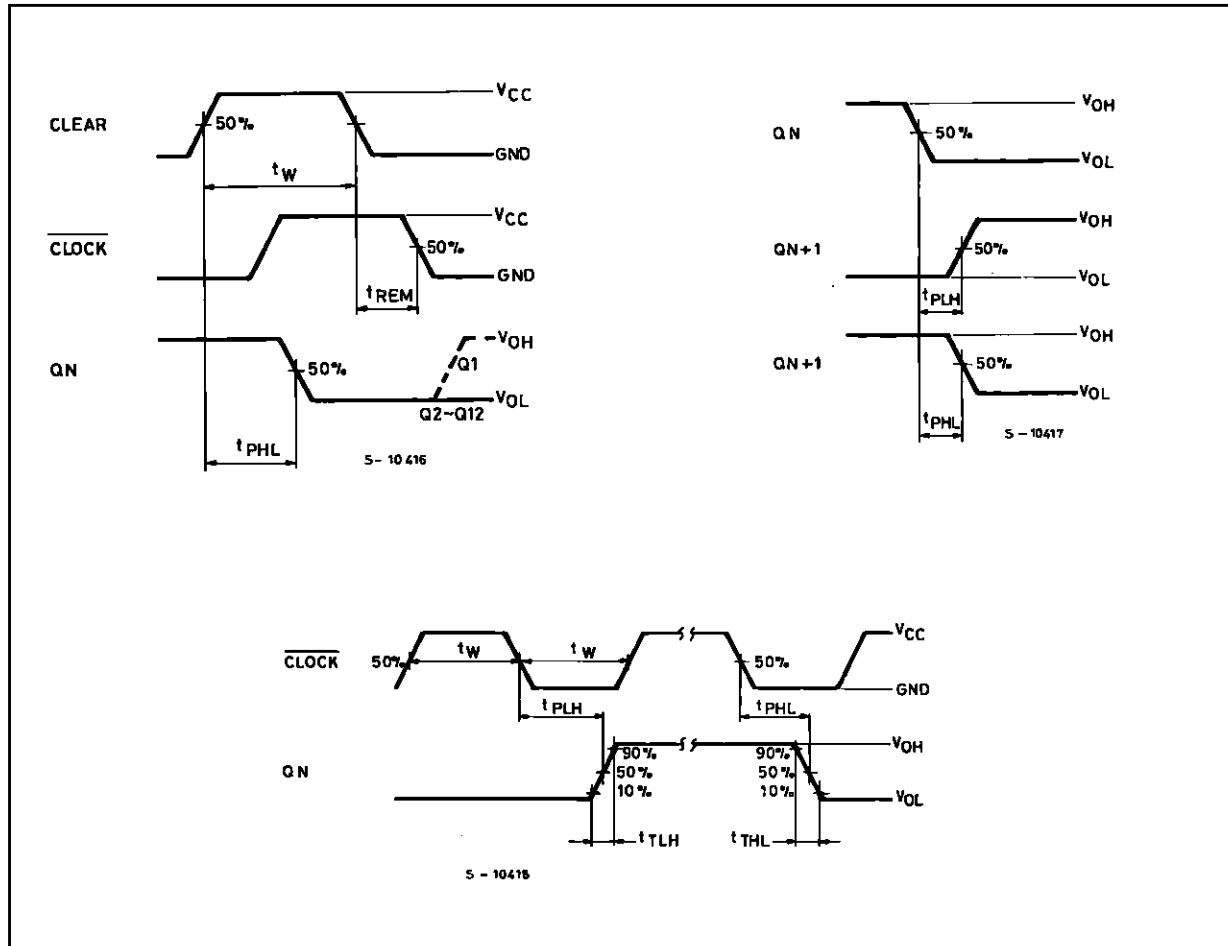
Symbol	Parameter	Test Conditions		Value						Unit		
		V _{CC} (V)		T _A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC			
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.	
V _{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5	V		
		4.5		3.15			3.15		3.15			
		6.0		4.2			4.2		4.2			
V _{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V	
		4.5				1.35		1.35		1.35		
		6.0				1.8		1.8		1.8		
V _{OH}	High Level Output Voltage	2.0	V _I = V _{IH} or V _{IL}	I _O = -20 μA	1.9	2.0		1.9		1.9	V	
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5	I _O = -4.0 mA	4.18	4.31		4.13		4.10			
		6.0		I _O = -5.2 mA	5.68	5.8		5.63		5.60		
V _{OL}	Low Level Output Voltage	2.0	V _I = V _{IH} or V _{IL}	I _O = 20 μA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I _O = 4.0 mA		0.17	0.26		0.33		0.40	
		6.0			I _O = 5.2 mA		0.18	0.26		0.33		
I _I	Input Leakage Current	6.0	V _I = V _{CC} or GND			±0.1		±1		±1	μA	
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND			4		40		80	μA	

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

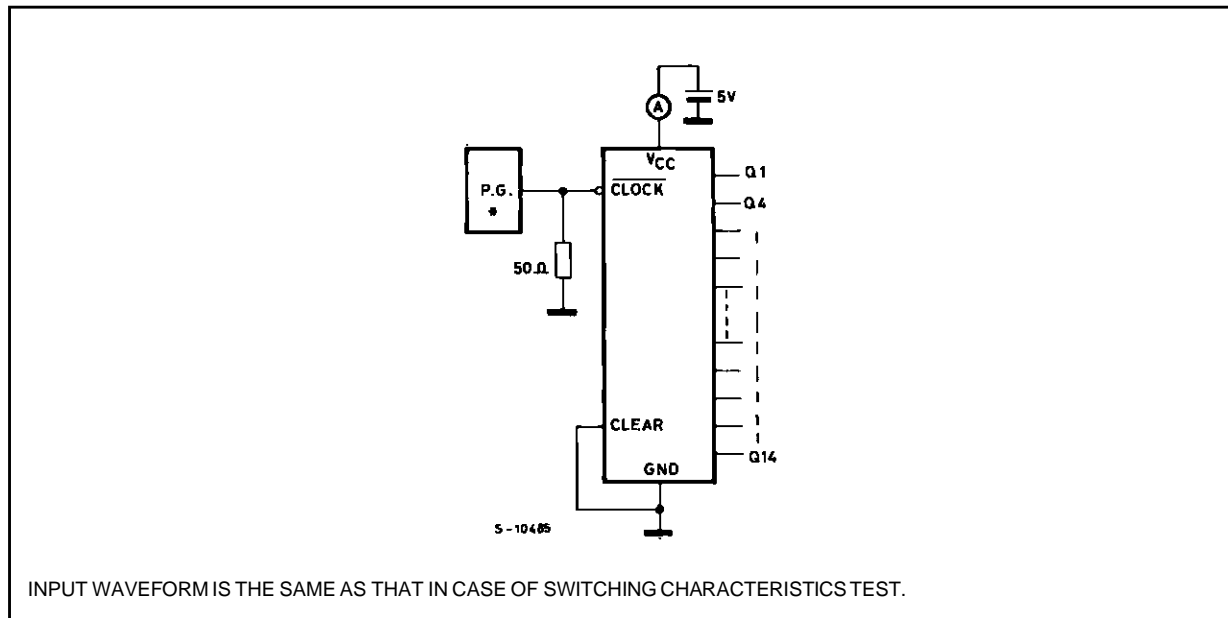
Symbol	Parameter	Test Conditions		Value						Unit	
		V _{CC} (V)		T _A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t _{TLH} t _{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t _{PLH} t _{PHL}	Propagation Delay Time (Q _n - Q _{n+1})	2.0			20	50		65		75	ns
		4.5			5	10		13		15	
		6.0			4	9		11		13	
t _{PLH} t _{PHL}	Propagation Delay Time (CLOCK Q1)	2.0	for HC4020		76	145		180		220	ns
		4.5			21	29		36		44	
		6.0			18	25		31		38	
t _{PLH} t _{PHL}	Propagation Delay Time (CLOCK Q1)	2.0	for HC4040		48	145		180		220	ns
		4.5			17	29		36		44	
		6.0			13	25		31		38	
t _{PHL}	Propagation Delay Time (CLEAR - Q _n)	2.0	for HC4020		60	140		175		210	ns
		4.5			18	28		35		42	
		6.0			15	24		30		36	
t _{PHL}	Propagation Delay Time (CLEAR - Q _n)	2.0	for HC4040		56	140		175		210	ns
		4.5			18	28		35		42	
		6.0			15	24		30		36	
f _{MAX}	Maximum Clock Frequency	2.0		6.0	15		4.8		4		MHz
		4.5		30	65		24		20		
		6.0		35	70		28		24		
t _{W(H)} t _{W(L)}	Minimum Pulse Width (CLOCK)	2.0			40	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t _{W(H)}	Minimum Pulse Width (CLEAR)	2.0	for HC4020		32	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t _{W(H)}	Minimum Pulse Width (CLEAR)	2.0	for HC4040		70	175		220		265	ns
		4.5			19	35		44		53	
		6.0			16	30		37		45	
t _{REM}	Minimum Removal Time	2.0	for HC4020		0			0		0	ns
		4.5			0			0		0	
		6.0			0			0		0	
t _{REM}	Minimum Removal Time	2.0	for HC4040		25			30		40	ns
		4.5			5			6		8	
		6.0			5			5		7	
C _{IN}	Input Capacitance				5	10		10			pF
C _{PD} (*)	Power Dissipation Capacitance				34						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. I_{CC(opr)} = C_{PD} • V_{CC} • f_{IN} + I_{CC/2} (per FLIP/FLOP)

SWITCHING CHARACTERISTICS TEST WAVEFORM



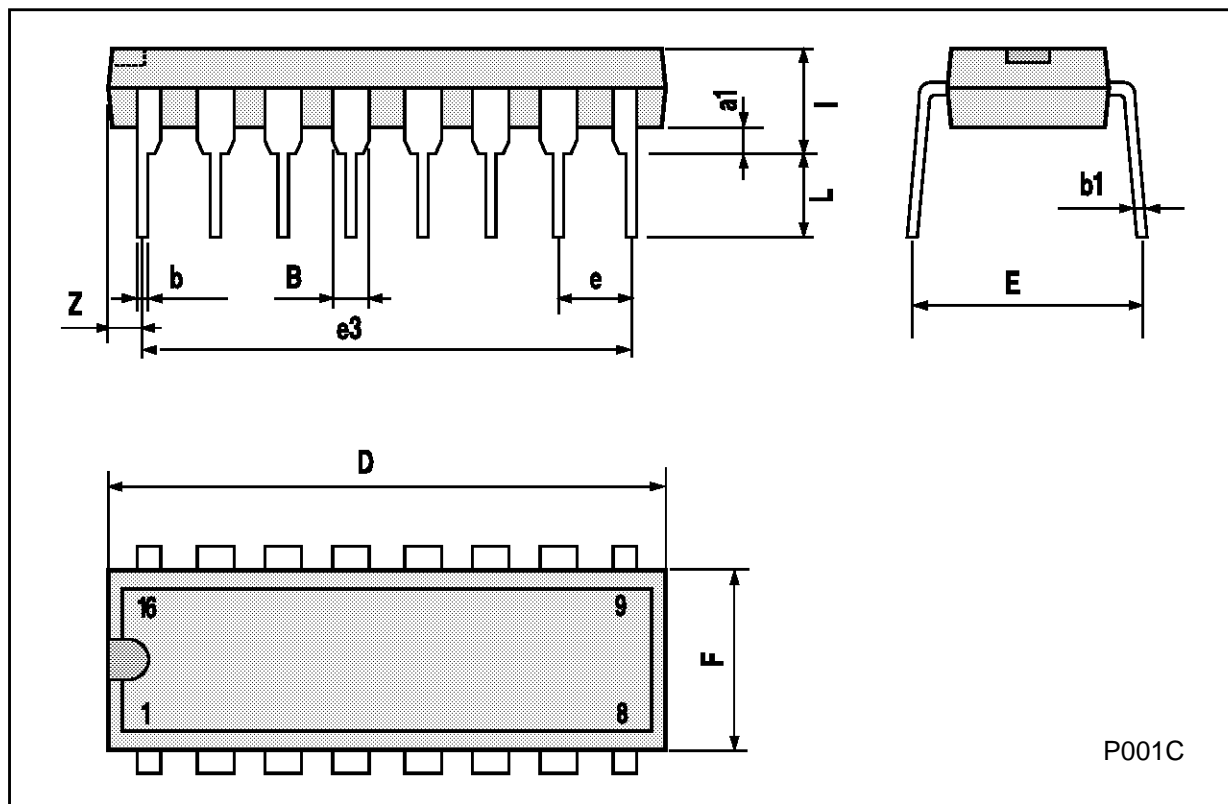
TEST CIRCUIT I_{cc} (Opr.)



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

Plastic DIP16 (0.25) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

Ceramic DIP16/1 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			20			0.787
B			7			0.276
D		3.3			0.130	
E	0.38			0.015		
e3		17.78			0.700	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
H	1.17		1.52	0.046		0.060
L	0.22		0.31	0.009		0.012
M	0.51		1.27	0.020		0.050
N			10.3			0.406
P	7.8		8.05	0.307		0.317
Q			5.08			0.200



SO16 (Narrow) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



P013H

PLCC20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	



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