

# DATA SHEET

## **PDTC115E series**

**NPN resistor-equipped transistors;**

**R1 = 100 k $\Omega$ , R2 = 100 k $\Omega$**

Product specification  
Supersedes data of 2004 Apr 06

2004 Aug 06

## NPN resistor-equipped transistors; R1 = 100 k $\Omega$ , R2 = 100 k $\Omega$

## PDTC115E series

### FEATURES

- Built-in bias resistors
- Simplified circuit design
- Reduction of component count
- Reduced pick and place costs.

### APPLICATIONS

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver.

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V <sub>CEO</sub>	collector-emitter voltage	–	50	V
I <sub>O</sub>	output current (DC)	–	20	mA
R1	bias resistor	100	–	k $\Omega$
R2	bias resistor	100	–	k $\Omega$

### DESCRIPTION

NPN resistor equipped transistor (see “Simplified outline, symbol and pinning” for package details).

### PRODUCT OVERVIEW

TYPE NUMBER	PACKAGE		MARKING CODE	PNP COMPLEMENT
	PHILIPS	EIAJ		
PDTC115EE	SOT416	SC-75	46	PDTA115EE
PDTC115EEF	SOT490	SC-89	49	PDTA115EEF
PDTC115EK	SOT346	SC-59	56	PDTA115EK
PDTC115EM	SOT883	SC-101	DV	PDTA115EM
PDTC115ES	SOT54 (TO-92)	SC-43	TC115E	PDTA115ES
PDTC115ET	SOT23	–	*44 <sup>(1)</sup>	PDTA115ET
PDTC115EU	SOT323	SC-70	*15 <sup>(1)</sup>	PDTA115EU

### Note

1. \* = p: Made in Hong Kong.  
\* = t: Made in Malaysia.  
\* = W: Made in China.

NPN resistor-equipped transistors;  
 R1 = 100 kΩ, R2 = 100 kΩ

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SIMPLIFIED OUTLINE, SYMBOL AND PINNING

TYPE NUMBER	SIMPLIFIED OUTLINE AND SYMBOL	PINNING	
		PIN	DESCRIPTION
PDTC115ES	<p style="text-align: center;"><i>MAM364</i></p>	1 2 3	base collector emitter
PDTC115EE PDTC115EEF PDTC115EK PDTC115ET PDTC115EU	<p style="text-align: center;">Top view <i>MDB269</i></p>	1 2 3	base emitter collector
PDTC115EM	<p style="text-align: center;">bottom view <i>MHC506</i></p>	1 2 3	base emitter collector

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### ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PDTC115EE	–	plastic surface mounted package; 3 leads	SOT416
PDTC115EEF	–	plastic surface mounted package; 3 leads	SOT490
PDTC115EK	–	plastic surface mounted package; 3 leads	SOT346
PDTC115EM	–	leadless ultra small plastic package; 3 solder lands; body 1.0 × 0.6 × 0.5 mm	SOT883
PDTC115ES	–	plastic single-ended leaded (through hole) package; 3 leads	SOT54
PDTC115ET	–	plastic surface mounted package; 3 leads	SOT23
PDTC115EU	–	plastic surface mounted package; 3 leads	SOT323

### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CBO</sub>	collector-base voltage	open emitter	–	50	V
V <sub>CEO</sub>	collector-emitter voltage	open base	–	50	V
V <sub>EBO</sub>	emitter-base voltage	open collector	–	10	V
V <sub>I</sub>	input voltage positive negative		–	+40	V
			–	–10	V
I <sub>O</sub>	output current (DC)		–	20	mA
I <sub>CM</sub>	peak collector current		–	100	mA
P <sub>tot</sub>	total power dissipation SOT54 SOT23 SOT346 SOT323 SOT416 SOT883 SOT490	T <sub>amb</sub> ≤ 25 °C			
		note 1	–	500	mW
		note 1	–	250	mW
		note 1	–	250	mW
		note 1	–	200	mW
		note 1	–	150	mW
		notes 2 and 3	–	250	mW
notes 1 and 2	–	250	mW		
T <sub>stg</sub>	storage temperature		–65	+150	°C
T <sub>j</sub>	junction temperature		–	150	°C
T <sub>amb</sub>	operating ambient temperature		–65	+150	°C

### Notes

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60  $\mu$ m copper strip line.

NPN resistor-equipped transistors;  
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### THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air		
	SOT54	note 1	250	K/W
	SOT23	note 1	500	K/W
	SOT346	note 1	500	K/W
	SOT323	note 1	625	K/W
	SOT416	note 1	833	K/W
	SOT833	notes 2 and 3	500	K/W
SOT490	notes 1 and 2	500	K/W	

### Notes

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60  $\mu\text{m}$  copper strip line.

### CHARACTERISTICS

T<sub>amb</sub> = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I <sub>CBO</sub>	collector-base cut-off current	V <sub>CB</sub> = 50 V; I <sub>E</sub> = 0 A	–	–	100	nA
I <sub>CEO</sub>	collector-emitter cut-off current	V <sub>CE</sub> = 30 V; I <sub>B</sub> = 0 A	–	–	1	$\mu\text{A}$
		V <sub>CE</sub> = 30 V; I <sub>B</sub> = 0 A; T <sub>j</sub> = 150 °C	–	–	50	$\mu\text{A}$
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = 5 V; I <sub>C</sub> = 0 A	–	–	50	$\mu\text{A}$
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = 5 V; I <sub>C</sub> = 5 mA	80	–	–	
V <sub>CEsat</sub>	collector-emitter saturation voltage	I <sub>C</sub> = 5 mA; I <sub>B</sub> = 0.25 mA	–	–	150	mV
V <sub>i(off)</sub>	input-off voltage	I <sub>C</sub> = 100 $\mu\text{A}$ ; V <sub>CE</sub> = 5 V	–	1.1	0.5	V
V <sub>i(on)</sub>	input-on voltage	I <sub>C</sub> = 1 mA; V <sub>CE</sub> = 0.3 V	3	1.5	–	V
R1	input resistor		70	100	130	k $\Omega$
$\frac{R2}{R1}$	resistor ratio		0.8	1	1.2	
C <sub>c</sub>	collector capacitance	I <sub>E</sub> = i <sub>e</sub> = 0 A; V <sub>CB</sub> = 10 V; f = 1 MHz	–	–	2.5	pF

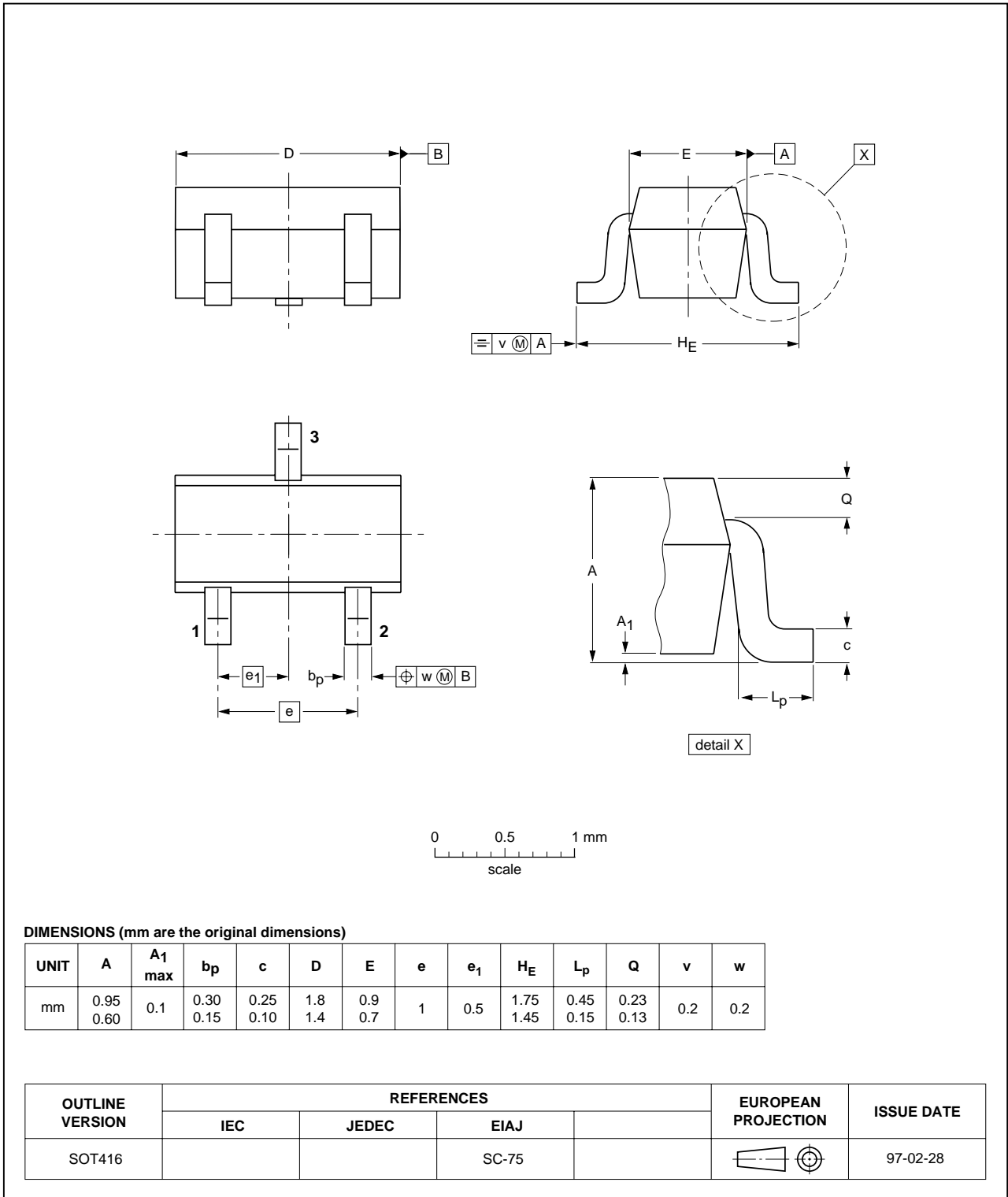
NPN resistor-equipped transistors;  
R1 = 100 kΩ, R2 = 100 kΩ

PDTC115E series

PACKAGE OUTLINES

Plastic surface mounted package; 3 leads

SOT416

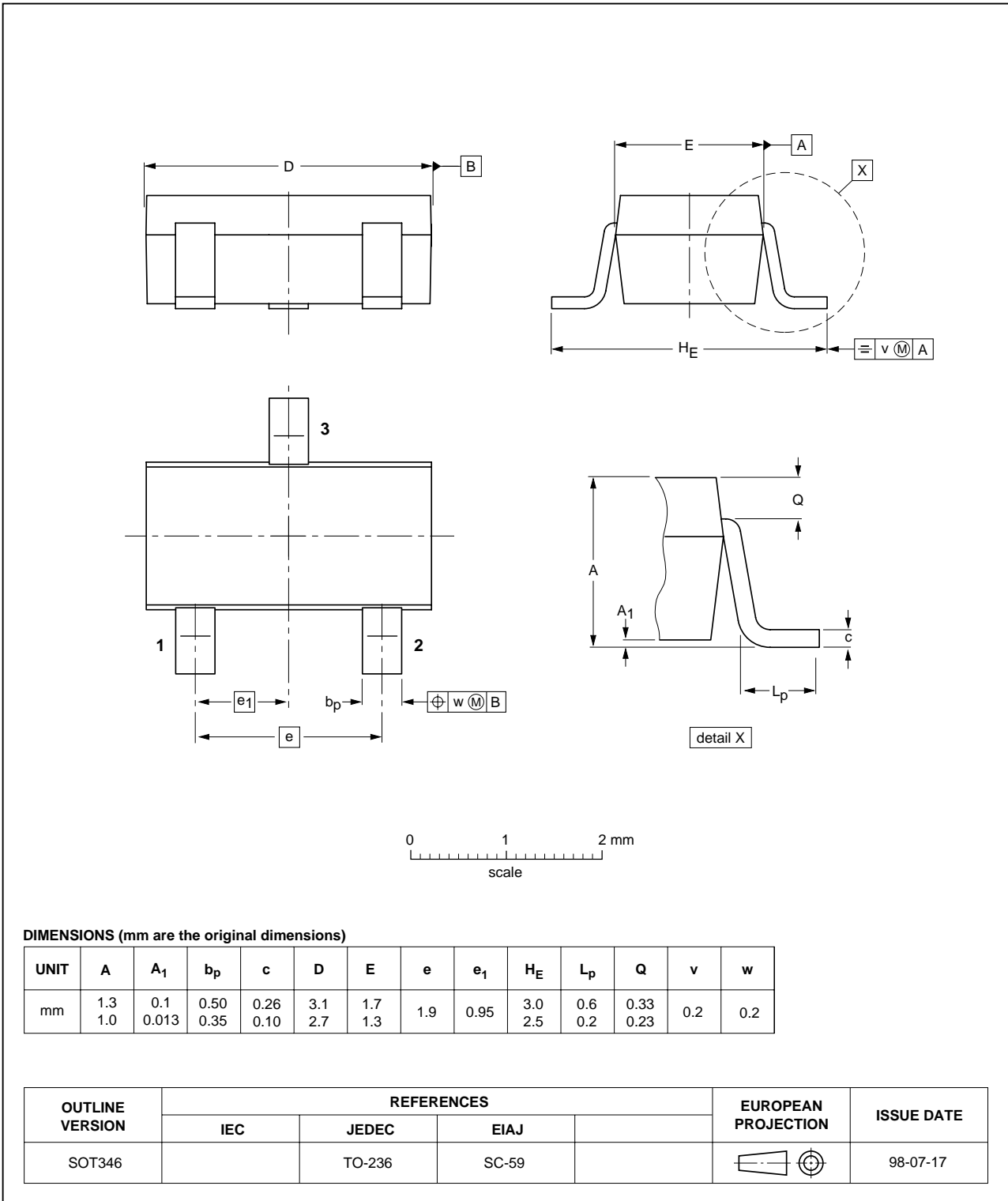


NPN resistor-equipped transistors;  
R1 = 100 kΩ, R2 = 100 kΩ

PDTC115E series

Plastic surface mounted package; 3 leads

SOT346

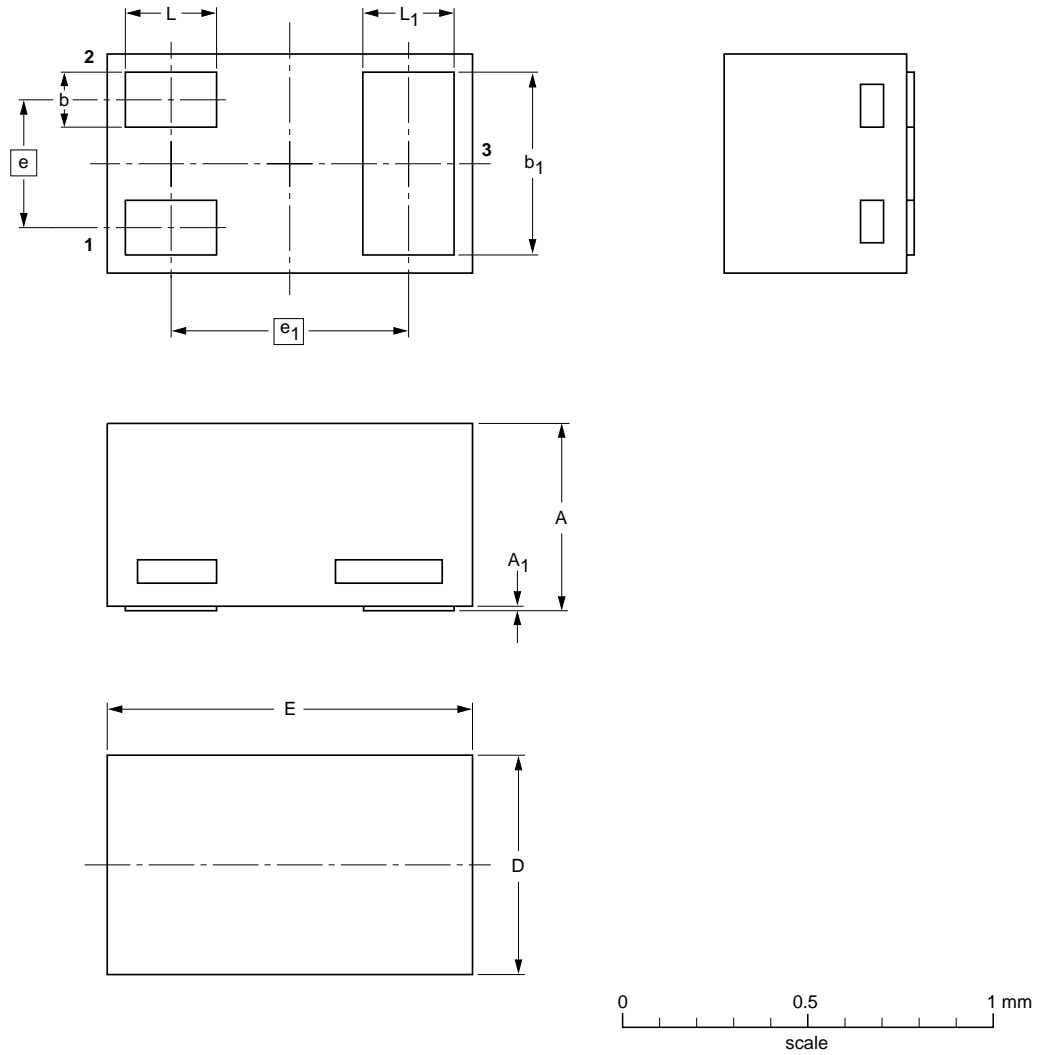


NPN resistor-equipped transistors;  
R1 = 100 kΩ, R2 = 100 kΩ

PDTC115E series

Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.5 mm

SOT883



DIMENSIONS (mm are the original dimensions)

UNIT	A <sup>(1)</sup>	A <sub>1</sub> max.	b	b <sub>1</sub>	D	E	e	e <sub>1</sub>	L	L <sub>1</sub>
mm	0.50 0.46	0.03	0.20 0.12	0.55 0.47	0.62 0.55	1.02 0.95	0.35	0.65	0.30 0.22	0.30 0.22

Note

1. Including plating thickness

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT883			SC-101		03-02-05 03-04-03

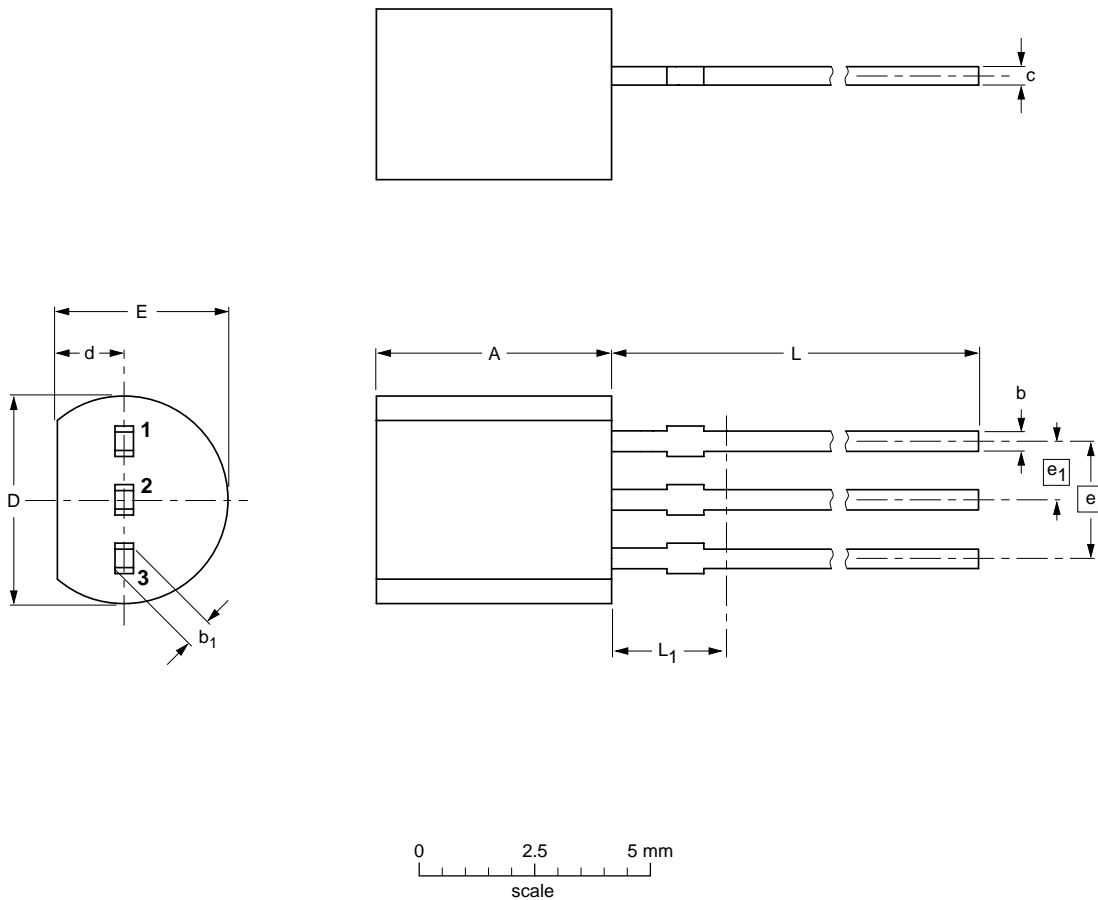


NPN resistor-equipped transistors;  
R1 = 100 kΩ, R2 = 100 kΩ

PDTC115E series

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



**DIMENSIONS (mm are the original dimensions)**

UNIT	A	b	b <sub>1</sub>	c	D	d	E	e	e <sub>1</sub>	L	L <sub>1</sub> <sup>(1)</sup> max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

**Note**

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

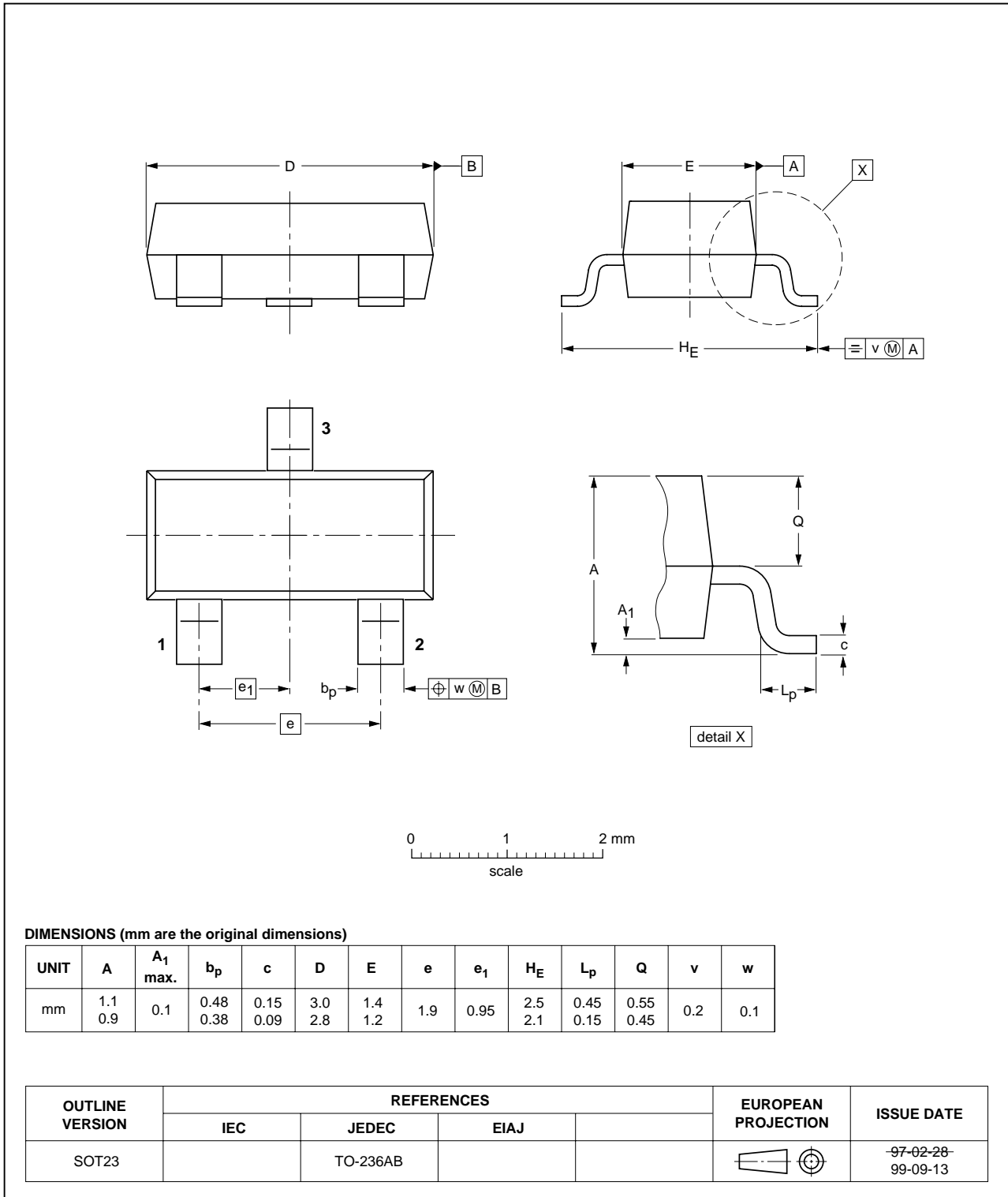
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT54		TO-92	SC-43A		-97-02-28 04-06-28

NPN resistor-equipped transistors;  
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Plastic surface mounted package; 3 leads

SOT23

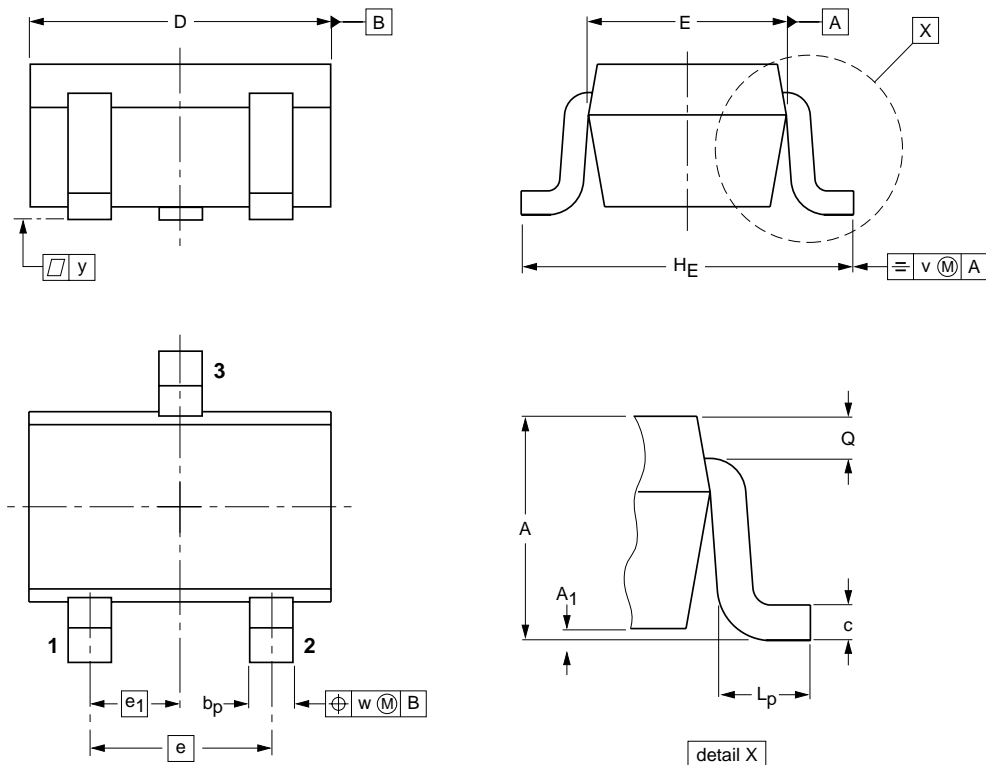


NPN resistor-equipped transistors;  
R1 = 100 kΩ, R2 = 100 kΩ

PDTC115E series

Plastic surface mounted package; 3 leads

SOT323



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w
mm	1.1 0.8	0.1	0.4 0.3	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2

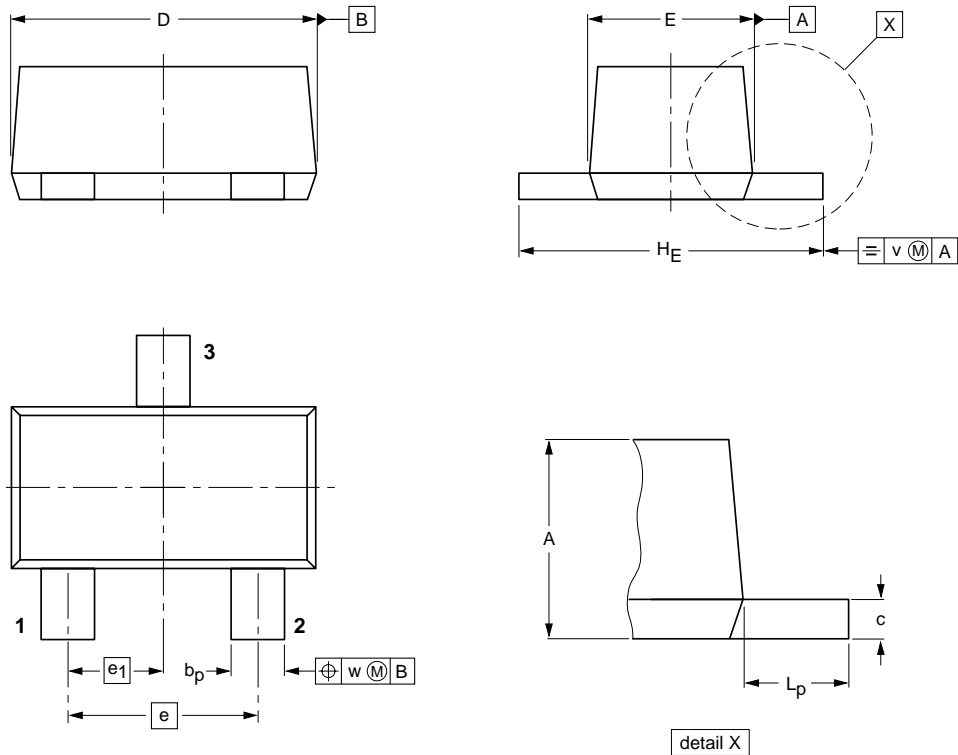
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT323			SC-70			97-02-28

NPN resistor-equipped transistors;  
R1 = 100 kΩ, R2 = 100 kΩ

PDTC115E series

Plastic surface mounted package; 3 leads

SOT490



**DIMENSIONS (mm are the original dimensions)**

UNIT	A	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	v	w
mm	0.8 0.6	0.33 0.23	0.2 0.1	1.7 1.5	0.95 0.75	1.0	0.5	1.7 1.5	0.5 0.3	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT490			SC-89			98-10-23

NPN resistor-equipped transistors;  
R1 = 100 k $\Omega$ , R2 = 100 k $\Omega$

PDTC115E series

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