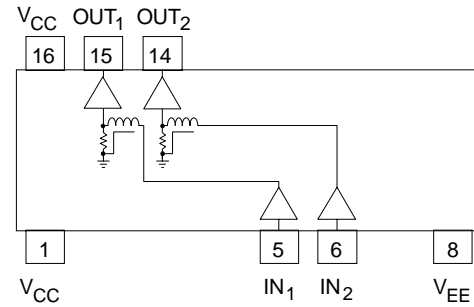


# MECH2B Series

## 10KH ECL Logic Buffered Dual Independent Delays

Also in 10K ECL: MEC2B Series  
For 10KH Triples: MECLH Series

MECH2B Style Schematic



### OPERATING SPECIFICATIONS

$V_{EE}$ Supply Voltage	-5.20 ± 0.25 VDC
$I_{EE}$ Supply Current	65mA typ, 105 mA max.
Logic "1" Input:	
$V_{IH}$	-1.07 V min.
$I_{IH}$	425 $\mu$ A max.
Logic "0" Input:	
$V_{IL}$	-1.48 V max.
$I_{IL}$	0.5 $\mu$ A max.
$V_{OH}$ Logic "1" Voltage Out	-1.02 V min.
$V_{OL}$ Logic "0" Voltage Out	-1.60 V max.
$T_{RO}$ Output Rise Time	< 3.00 ns typ.
Minimum Input Pulse Width, $P_{WI}$	100% of total delay, min.
Operating Temperature Range	0° to +75°C
Storage Temperature Range	-65° to +150°C

Electrical Specifications at 25°C)

Delay Tolerance (ns)	10KH ECL Dual P/N
3 ± 1.0	MECH2B-3
4 ± 1.0	MECH2B-4
5 ± 1.0	MECH2B-5
6 ± 1.0	MECH2B-6
7 ± 1.0	MECH2B-7
8 ± 1.0	MECH2B-8
9 ± 1.0	MECH2B-9
10 ± 1.0	MECH2B-10
11 ± 1.0	MECH2B-11
12.5 ± 1.0	MECH2B-12P5

Delay Tolerance (ns)	10KH ECL Dual P/N
15 ± 1.0	MECH2B-15
20 ± 1.0	MECH2B-20
25 ± 2.0	MECH2B-25
30 ± 2.0	MECH2B-30
35 ± 2.0	MECH2B-35
40 ± 2.0	MECH2B-40
50 ± 2.5	MECH2B-50
60 ± 3.0	MECH2B-60
75 ± 3.75	MECH2B-75
100 ± 5.0	MECH2B-100

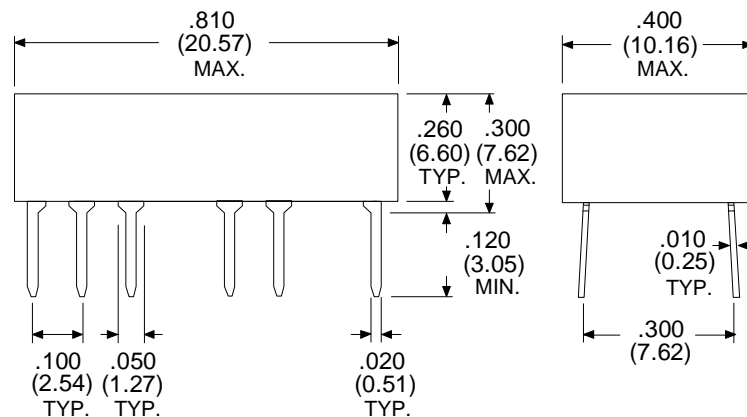
### TEST CONDITIONS

(Measurements made at 25°C)

$V_{EE}$ Supply Voltage	-5.20VDC
Input Pulse Voltage	-.80V to -1.80V
Input Pulse Rise Time	3.00ns max.
Input Pulse Period	4.0 x Total Delay
Input Pulse Duty Cycle	50%
Outputs terminated through 100 $\Omega$ to -2.00 Vdc.	

Package Dimensions: 16 Pin Dual-in-line (Unused leads removed)

Inches (mm)



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Specifications subject to change without notice.

For other values & Custom Designs, contact factory.

MECH2B 2000-01

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