

FUJI Power Supply Control IC

Power Factor Correction

FA5502P/M

Application Note

*June '02
Fuji Electric Co., Ltd.
Matsumoto Factory*

FUJI
ELECTRIC

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CONTENTS

	page
1. Description	4
2. Features	4
3. Outline	4
4. Block diagram	5
5. Pin assignment	5
6. Ratings and characteristics	6
7. Characteristic curves	9
8. Description of each circuit	13
9. Design advice	18
10. Example of application circuit	23

Note

- Parts tolerance and characteristics are not defined in all application described in this Data book. When design an actual circuit for a product, you must determine parts tolerances and characteristics for safe and economical operation.

1. Description

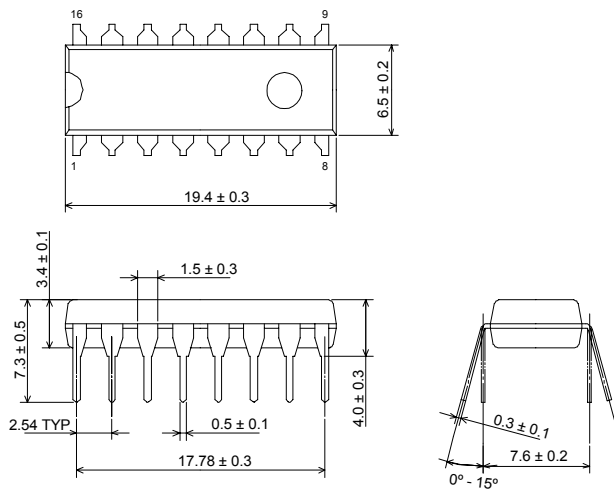
FA5502P/M is a control IC for a power factor correction system. This IC uses a CMOS device with high dielectric strength (30V) to implement low power consumption. This IC uses the average current control system to ensure stable operation. With this system, a power factor of 99% or better can be achieved.

2. Features

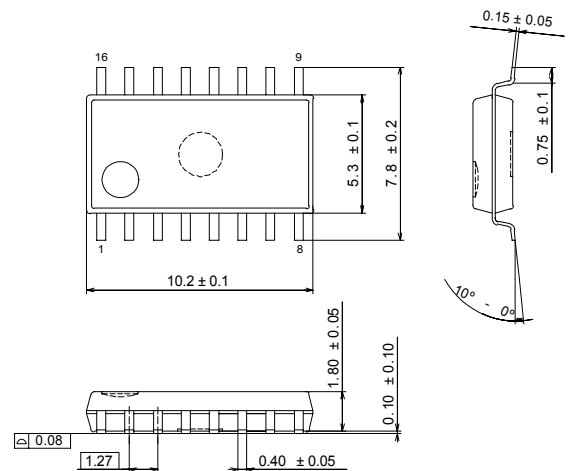
- Low current consumption by CMOS process
- Stand-by : $3\mu\text{A}(\text{max})$, Start-up : $30\mu\text{A}(\text{max})$, Operating : $4\text{mA}(\text{typ})$
- Good regulation of PFC output voltage from no-load to full-load
- Drive circuit for connecting a power MOSFET($I_{\text{OUT}} = \pm 1.5\text{A}$)
- Pulse-by-pulse overcurrent and overvoltage limiting function
- $\pm 2\%$ accuracy reference voltage for setting DC output and overvoltage protection
- Output ON/OFF control function by external signal
- External synchronizing input pin for synchronous operation with other circuits
- Undervoltage lockout function (ON:16.5V, OFF:8.9V)
- 16-pin package (DIP/SOP)

3. Outline

DIP-16 (FA5502P)



SOP-16 (FA5502M)



6. Ratings and characteristics

The contents are subject to change without notice. When using a product, be sure to obtain the latest specifications.

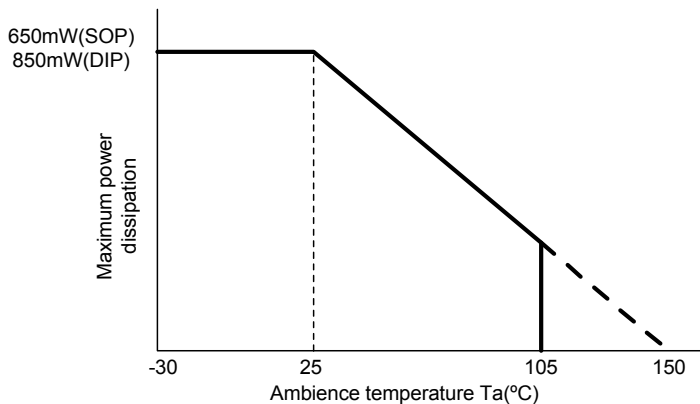
(1) Absolute maximum ratings

Item	Symbol	Rating	Unit
Supply Voltage	VC pin	Vc	V _{cc}
	VCC pin Low impedance source (I _{cc} >15mA)	VCC1	30
	VCC pin Internal zener clamp voltage (I _{cc} <15mA)	VCC2	Self Limiting
Output peak current	I _{OUT}	±1.5	A
SYNC, VIN-, VDET and OVP pins Input voltage	V _{SYNC} V _{VIN-} V _{VDET} V _{OVP}	-0.3 to 5.0	V
IDET pin input voltage	V _{IDET}	-10 to 5.0	V
ON/OFF pin input voltage	V _{ON/OFF}	-0.3 to V _{cc}	V
REF pin source current	I _{REF}	-10	mA
Power dissipation (Ta=25°C)	DIP-16	Pd	850
	SOP-16		650
Ambiance temperature	Ta	-30 to +105	°C
Maximum junction temperature	Tj	+150	°C
Storage temperature	Tstg	-40 to +150	°C

Note) VC and ON/OFF pins voltage must be less than or equal to VCC pin voltage in all the conditions.

Peak current at OUT pin may flow to rated value neither according to supply voltage nor temperature conditions.

Maximum dissipation curve



(2) Recommended operating conditions

Item	Symbol	MIN	TYP.	MAX	Unit
Supply voltage	V _{cc} , Vc	10		28	V
IDET pin input voltage	V _{IDET}	-1.0		0	V
VDET pin input voltage	V _{VDET}	0		2.4	V
VDET pin peak input voltage	V _{PVDET}	0.65		2.4	V
Oscillation frequency	f _{OSC}	15		150	kHz
Oscillation timing capacitance	C _T	330		1000	pF
Oscillation timing resistance	R _T	10		75	kΩ
Noise filter resistance connected to IDET pin	R _n	0		27	Ω
REF-GND capacitance	C _{ref}	0.1	0.47		μF

Note) If the synchronous operation is not necessary, connect the SYNC pin to GND.

(3) Electrical Characteristics (Unless otherwise specified, $V_{CC}=V_C=18V$, $T_a=25^\circ C$, $C_T=470pF$, $R_T=22k\Omega$)**Reference voltage section (REF pin)**

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Output voltage	VREF		4.8	5	5.2	V
Line regulation	Vrdv	$V_{CC}=10$ to 28V			± 25	mV
Load regulation	Vrdi	$I_{Load}=0.1$ to 2mA	-50	-25		mV
Temperature stability	Vrdt	$T_a=-30$ to $105^\circ C$		± 0.5		mV/ $^\circ C$

Oscillator section (CT, SYNC pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Oscillation frequency	fosc	$C_T=470pF$, $R_T=22k\Omega$, $T_a=25^\circ C$	71	78	85	kHz
Voltage stability	fdv	$V_{CC}=10$ to 28V		± 1	± 3	%
Temperature stability	fdt	$T_a=-30$ to $+105^\circ C$		± 0.04	± 0.07	%/ $^\circ C$
Output peak voltage	VOSC			3.4		V
Synchronizing input threshold voltage	VTHSYNC	SYNC pin voltage	1.0	1.5	2.0	V
SYNC pin input current	ISYNC	SYNC pin=2V	75	125	175	μA

Pulse width modulation circuit section (OUT pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Maximum duty cycle	DMAX		91	94	97	%

Overcurrent limiter circuit section (IDET pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Input threshold voltage	VTHOCP	IDET pin voltage	-1.20	-1.10	-1.00	V
Delay time	TpdOCP			150		ns

Soft start circuit section (CS pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Charge current	ICHG	CS pin=0V		-11		μA
Input threshold voltage	VTHCS0	Dutycycle=0%		0.34		V
	VTHCSM	Dutycycle=DMAX		3.40		V

Output ON/OFF control circuit section (ON/OFF pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
On-state input current	ITHON	ON/OFF pin= V_{THON}			± 500	nA
ON/OFF control threshold voltage	VTHON	OFF \rightarrow ON	3.55	3.95	4.35	V
	VTHOFF	ON \rightarrow OFF	2.40	2.80	3.20	V

Voltage error amplifier section (VIN-, VFB pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Reference voltage	Vr		1.519	1.550	1.581	V
Line regulation	Vredv	$V_{CC}=10$ to 28V		± 0.5		mV
Temperature stability	VredT	$T_a=-30$ to $105^\circ C$		± 0.2		mV/ $^\circ C$
Input bias current	I _{BE}				± 500	nA
Open loop gain	A _{ve}		60			dB
Output voltage	VOE+	No load	3.7	4.1		V
	VOE-	No load		50	200	mV
Output source current	IOE+	VFB pin=0V		-2.8		mA
Output sink current	IOE-	VFB pin=2V		280		μA

Current error amplifier section (IIN-, IFB, IDET pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Input threshold voltage	VTHIDET	VDET pin=0V VFB pin=Vr Rn=30Ω	-50	0	50	mV
Input bias current	IBC	IDET pin=0V	-350	-250	-150	μA
Open loop gain	AvC		60			dB
Output voltage	VOC+	No load	3.55	3.8		V
	VOC-	No load		50	200	mV
Output source current	IOC+	IFB pin=0V		-5.1		mA
Output sink current	IOC-	IFB pin=2V		800		μA

Multiplier section (VDET, IIN-, VFB pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
VDET pin input voltage	VMVDET		0		2.4	V
VFB pin input voltage	VMVFB		1.5		3.5	V
Input bias current	IBVDET	VDET pin=0V	-1.5	-0.5		μA
Output current	IM	IIN- pin=0V		-44		μA
Output voltage factor	K			-1.2		-

Overvoltage protection circuit section (OVP pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Input threshold voltage	VTHOVP	OVP pin voltage	1.607	1.640	1.673	V
VTHOVP/Vr ratio	α		1.037	1.058	1.079	-
Input bias current	IBOVP	OVP pin=0V	-1.0	-0.3		μA
Delay time	Tpdovp			150		ns

Undervoltage lockout circuit section (VCC pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Start-up threshold voltage	VTHUON		15.5	16.5	17.5	V
Shutdown threshold voltage	VTHUOFF		8.2	8.9	9.6	V
Hysteresis voltage	VUHYS		6.8	7.6	8.4	V

Output circuit section (OUT, VC pin)

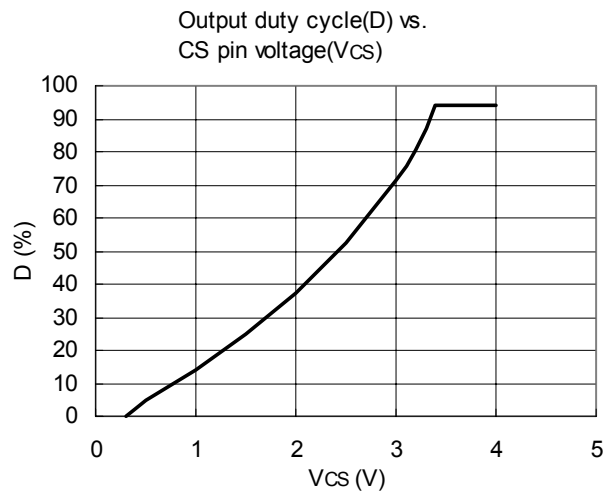
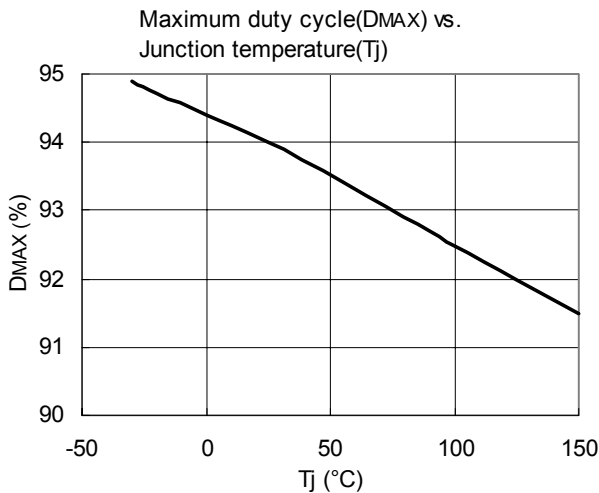
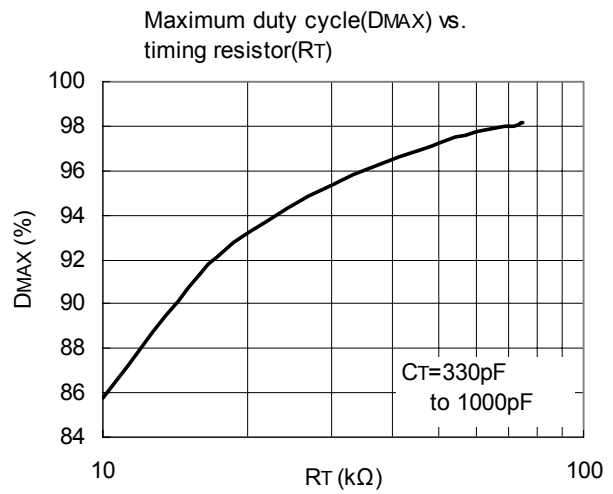
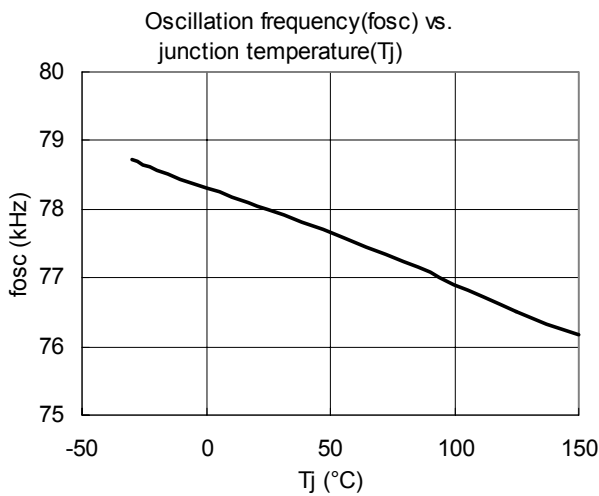
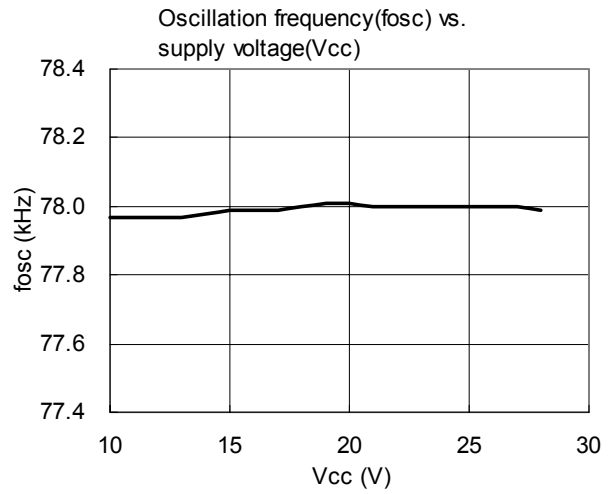
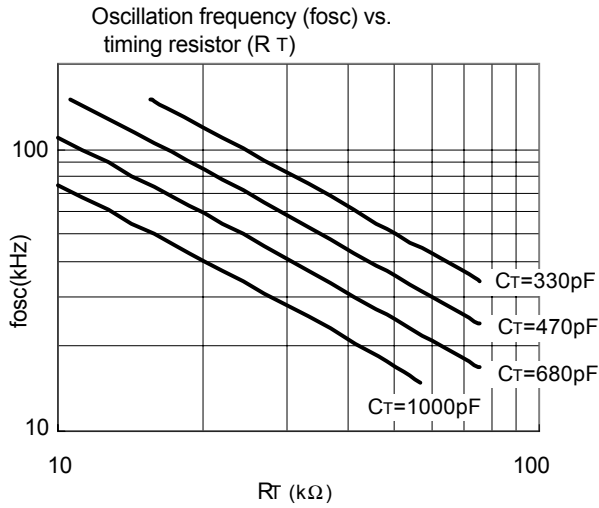
Item	Symbol	Condition	MIN	TYP	MAX	Unit
Low output voltage	VOL	IOL=100mA		0.5	1.0	V
High output voltage	VOH	IOH=-100mA, Vcc=18V	15.5	16.5		V
Rise time	tr	No load		50		ns
Fall time	tf	No load		50		ns

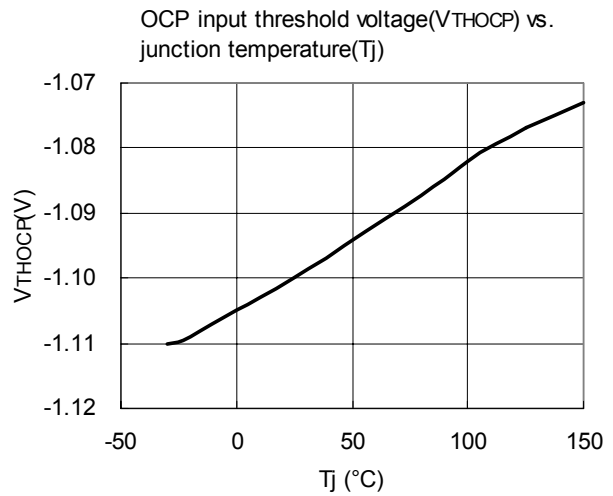
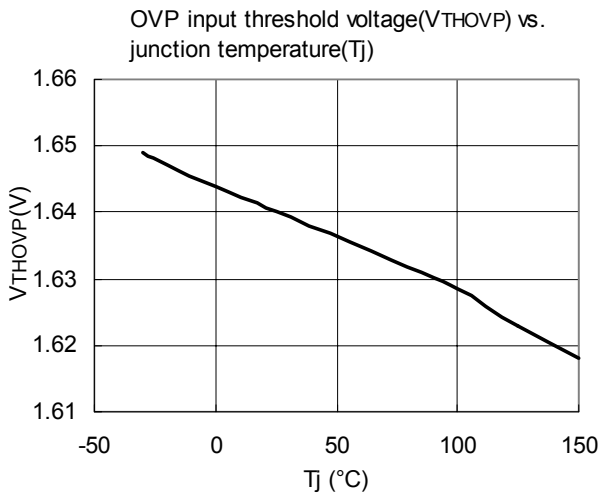
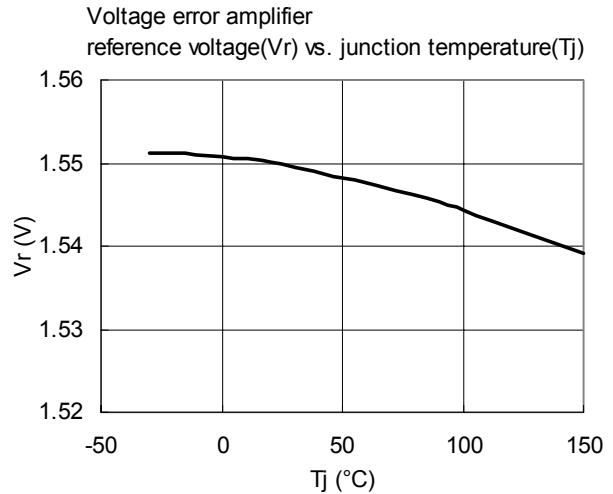
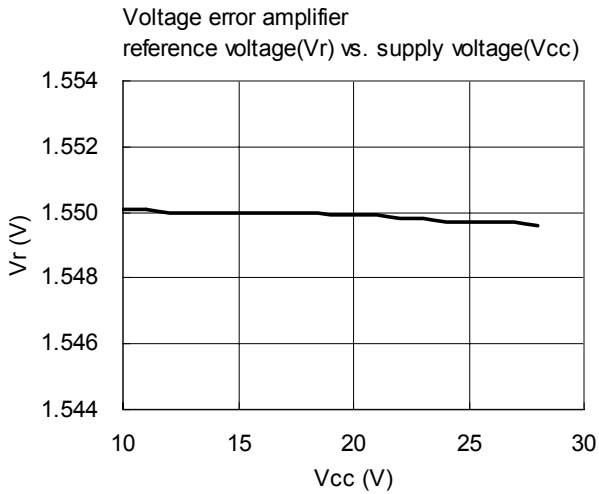
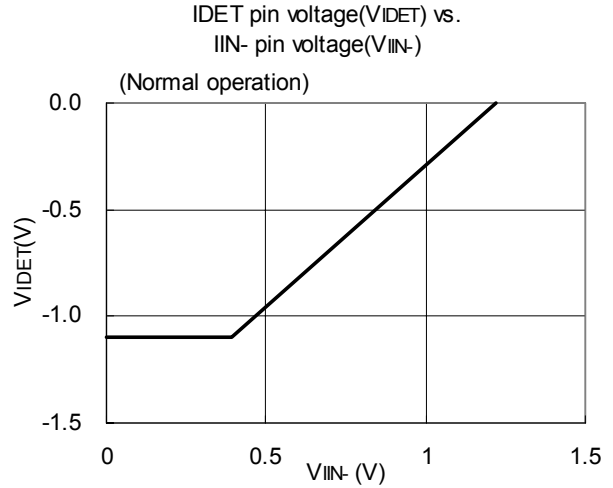
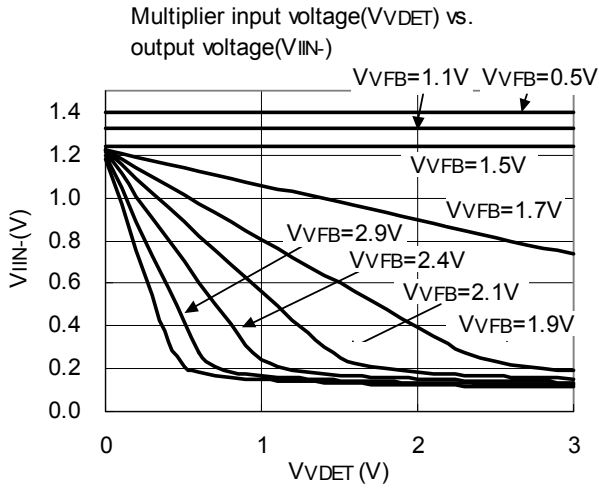
Power supply current (VCC pin)

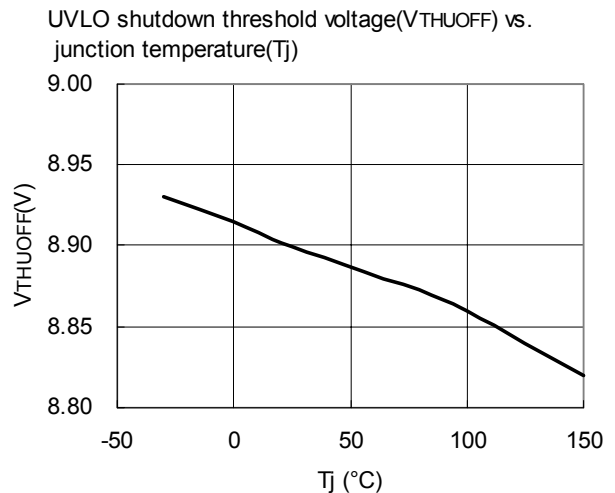
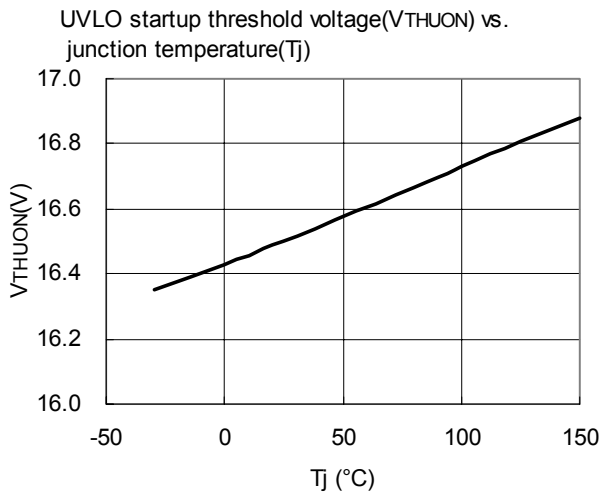
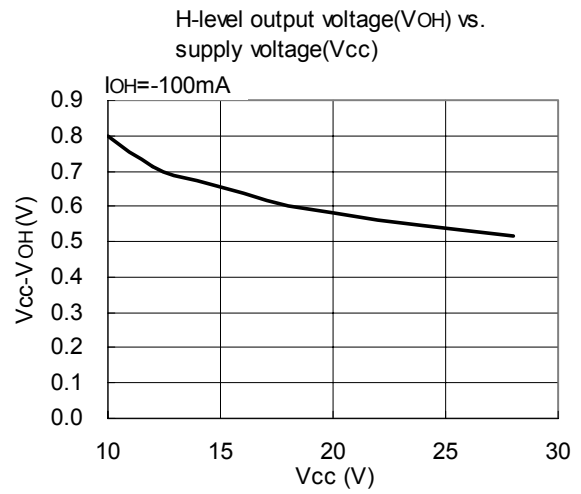
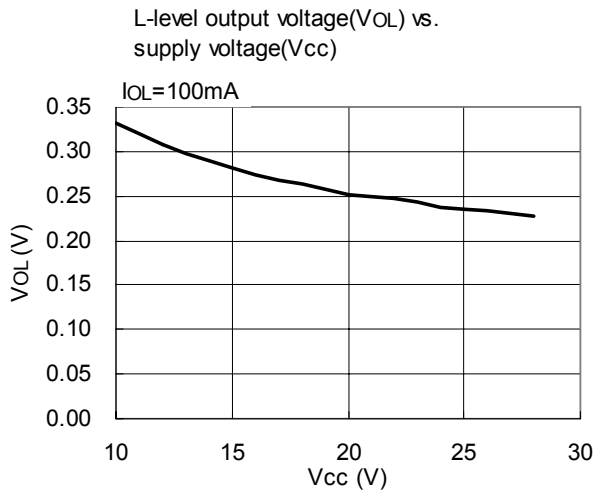
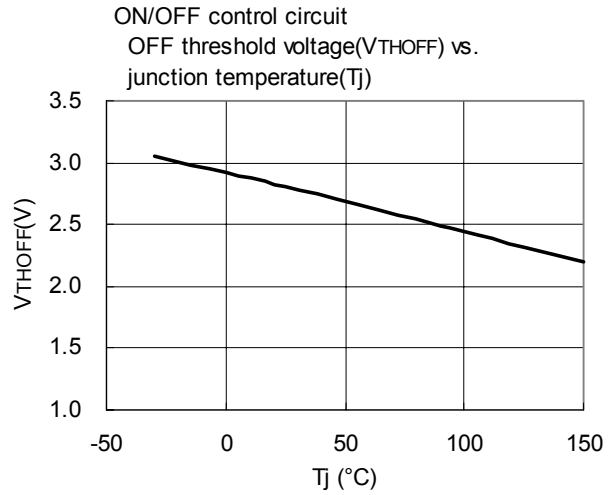
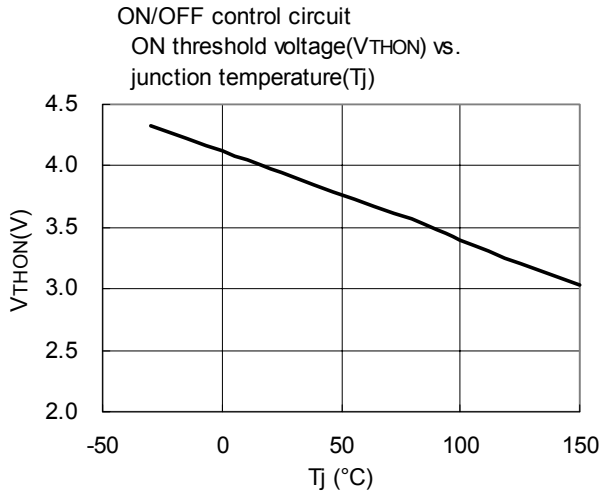
Item	Symbol	Condition	MIN	TYP	MAX	Unit
Stand-by current	ICCST	Vcc=14V			3	μA
Starting-up current	ICCSTA	Vcc=start threshold		10	30	μA
Operating-state supply current	ICCOP	No load		4	6	mA
OFF-state supply current	ICCOFF	ON/OFF pin=0V		80	200	μA

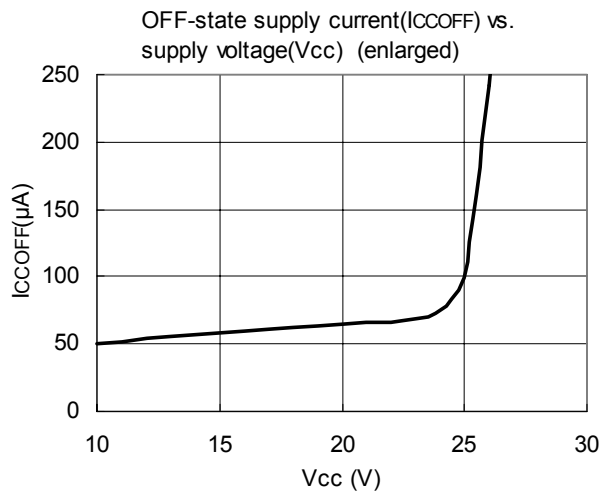
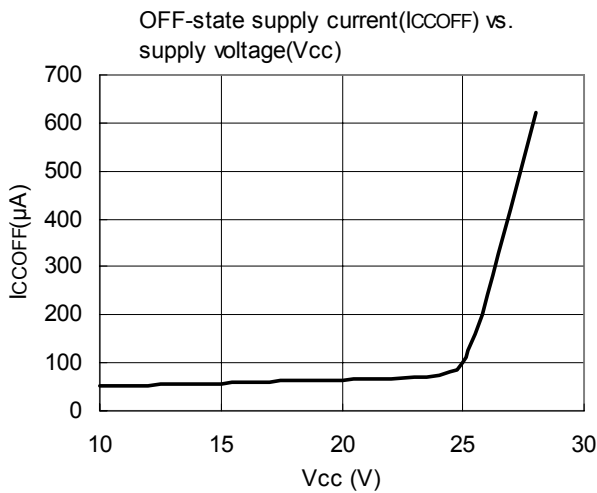
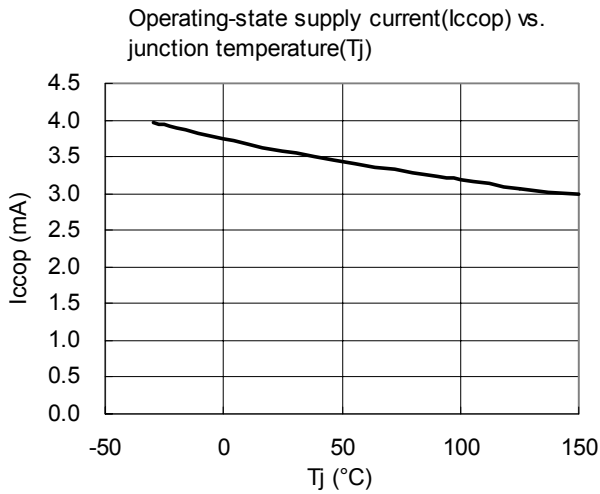
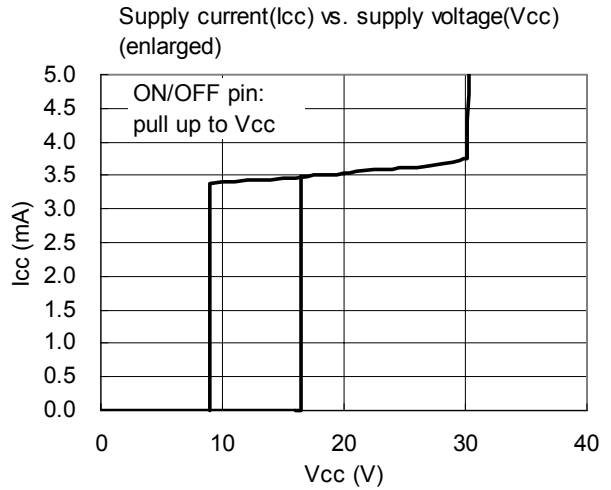
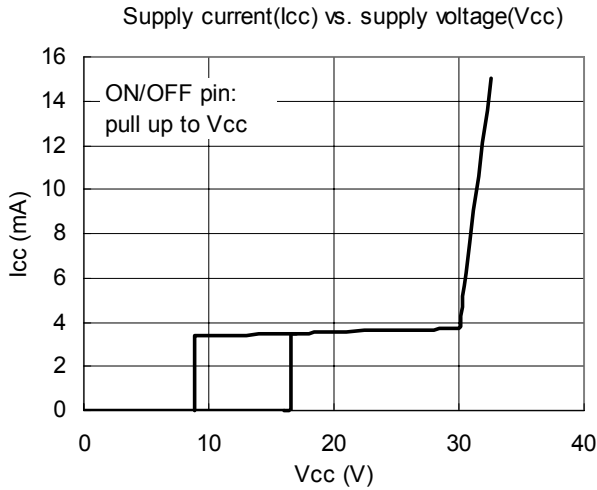
7. Characteristic curves

(Unless otherwise specified, $V_{cc}=V_c=18V$, $T_a=25^\circ C$, $C_T=470pF$, $R_T=22k\Omega$)









8. Description of each circuit

(1) Oscillator section

The oscillator generates sawtooth waveform between 0.3V and 3.4V by charging and discharging capacitor. Fig.1 shows the connection. The oscillation frequency is determined by CT and RT.

(see characteristics curve).

The oscillator waveform is input to the PWM comparator. The oscillator is also used for determining the maximum duty cycle of output pulses. Concretely, a signal is sent to the output circuit section and the OUT pin is forced to be Low level during the CT discharge period (fall time of CT pin voltage).

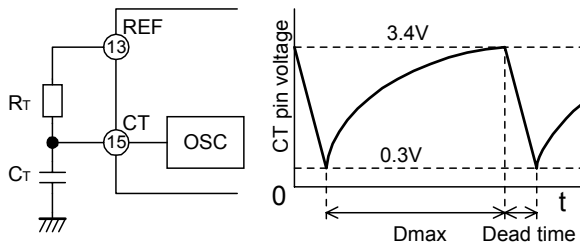


Fig.1 Oscillator circuit

SYNC pin (pin 14) is a synchronizing signal input pin. It is usable for synchronized operation. When it is desired to adopt synchronized operation, the free-running frequency (determined by CT and RT) must be set about 10% lower than that of external synchronizing signal.

The input resistance in SYNC pin is approximately 16kΩ. Usually, a square-wave synchronizing signal is differentiated by R and C, and the voltage input to SYNC pin is so arranged to be below 1V within CT discharge period. Concretely, the waveform must satisfy the condition in Fig.3.

Depending on the amplitude, etc. of square-wave signal used as external synchronizing signal, the RC differentiating circuit shown in Fig.2 could not generate a waveform in Fig.3. In such a case, add a resistor between SYNC pin and GND so as to clear the condition in Fig.3.

Fig.5 shows timing chart of synchronized operation.

Note that diode D2 in Fig.2 is required so that no negative voltage will be applied to SYNC pin while in the discharge period of capacitor Csy in the differentiating circuit. Considering the rated voltage of SYNC pin, use a Schottky diode of a low forward voltage.

Unless the external synchronization function is used, connect SYNC pin to GND pin to avoid a malfunction.

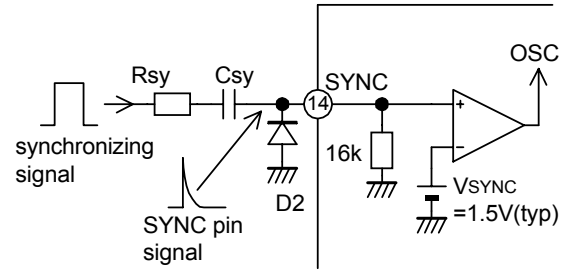


Fig.2 SYNC pin circuit (1)

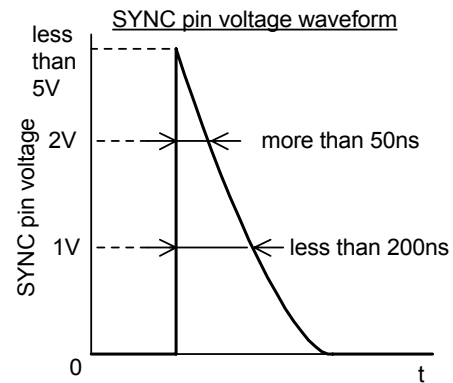


Fig.3 Condition for SYNC pin signal

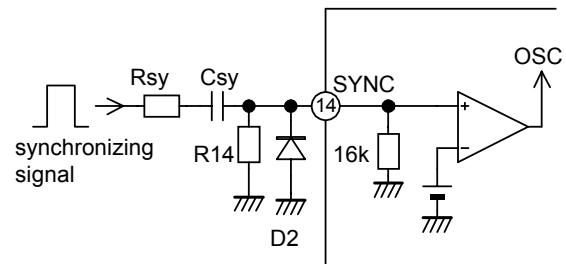


Fig.4 SYNC pin circuit (2)

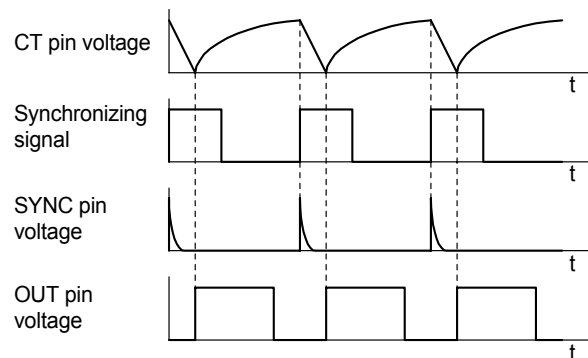


Fig.5 Timing chart of synchronized operation

(2) Voltage error amplifier and overvoltage limiting circuit

ER.AMP is an error amplifier which constitutes a voltage feedback loop for keeping the output voltage constant. The non-inverting input is internally connected to reference voltage Vr of 1.55V (typ.). Fig.6 shows the connection. The output voltage is determined by:

$$V_o = \frac{R1+R2}{R1} \times V_r \dots \dots (1)$$

The error amplifier output is pinned out at VFB pin (pin 5). Between VFB pin and VIN- pin, RC network are connected for loop compensation. The voltage gain Av is expressed by

$$A_v = \frac{R4}{R3(1+j\omega C1 \times R4)} \dots \dots (2)$$

Cutoff frequency fc is expressed by:

$$f_c = \frac{1}{2\pi C1 \times R4} \dots \dots (3)$$

If 100Hz or 120Hz ripples appear at the error amplifier output, the PFC converter will not operate stably. Therefore, determine C1 and R4 so that voltage gain Av at 100 Hz or 120 Hz will be small enough. Also set fc to approximately 1Hz to ensure a stable operation. Practically, the optimum value should be determined by evaluation in the actual circuit.

To limit the output voltage when it has risen above the normal voltage, overvoltage limiting comparator OVP.COMP is incorporated. Its threshold voltage Vp is as follows:

$$V_p = \alpha \times V_r \quad (\alpha=1.058(\text{typ})) \dots \dots (4)$$

According to the connection in Fig.6, therefore, the output overvoltage is limited to 1.058 times (typ.) the normal output voltage.

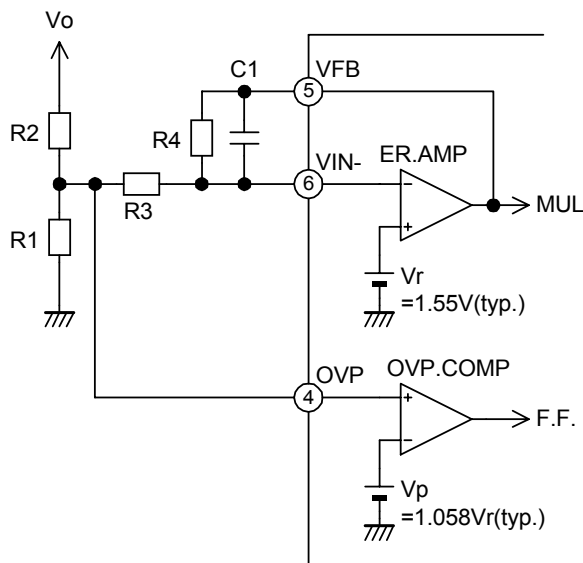


Fig.6 Voltage error amplifier and overvoltage limiting circuit

(3) Current error amplifier and overcurrent limiting circuit

CUR.AMP is an error amplifier which constitutes a current loop to control the line current to a sinusoidal waveform. As shown in Fig.7, to IIN- pin (pin 2), a multiplier output is connected via resistor RA as a current reference signal. Inductor current is monitored by IDET pin (pin 16). The IDET pin should be used within the voltage range from 0V to -1.0V in normal operation. RC network for loop compensation is connected between IFB pin and IIN- pin. According to the circuit in Fig.7, the characteristics of voltage gain AV are as shown in Fig.8. Where,

$$Z = \frac{1}{2\pi R5 \times C3} \dots \dots (5)$$

$$P = \frac{1}{2\pi R5 \times C} \quad C = \frac{C2 \times C3}{C2 + C3} \dots \dots (6)$$

Voltage gain (G1) between Z and P (gain between IDET pin and IFB pin) in Fig.8 is:

$$G1 = 20 \log \left(0.75 \left(\frac{R5}{RA} + 1 \right) \right) \dots \dots (7)$$

Select C2 and C3 so that P/Z will be about 10 for adequate phase margin. The output of current error amplifier is input to PWM comparator.

The optimum value of loop compensation should be determined by evaluation in actual circuit referring to application circuit, etc.

To limit the overcurrent, overcurrent limiting comparator OCP.COMP is provided. The threshold voltage at IDET pin is -1.10V (typ.). If a noise is picked up at IDET pin, suppress it by connecting Rn and Cn. Rn must be lower than 27 Ω.

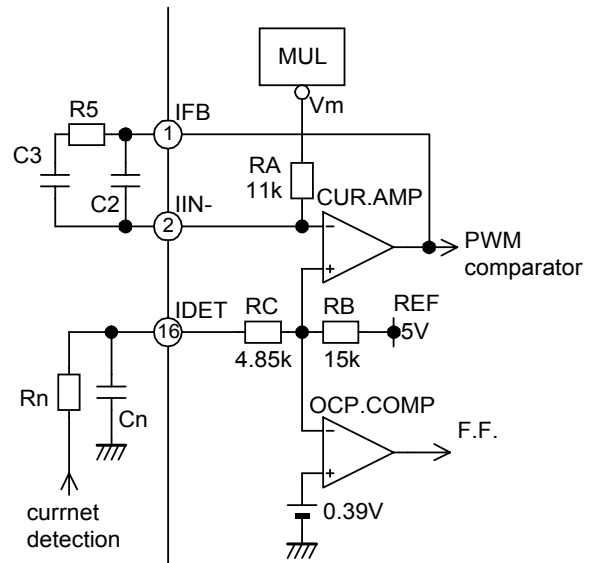


Fig.7 Current error amplifier and overcurrent limiting circuit

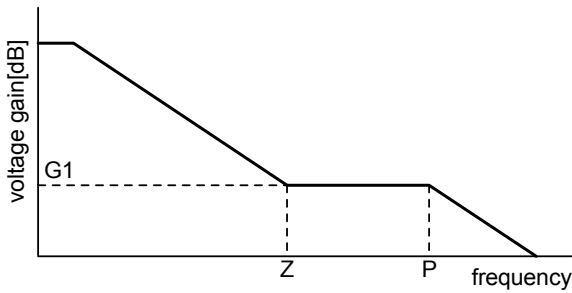


Fig.8 Voltage gain of CUR.AMP

(4) PWM comparator

Fig.9 shows the configuration of PWM comparator. Oscillator output V_{CT} and current error amplifier output V_{IFB} are compared. While $V_{CT} < V_{IFB}$, PWM comparator output goes High and OUT pin also goes High. Note that, during the oscillator discharge period, OUT pin is forced to be Low, thereby determining the maximum duty cycle. (see characteristics curve).

CS pin (pin 11) is a soft start pin. When start up, an internal constant current ($11\mu A$ (typ.)) charges capacitor C4 for soft start. Priority is given to V_{CS} or V_{IFB} whichever is lower. Fig.10 shows PWM comparator timing chart.

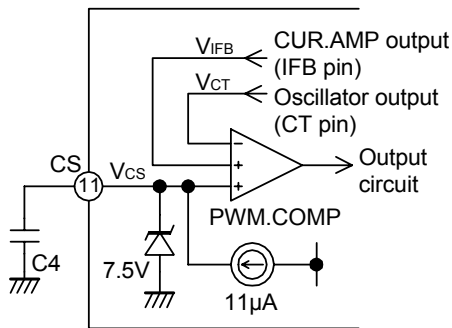


Fig.9 PWM comparator circuit

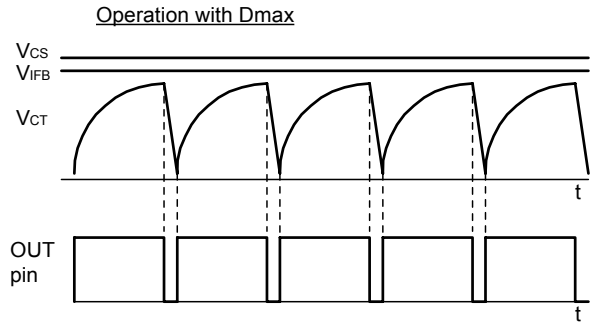
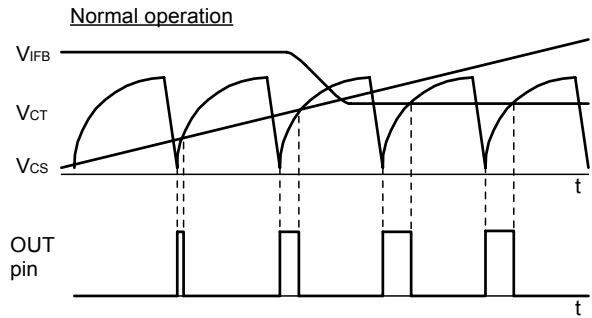


Fig.10 PWM comparator timing chart

(5) Multiplier

The multiplier generates a current reference signal. The rectified line voltage is divided down by resistor and monitored by V_{DET} pin (pin 3). Considering the dynamic range of multiplier, design the R6 and R7 in Fig.11 so that the peak voltage at V_{DET} pin within a range from 0.65V to 2.4V over the entire range of line voltage. V_{FB} pin is normally above 1.55V and, at this status, multiplier output voltage V_m is approximately expressed by:

$$V_m = 1.25 - K \times (V_{VFB} - 1.55) \times V_{VDET} \dots \dots (8)$$

Where

K: Output voltage factor (multiplier section)

When V_{FB} pin is lower than 1.55V, compensation circuit for light load operates.

As shown in Fig.7, V_m is applied via a resistor of $11\text{ k}\Omega$ to inverting input (IIN-) of current error amplifier CUR. AMP. (For input/output characteristics of multiplier, see characteristics curve.)

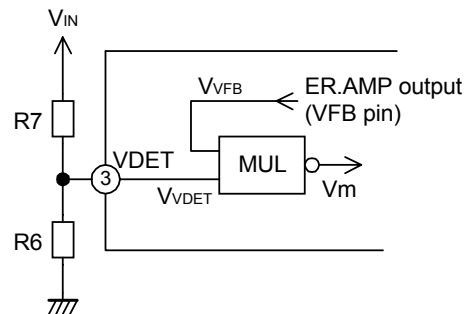


Fig.11 Multiplier circuit

(6) ON/OFF control circuit

Fig.12 shows the configuration of the ON/OFF control circuit. The ON/OFF control circuit consists of a comparator with hysteresis. To turn the IC from OFF mode to operating mode, pull up the ON/OFF pin voltage to 3.95V (typ.) or higher. On the other hand, to turn the IC from operating mode to OFF mode, pull down the ON/OFF pin to 2.80V (typ.) or lower.

In the OFF mode, the reference (REF) voltage is cut off, and the CS pin and OUT pin go approximately 0V. IC consumption current during OFF mode is 200μA (max.) which is much smaller than at an operating mode.

The input current at ON/OFF pin is a very small value of 500nA.

In the case that external signal is applied to ON/OFF pin, the ON/OFF pin voltage must not exceed the VCC pin voltage, even when start up or stop operation.

If ON/OFF operation is not made by external signal, the ON/OFF pin is normally pulled up to Vcc pin through 10kΩ to 1MΩ. Then ON/OFF pin voltage goes to approximately Vcc voltage.

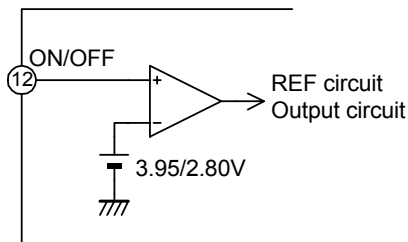


Fig.12 ON/OFF control circuit

(7) Output circuit

As shown in Fig.13, VC pin (pin 9) is configured as the high power terminal, independent of the IC power terminal (VCC pin). This pin allows an independent drive resistance when the power MOSFET is ON and OFF. Suppose the drive resistance when ON and OFF are Rg (on) and Rg (off),

$$R_{g(\text{on})} = R_{g1} + R_{g2} \quad \dots \dots (9)$$

$$R_{g(\text{off})} = R_{g2} \quad \dots \dots (10)$$

At standby, the OUT pin is kept Low.

If the drain voltage of power MOSFET oscillates, a parasitic capacitance between gate and drain may swing the OUT pin (pin 8) of IC below 0V. If OUT pin voltage falls below -0.3V, a current may flow to the parasitic element in IC, whereby the IC may malfunction. In such a case, Schottky diode must be connected between OUT pin and GND so as not to allow a parasitic current to flow to IC.

If VC pin is fed with a source which is independent of VCC pin, the voltage of VC pin must not exceed that of VCC pin even start up or stop operation.

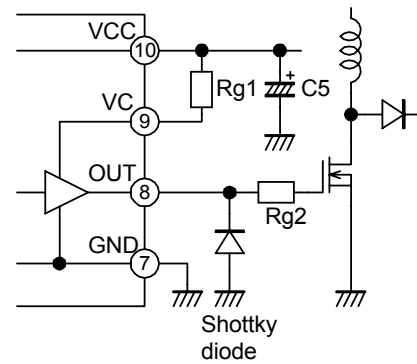


Fig.13 Output circuit

(8) Undervoltage lockout circuit

This IC contains an undervoltage lockout circuit to prevent malfunction when the Vcc voltage drops. When the Vcc voltage rises from 0V, this IC starts operation at 16.5V (typ.). If the Vcc voltage drops after the IC starts up, this IC stops operation at 8.9V (typ.). When IC stops operation by undervoltage lockout circuit, OUT pin and CS pin is kept low

(9) Compensation circuit for light load

If the output of multiplier and the input of current error amplifier do not have offset voltage, the input current to the converter is approximately zero under condition that the PFC converter operates in no load. But an actual multiplier and current error amplifier may have offset voltage. If the offset voltage is negative, the input current, which corresponds to the offset voltage, flows into the converter even when the PFC converter operates in no load. In this case, the PFC output voltage rises abnormally because of too much input current.

To avoid these, this IC has an automatic offset correction circuit for light load. The output voltage of error amplifier is approximately 1.55V or higher in normal operation.

If the output voltage drops below 1.55V, this circuit operates. If there is a negative offset voltage, the output voltage of error amplifier falls below 1.55V in the case that the PFC converter operates in no load or light load. Then, the offset voltage is corrected in the multiplier circuit. Because of this operation, even under no load or light load, the PFC output voltage does not rise abnormally, but is always kept stable. The amount of correction changes linearly according to the output of error amplifier, which can make operation stable.

Fig.14 shows the outline of the effect of this circuit.

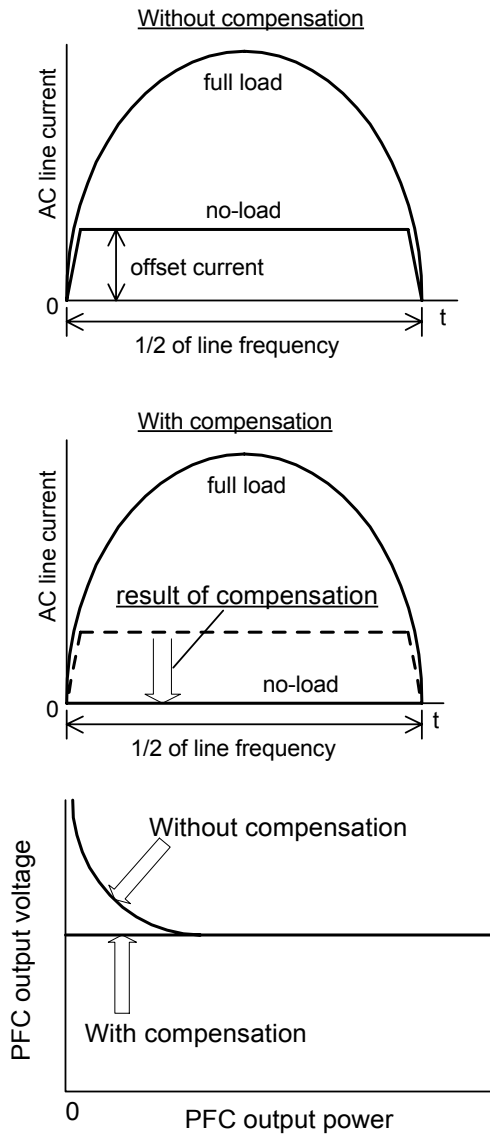


Fig.14 Operation outline of compensation circuit for light load

9. Design advice

(1) Vcc circuit

Vcc voltage can be supplied from an auxiliary winding of the inductor. An example circuit is shown in Fig.15.

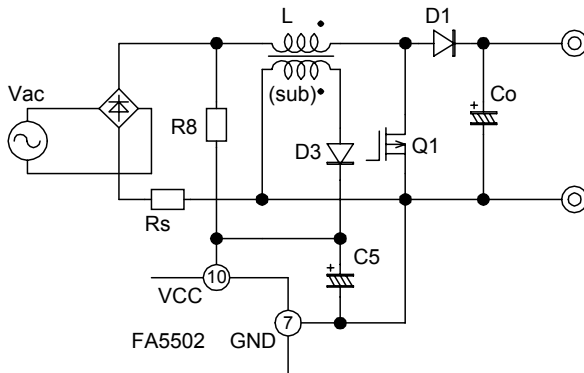


Fig.15 Vcc circuit (1)

In this circuit, R8 is a start up resistor. The start up resistor R8 should be satisfied the following formula in order to supply with at least 30 μ A of IC start up current.

$$R8 < \frac{\sqrt{2} \times \text{Vac}(\text{min}) - 17.5}{30 \times 10^{-6}} \dots \dots (11)$$

Note that this formula is a minimum condition for starting the IC. Practically, determine the value upon taking into account the start up time required for converter. The start up time must be determined upon measurement at actual circuit operation.

In steady state, Vcc is supplied from the auxiliary winding (sub) of inductor. When the IC is just starting up, however, it takes time for the voltage from auxiliary winding to rise enough. The value of capacitor C5 connected to Vcc pin should be determined to prevent Vcc from falling below the OFF threshold voltage of UVLO during this period. The capacity of C5 should be determined by evaluation in the actual circuit because the time lag is different in each circuit.

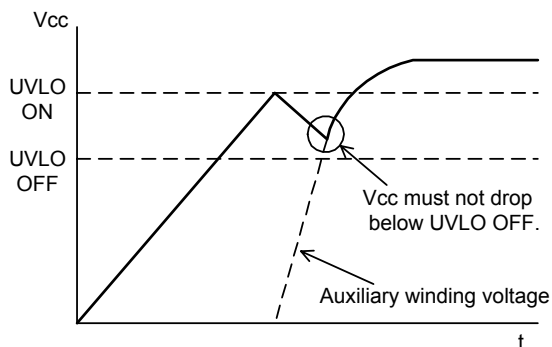


Fig.16 Vcc voltage at start up

Even after PFC starts up, Vcc may fall due to step changes of the load or inputs. To prevent the IC from stopping in those cases, the circuit shown in Fig.17 is effective to prolong the hold time of the Vcc voltage. After the PFC converter starts up, Vcc is supplied through C6. Therefore, you can prolong the hold time of Vcc by using a large capacity for C6.

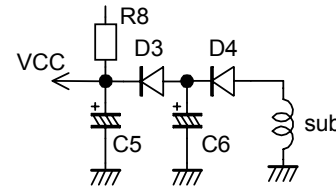


Fig.17 Vcc circuit (2)

In some case, the Vcc voltage cannot be supplied enough in light load condition. In this case, the circuit shown in Fig.18 may be effective to improve the Vcc. The appropriate value of C7 and R9 should be determined by evaluation in actual circuit because they depend on each circuit.

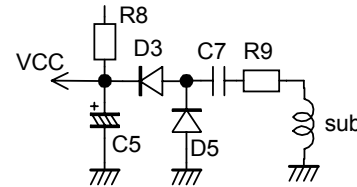


Fig.18 Vcc circuit (3)

(2) Supplying Vcc from external power supply

If Vcc is not supplied from the auxiliary winding of inductor but from an external power supply, pay attention to the followings.

- In order to start up the IC, Vcc must be above the ON threshold voltage VTHUON (17.5V (max.)) of undervoltage lockout circuit (UVLO). When starting up, apply at least this VTHUON. After starting up, the operation is available within the recommended range of 10 to 28V.
- If a noise is applied to Vcc pin, it may cause malfunction. To avoid a noise, connect a capacitor near VCC pin even when Vcc is supplied from an external power supply. To prevent a malfunction, suppress the noise below about ± 0.6 V. And, make sure there is no malfunction attributable to noise.

(3) Designing a boost converter

Fig.19 shows a basic circuit of boost converter used as an PFC converter. The following describes how to determine each values of the circuit.

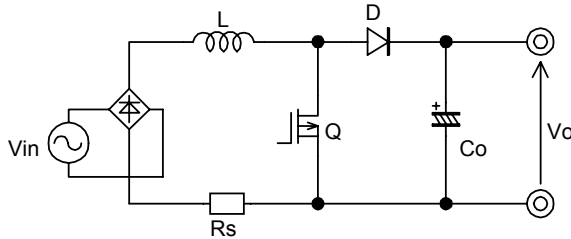


Fig.19 Boost converter circuit

(3-1) Output voltage

Set the output voltage of boost converter at least 10V higher than the peak value of maximum input voltage to ensure a stable operation. When it is used as PFC converter, the input voltage has a sinusoidal waveform. Therefore, set the output voltage Vo by:

$$V_o \geq \sqrt{2} \times V_{in(max)} + 10 [V] \quad \dots (12)$$

$V_{in(max)}$: Maximum AC input voltage [Vrms]

(3-2) Inductor

When PFC converter operates in the continuous current mode, select an approximate inductance considering the ratio of inductor ripple current to the peak input current by:

$$L \geq \frac{V_{in}^2 (V_o - \sqrt{2} \times V_{in})}{\gamma \times f_s \times P_{in} \times V_o} \quad \dots (13)$$

Where,

- V_{in} : AC input voltage [Vrms]
- γ : Ratio of ripple content to peak input current. (Set to approx. 0.2, see Fig.20)
- f_s : Switching frequency [Hz]
- P_{in} : Maximum input power [W]

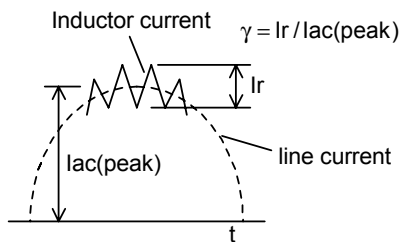


Fig.20 Outline of inductor and AC line current

(3-3) Current detecting resistance Rs

R_s is a resistor which allows to detect an inductor current to control the line current into sinusoidal. Because the threshold voltage for overcurrent limiting circuit is -1.1V (typ.), peak inductor current limit I_p is calculated by:

$$I_p = \frac{1.1}{R_s} [A] \quad \dots (14)$$

So that the voltage inputted to IDET pin will not be beyond -1V, whereby the overcurrent limiting circuit will not operate at a normal operation, calculate R_s by:

$$R_s \leq \frac{V_{in(min)}}{\sqrt{2} \times P_{in(max)}} [\Omega] \quad \dots (15)$$

Where,

- $V_{in (min)}$: Minimum AC input voltage [Vrms]
- $P_{in (max)}$: Maximum input position [W]

As a matter of fact, the peak current changes with switching ripple current contained in the inductor current, circuit efficiency, etc. Definitely determine it by evaluation on a actual circuit.

(3-4) Smoothing capacitor

PFC converter output contains ripple voltage of twice the line frequency as shown in Fig.21.

Instantaneous value $V_o(t)$ of output voltage is approximated by:

$$V_o(t) = V_o - \frac{I_o}{2\omega_0 \times C_o} \times \sin(2\omega_0 \times t) \quad \dots (16)$$

Where,

- I_o : Output current [A]
- $\omega_0 = 2\pi f_0$ (f_0 : AC line frequency [Hz])
- C_o : Output smoothing capacitance [F]

Therefore, output ripple voltage V_{rp} (p-p) is:

$$V_{rp} = \frac{I_o}{\omega_0 \times C_o} \quad \dots (17)$$

Using formula (17), determine the necessary value. The overvoltage limiting circuit of FA5502 monitors the instantaneous output voltage. Therefore, determine the capacitance of smoothing capacitor C_o so that the instantaneous output voltage including the ripple at a normal operation will not reach the overvoltage limit.

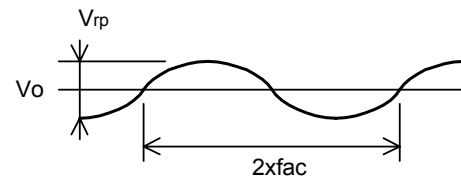


Fig.21 Output ripple voltage

(4) Output overvoltage at light load

A compensation circuit for light load is incorporated for preventing an overvoltage when light or no load. Though, according to the condition, this circuit may not compensate enough and overvoltage may occur. To prevent overvoltage, the following condition must be satisfied.

- Noise filter resistor Rn connected to IDET pin (pin 16) must be below 27Ω.
- As shown in Fig.22, DC gain limiting resistor R10 for current error amplifier must not be connected between IFB pin (pin 1) and IIN- pin (pin 2).

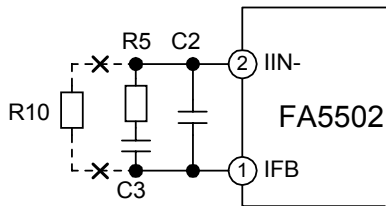


Fig.22 Prevention of overvoltage at light load

(5) Notes for setting the output voltage and overvoltage limit

In the actual circuit, the output voltage drops depending on the line voltage or load current. Therefore, the output voltage may be lower than the voltage calculated by expression (1) in "8-(2)". When setting the output voltage, sufficiently evaluate it on an actual circuit.

On the circuit shown in Fig.6 in "8-(2)", the overvoltage setting is fixed at 1.058 times the output voltage setting.

For setting the overvoltage independently of the output voltage setting, connect voltage divider additionally to OVP pin as shown in Fig.23.

On the circuit in Fig.23, even if the voltage divider for setting the output voltage has troubled, the overvoltage limiting circuit operates properly, thereby preventing the output voltage from rising excessively.

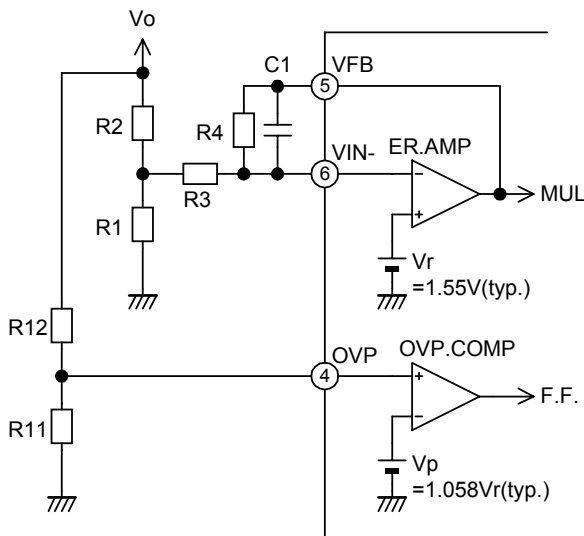


Fig.23 Independent setting of OVP limit

(6) Improvement of output voltage regulation

As stated in "9-(5)", the output voltage may change with input voltage or load current on the circuit in Fig.6 in "8-(2)", thereby causing a problem in some case. In such a case, the circuit in Fig.24 may improve the regulation.

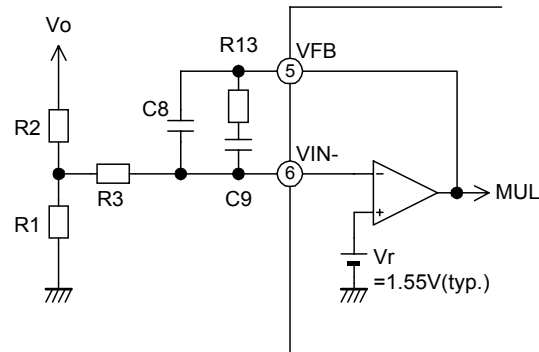


Fig.24 ER.AMP circuit for improvement of regulation

Voltage gain Av2 of this circuit is expressed by:

$$A_{v2} = \frac{1 + j\omega C9 \times R13}{j\omega((C8 + C9) + j\omega C8 \times C9 \times R13)R3} \dots (18)$$

Optimum values depend on an each circuit. Referring the following relations or the example applied to "10 Example of application circuit", adjust the values on actual circuit.

- Set the voltage gain Av2 at 100 or 120 Hz almost the same as before changing the compensation circuit.

- Determine C8, C9 and R13 so as to satisfy the following relations.

- Set fz determined by the following expression to several Hz to several ten Hz.

$$f_z = \frac{1}{2\pi C9 \times R13} \dots (19)$$

- Set fp determined by the following expression so that the fp/fz ratio is about 10.

$$f_p = \frac{1}{2\pi C \times R13} \quad C = \frac{C8 \times C9}{C8 + C9} \dots (20)$$

*Example of values applied to "10 Example of application circuit"

C8=0.033μF, C9=0.15μF, R13=330kΩ, R3=100kΩ

(These values are given as references and not intended for guaranteeing the operation in any circuit.)

In this circuit, not only the output voltage characteristics at a steady status but also transient response to line voltage and load current may change. Before determining the circuit values, evaluate sufficiently.

(7) Prevention of intermittent switching of low frequency

An intermittent switching below 10 Hz may occur in some application. It may be avoided by the following methods. They are given as typical preventions of intermittent switching and may not be effective for certain circuits. They may also affect the characteristics of PFC converter. Sufficiently check the operation on a actual circuit.

(7-1) Lowering the dc gain of voltage error amplifier

Lower the dc gain of the voltage error amplifier. Concretely, reduce the resistance of R4 on the circuit in Fig.6 in "8-(2)". Note that, in this case, the line and load regulation will be lowerd.

(7-2) Connection of Rofst

Adjust the offset of the current error amplifier. Concretely, connect a resistor Rofst of 1M Ω or higher between REF pin and IIN- pin as shown in Fig.25. Note that, in this case, the input current will be distorted and the power factor will be slightly lowered.

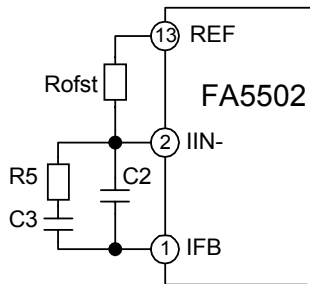


Fig.25 Connection of Rofst

(7-3) Change of compensation network of voltage error amplifier

Replace the compensation network connected to the voltage error amplifier with the circuit in Fig.24 in "9-(6)". Note that, in this case, the transient response may be different from that before the change.

(8) Improvement of operation around zero crossing

In some application, surge current may appear on the line current around zero crossing. This surge current may cause harmonic current especially in high order. In such a case, the following method may suppress this surge current.

(8-1) Connection of Rofst

As shown in Fig.25, connect resistor Rofst between REF pin and IIN- pin. Use a resistor of about 1M Ω or higher.

(8-2) Increase of Dmax

Increase the maximum duty cycle. Concretely, select such a network of R_T and C_T for the same frequency that C_T is a smaller and R_T a larger.

(See (9) Oscillator setting and maximum duty cycle.)

(9) Oscillator setting and maximum duty cycle

The maximum duty cycle is determined by forcing the OUT pin to be Low during the oscillator discharge period. The oscillator discharge period changes with R_T and C_T connected to CT pin. On a network of C_T and R_T providing the same oscillation frequency, the discharge period shortens and the maximum duty cycle increases by minimizing C_T and maximizing R_T. (See characteristics curve.) The maximum duty cycle may affect the input current waveform, particularly at zero crossing. Therefore, sufficiently test C_T and R_T before determining them. Too small C_T could not give a stable oscillation on account of noise, etc. It should be 330pF or more according to the recommended condition.

(10) Npte in use of SYNC pin

If the external synchronizing signal is not a square waveform or if has a trapezoid shape, a differentiating circuit of RC network may not satisfy the waveform condition shown in Fig.3 in "8-(1)". In such a case, convert the external synchronizing signal into a square waveform by means of comparator or the like before inputting it to a differentiating circuit of RC network. (See "8-(1) Oscillator section".)

(11) Prevention of malfunction by noise

Noise applied to each pin may cause malfunction of IC. If noise causes malfunction, see the notes summarized below and confirm in actual circuit to prevent malfunction.

Capacitor for noise suppressing should be connected as close to IC as possible so as to suppress noise effectively.

(11-1) REF pin

REF pin voltage is supplied to each components of IC as voltage source and reference voltage. A noise applied to this pin may cause a malfunction of IC. To suppress a malfunction by noise, connect a capacitor of 0.1 μ F or more between REF pin and GND.

(11-2) IDET pin

If a noise is applied to IDET pin which detects induvtor current, the overcurrent limiting circuit may suffer from a malfunction. In such a case, insert an RC filter at IDET pin.

(11-3) OVP pin

If a noise applied to OVP pin causes a malfunction, connect a noise suppressing capacitor between OVP and GND pins.

(11-4) CT pin

A noise applied to CT pin, which is an oscillator output, may disturb the oscillation frequency or OUT pulses. The wiring between oscillator timing capacitor C_T and IC must be as short as possible so as to suppress the noise to CT pin. Pay utmost attention to

GND wiring so as not to generate a common impedance with other wires.

(11-5) VCC pin

A noise applied to VCC pin may cause a malfunction. To suppress this noise, connect a capacitor near VCC pin even if IC is energized by another power supply. Determine the capacitance so that the noise generated at VCC pin will be within about $\pm 0.6V$. Then, make sure no malfunction occurs by noise.

(12) Voltage rating of IDET pin

The voltage rating of IDET pin, which monitors an inductor current, is -10V. In case of a general boost circuit, a inrush current for charging the output smoothing capacitor C_o flows at the instant when an AC input voltage is connected. This current may be by far greater than the input current at a normal operation. As a result, a voltage much higher than normal may be applied to IDET pin. Pay attention so that a voltage beyond the maximum voltage rating of -10V will not be applied to IDET pin even at an instant when an AC input voltage has been connected. If there are cases where a voltage higher than rating is applied to IDET pin, insert a limiting circuit for inrush current, or add a Zener diode as shown in Fig.26 or 27 to suppress the voltage applied to IDET pin.

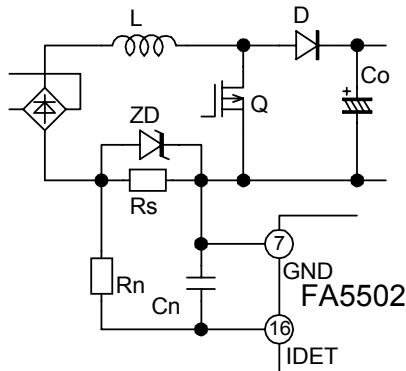


Fig.26 IDET pin protection (1)

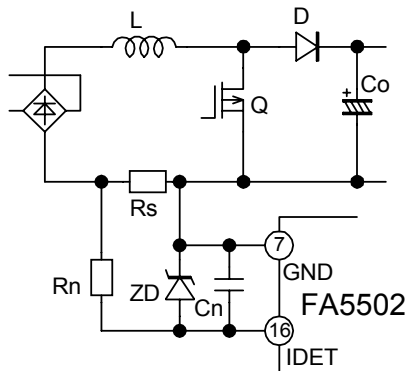
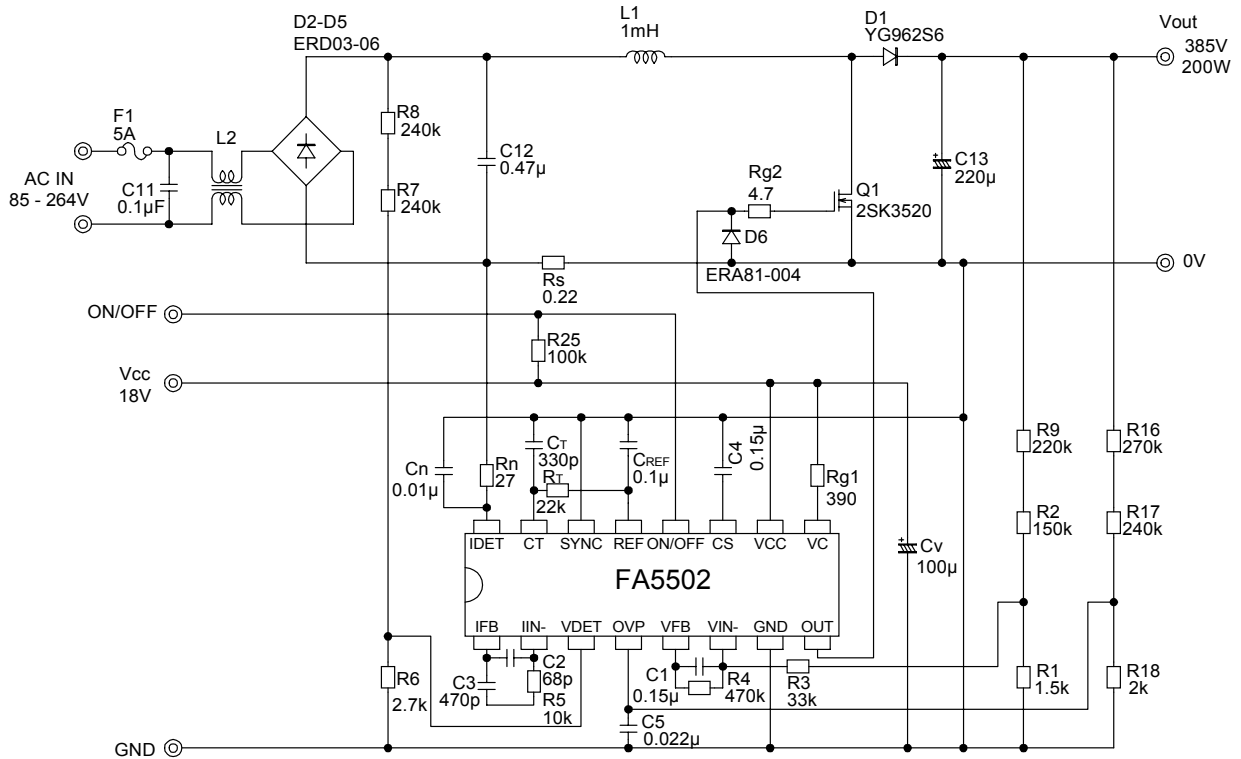


Fig.27 IDET pin protection (2)

(13) Prevention of malfunction by negative voltage of each pin

IDET pin is so designed as to input a negative voltage. In the case of other pins, however, if large negative voltage is applied, parasitic elements in IC may operate and it may cause a malfunction. Pay attention so that the voltage applied to pins other than IDET pin will not be lower than -0.3V.

10. Example of application circuit

**Note**

This application circuit exemplifies the use of IC for your reference only. Parts tolerance, parts characteristics, influence of noise, etc. are not defined in this application circuit. When design an actual circuit for a product, you must determine parts tolerance, parts characteristics, influence of noise, etc. for safe and economical operation. Neither Fuji nor its agents shall be liable for any injury caused by any use of this circuit.