FUDAN MICROELECTRONICS

复旦微电子

FM2827 Power Factor Correction Controller

Specification

May. 2008

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1. Product Overview

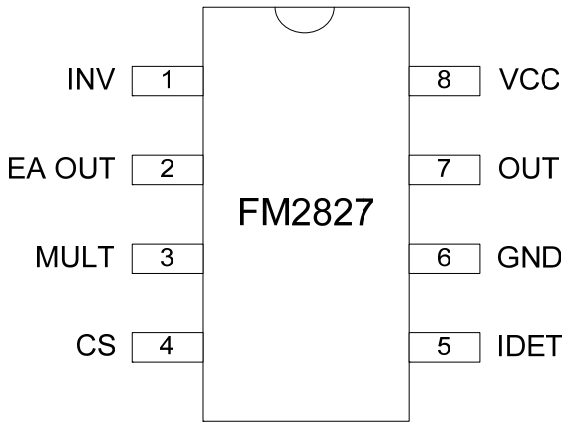
1.1. Description

The FM2827 is the high performance power factor correction controller designed by ShangHai FuDan Microelectronics Co., Ltd. The FM2827 is applied to electronic ballast with low power, high density which requires minimum board area. The FM2827 can also be minimized devices and power dissipation.

1.2. Features

- **Internal Startup Timer**
- **Internal R/C filter eliminates the Need for an External R/C filter**
- **Very Precise Adjustable Output Over Voltage Protection**
- **Zero Current Detector**
- **Trimmed Internal Bandgap Reference**
- **Under Voltage Lock Out with 3V of Hysteresis**
- **Low Startup and Operating Current**
- **8-Pin DIP or 8-Pin SOP**

1.3. Pin Configuration



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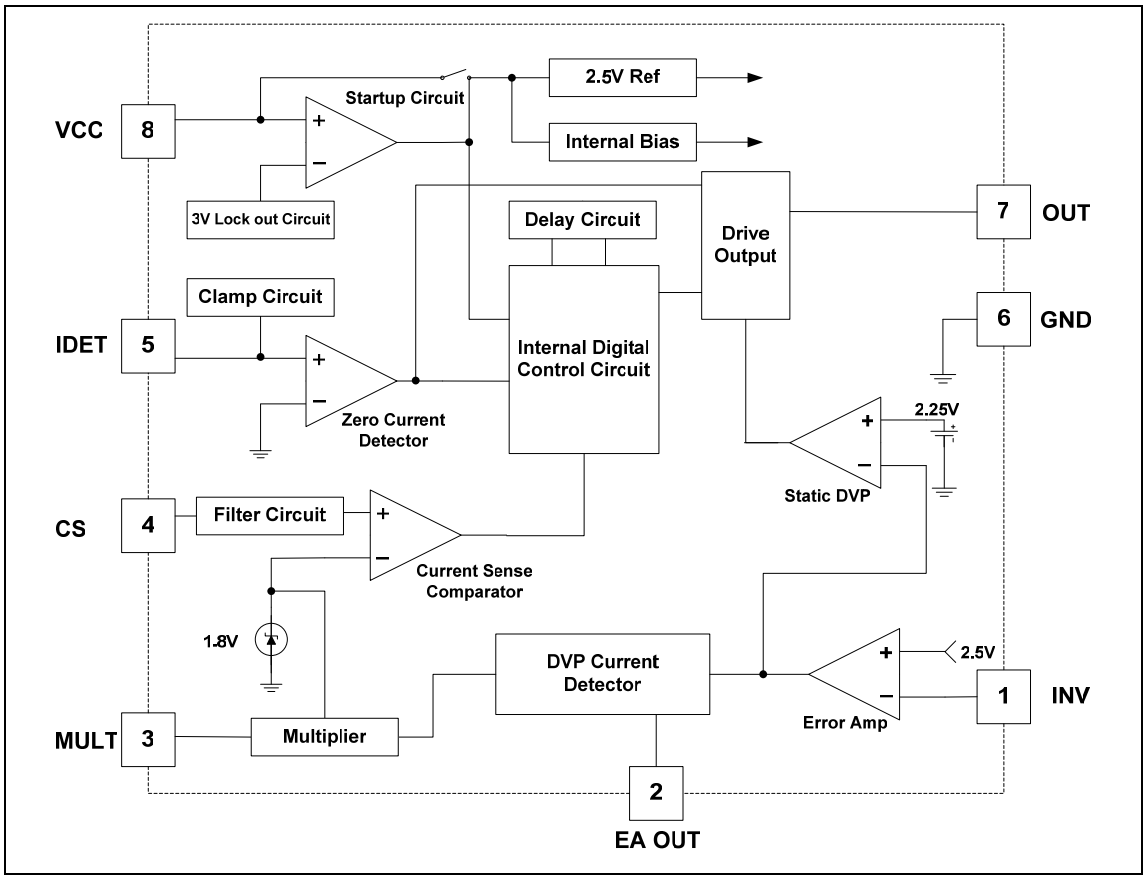
1.4. Pin Description

PIN	Symbol	Description
1	INV	Inverting input of the error amplifier. The output of the boost converter should be resistively divided to 2.5V and connected to this pin.
2	EAOUT	The output of the error amplifier. A feedback compensation network is placed between this pin and the INV pin.
3	MULT	Input to the multiplier stage. The full-wave rectified AC is divided to less than 3.8V and is connected to this pin.
4	CS	Input to the PWM comparator. Current is sensed in the boost stage MOSFET by a resistor in the source lead. An internal RC low pass filter has been included to reject any high frequency noise present on the current waveform.
5	DET	The zero current detector senses the inductor current by monitoring when the boost inductor auxiliary winding voltage falls below 1.8V.
6	GND	The ground potential of all the pins.
7	OUT	Gate driver output. A push pull output stage is able to drive the Power MOSFET.
8	VCC	Supply voltage of driver and control circuits.

1.5. Block Diagram



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2. State Description

2.1. Multiplier

The rectified AC line voltage is connected to an external resistor divider, and gets a rectified voltage range from 0 to 3.8V. The signal is sent to MULT pin. The other input is internally driven by a DC voltage which is the difference between error amplifier output (Pin 2) and reference voltage, Vref.

The multiplier is designed to have an extremely linear transfer curve over a wide dynamic range, 0V to 3.8V for Pin 3, and 2.25V to 7.3V for error amplifier output under all line and load conditions.

The multiplier output controls the current sense comparator threshold voltage as the ac voltage traverses sinusoidally from zero to peak line. This allows the inductor peak current to follow the ac line thus forcing the average input current to be sinusoidal. In other words, this has the effect of forcing the MOSFET on-time to track the input line voltage, resulting in a fixed drive output on-time, thus making the pre-converter load appear to be resistive to the ac line.

2.2. Current Sense Comparator

The current sense comparator adopts the RS latch configuration to ensure that only a single pulse appears at the drive output during a given cycle. MOSFET drain current is sensed using an external sense resistor in series with the external MOSFET. When the sensed voltage exceeds the threshold set by the multiplier output, the current sense comparator turns off the MOSFET and resets the PWM latch. The latch insures that the output remains in a low state after the MOSFET drain current falls back to zero. The peak inductor current under the normal operating condition is controlled by the multiplier output, Vmo. The abnormal operating condition occurs during pre-converter start-up at extremely high line or as output voltage sensing is lost. Under these conditions, the multiplier output and current sense threshold will be internally clamped to 1.8V. Therefore, the maximum peak switch current is limited to:

$$Ipk\ (max) = 1.8V / Rsense$$

An internal R/C filter has been included to attenuate any high frequency noise that may be present on the current waveform. This circuit block eliminates the need for an external R/C filter otherwise required for proper operation of the circuit.

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2.3. Zero Current Detector

The circuit operates as a critical conduction current mode controller. The zero current detector switches on the external MOSFET as the voltage across the boost inductor reverses, just after the current through the boost inductor has gone to zero. The slope of the inductor current is indirectly detected by monitoring the voltage across an auxiliary winding and connecting it to the zero current detector Pin 5. Once the inductor current reaches ground level, the polarity of the voltage across the winding is reversed. When the Idet input falls below 1.5V, the comparator output is triggered to the low state. To prevent false tripping, 0.5V hysteresis is provided. The zero current detector input is protected internally by two clamps. The upper 7.5V clamp prevents input over voltage breakdown while the lower 0.75V clamp prevents substrate injection. An internal current limit resistor protects the lower clamp transistor in case the Idet pin is shorted to ground accidentally. A watchdog timer function is added to the IC to eliminate the need for an external oscillator when used in stand-alone applications. The timer provides a means to start or restart the pre-converter automatically if the drive output has been off for more than 500us after the inductor current reached zero.

2.4. Voltage Protection Block

The chip monitors the current flowing into the EA_OUT pin. If the monitored current reaches about 30μA, the output of multiplier is forced to be decreased, thus reducing the input current drawn from the mains (soft OVP). If the monitored current exceeds 40μA, the OVP protection is triggered (dynamic OVP), and then the external power transistor is switched off until the current falls below about 10μA. In this case, it disables some internal blocks reducing the quiescent current of the chip to 2mA. However, if the over voltage lasts so long that the output of E/A goes below 2.25V, then the protection is activated (static OVP) keeping the output stage and the external power switch turned off. The operation of the device is re-enabled as the E/A output goes back into its linear region.

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3. Characteristics

3.1. Absolute Maximum Ratings

(Ta = 25°C)

Symbol	Characteristics	Value	Unit
VCC	Supply Voltage	15.5	V
IOH, IOL	Peak Drive Output Current	500	mA
Vin	Error Amp, Multiplier And Comparator Input Voltages	-0.3 ~ 6	V
Tj	Operating Junction Temperature	150	°C
Topr	Operating Temperature Range	-25 ~ +125	°C
Tstg	Storage Temperature Range	-65 ~ +150	°C
Pd	Power Dissipation	0.8	W

3.2. Electrical Characteristics

Symbol	Characteristic	Test condition	Min.	Typ.	Max.	Unit
UNDERVOLTAGE LOCK OUT SECTION						
Vth (st)	Start Threshold Voltage	VCC Increasing	10.5	11.5	12.5	V
Vimax	Input Clamp voltage		15.1	15.3	15.5	V
HY (st)	UVLO Hysteresis	-	2	3.2	4	V
SUPPLY CURRENT SECTION						
Ist	Start-up Supply current	VCC＝th (st) － 0.2V	20	80	100	μA
Icc	Operating Supply Current	Output not switching		2.8	6	mA
Icc (ovp)	Operating Current at OVP	Vinv = 3V	-	1.42	4	mA
Idcc	Dynamic Operating Supply Current	50kHz, C1 = 1nF	-	4	8	mA
ERROR AMPLIFIER SECTION						
Vref	Voltage Feedback Input Threshold	Iref = 0mA, Ta = 25°C	2.465	2.5	2.535	V
		0 ≤ Ta ≤ 125°C	2.44	2.5	2.56	V
△Vref1	Line Regulation		-	0.04	10	mV
Ib (ea)	Input Bias Current	-	-0.5	-	0.5	μA
Isource	Output Source Current	Vm2 = 4V	-4	-4	-	mA
Isink	Output Sink Current	Vm2 = 4V	4	8	-	mA
Veao (H)	Output Upper Clamp Voltage*	Isource = 0.1mA	-	7.3	-	V
Veao (L)	Output Lower Clamp Voltage	Isink = 0.1mA	-	2.2	-	V
Gv	Large Signal Open Loop Voltage*	-	60	83	-	dB

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Symbol	Characteristic	Test condition	Min.	Typ.	Max.	Unit
MULTIPLIER SECTION						
Ib (m)	Input Bias Current (pin3)	-	-0.5	-0.2	0.5	μA
△Vm1	M1 Input Voltage range (pin3)	-	0	-	3.8	V
△Vm2	M2 Input Voltage range (pin2)	-	Vref	-	Vref+ 2.5	V
K	Multiplier Gain*	Vm1 = 1V, Vm2 = 3.5	0.36	0.43	0.52	1 / V
Vomax (m)	Maximum Multiplier Output Voltage	Vea (-) = 0V, Vm1 = 2V	1.55	1.75	1.85	V
CURRENT SENSE SECTION						
Vio (cs)	Input Offset Voltage*	Vm1 = 0V, Vm2 = 2.2V	-10	3	10	mV
Ib (cs)	Input Bias Current	0 ≤ Vcc≤1.7V	-1	-0.07	1	μA
Td (cs)	Current Sense Delay To Output	-	-	400	-	ns
DETECT SECTION						
Vth (det)	Input Voltage Threshold	Vdet Increasing	1.7	2.24	2.4	V
HY (det)	Detect Hysteresis	-	0.2	0.55	0.8	V
Vclamp (l)	Input Low Clamp Voltage	Idet = -100μA	0.45	0.73	1	V
Vclamp (h)	Input High Clamp Voltage	Idet = 3mA	6.5	7.5	7.9	V
Ib (det)	Input Bias Current	1 ≤ Vdet ≤ 5V	-1	-0.1	1	μA
Iclamp	Input High / Low Clamp Diode Current	-	-	-	±3	mA
OUTPUT SECTION						
Voh	Output Voltage High	Io = -10mA	10.5	11	-	V
Vol	Output Voltage Low	Io = 10mA	-	0.7	1	V
Vomin (o)	Output Voltage With UVLO Acitivated	Vcc = 5V, Io = 100μA	-	0.2	1	V
RESTART TIMER SECTION						
Td(rst)	Restart Time Delay	Vm1 = 1V, Vm2 = 3.5V	-	500	-	μS
OVER VOLTAGE PROTECTION SECTION						
Isovp	Soft OVP Detecting Current		25	27.7	35	μA
Isovp	Dynamic OVP Detection Current		35	38.8	45	μA
Vovp	Static OVP Threshold Voltage	Vinv = 2.7V	2.1	2.25	2.4	V

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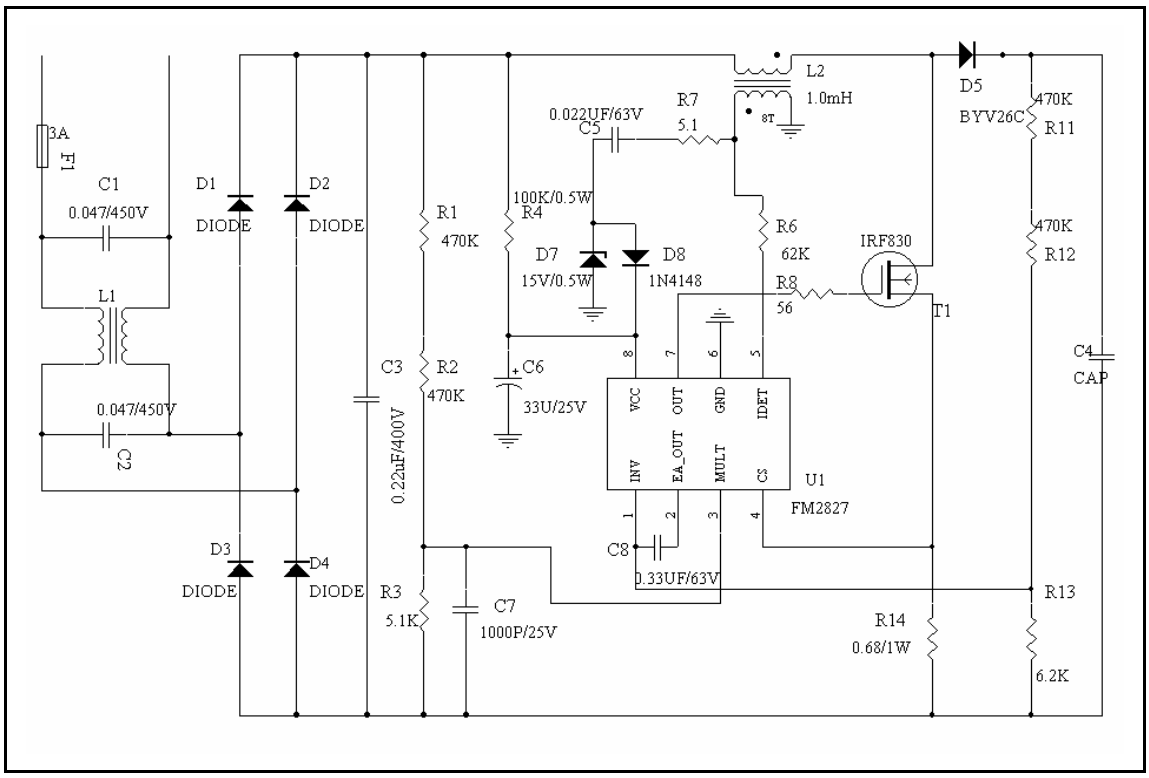
4. Design Example



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5. Ordering Information

Ordering Code	Package	Operation Range
FM2827-PD	DIP8	Industrial Temperature -25°C ~ +125°C
FM2827-SO	SOP8	

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6. Package Dimensions

6.1. 8-Pin DIP Package Dimensions

DIP 8

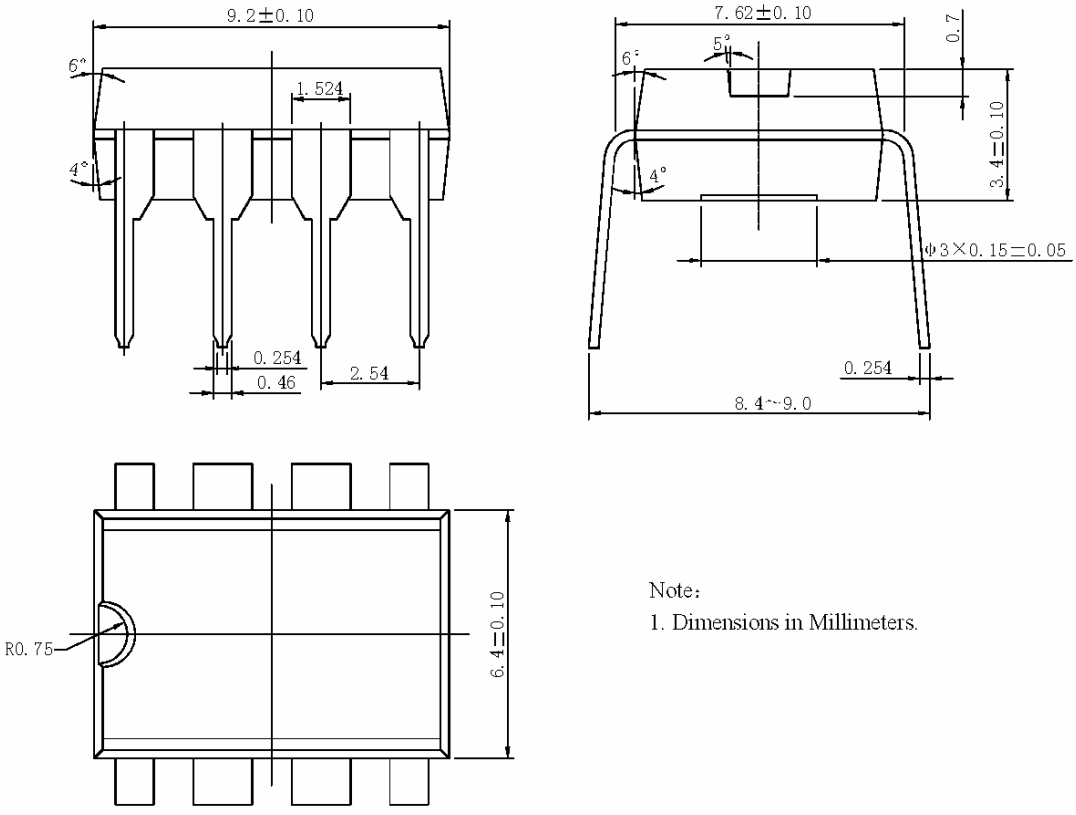

Figure 错误！未找到引用源。-1 FM2827 8-Pin DIP Dimensions

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6.2. 8-Pin SOP Package Dimensions

SOP 8

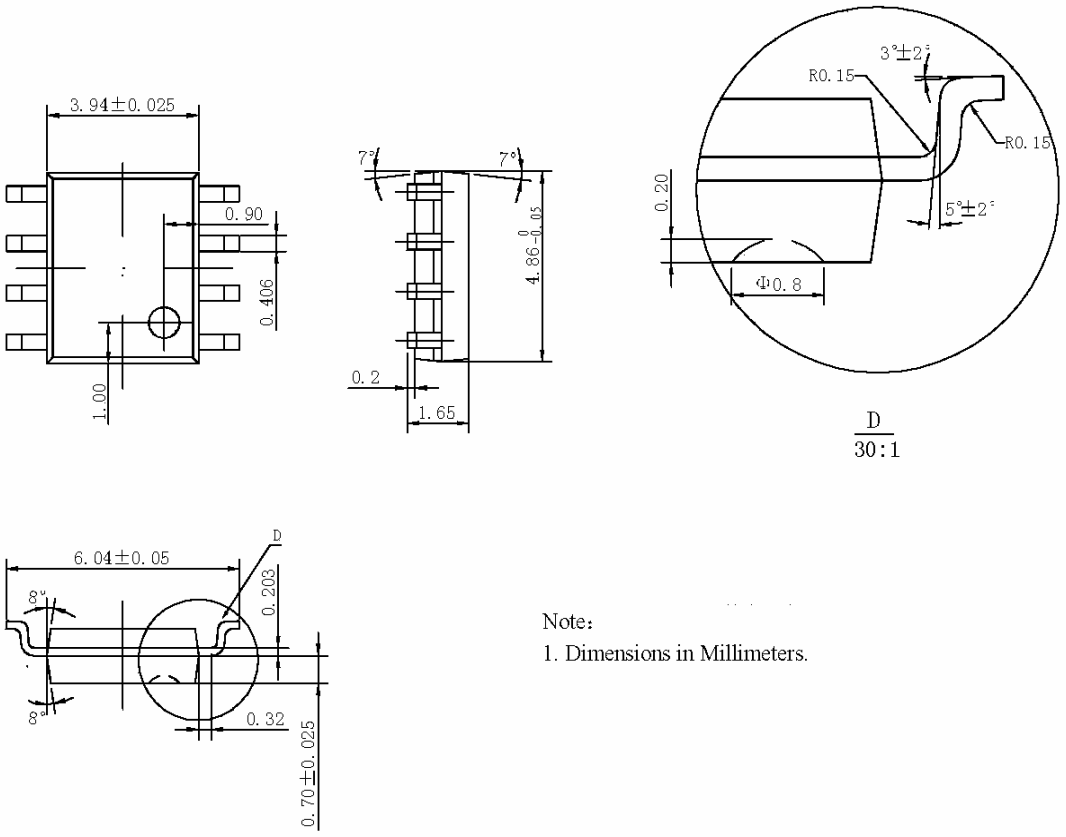

Figure 错误！未找到引用源。-2 FM2827 8-Pin SOP Dimensions

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Revision History

Version	Publication date	Pages	Paragraph or Illustration	Revise Description
1.0	Mar. 2007	14		Initial Release.
2.0	Oct. 2007	14		Updated format.
2.1	May. 2008	14	Sales and service	Updated the address of HK office.

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