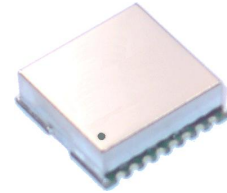


Features

- +5 dBm Output Level at 1690 MHz
- Channel Step Size : 1000 kHz
- 2nd Harmonic : < -20 dBc
- Spurious Level : < -65 dBc
- Lock Time : < 10 ms
- 30 mA Current Consumption

Description

The plerow™ PLL synthesizer module was designed for use in wireless and wireline systems in a wide range of frequency from 50 MHz to 6 GHz. ASB's PLL provides exceptionally low spurious and phase noise performance with fast locking time and low current consumption. All products are available in a surface-mount type package.



Specifications

Parameter	Unit	Min.	Typical	Max.
Frequency Range	MHz		1690	
Output Power	dBm	3	5	7
Supply Voltage	V	4.7	5.0	5.3
Current Consumption	mA		30	40
Channel Step Size	kHz		1000	
2 nd Harmonics	dBc		-25	-20
Spurious Level	dBc			-65
Lock Time	ms			10
Reference Frequency	MHz		13	
Reference Input Level	dBm		-	
Phase Noise (C / N)				
@ 1 kHz	dBc/Hz		-75	-65
@ 10 kHz	dBc/Hz		-105	-95
@ 100 kHz	dBc/Hz		-120	-115
Output Impedance	Ω		50	
Operating Temp. Range	°C	-40	25	85
Package Type & Size	mm	SMT, 19.0W×19.0L×5.8H		

1) Measurement conditions are as follows: T = 25°C, V_{CC} = 5 V, Freq. = 1090 MHz, 50 ohm system.

2) Frequency Stability of internal ref. TCXO is +/-2.5 ppm (max) over the operating temperature range.

More Information

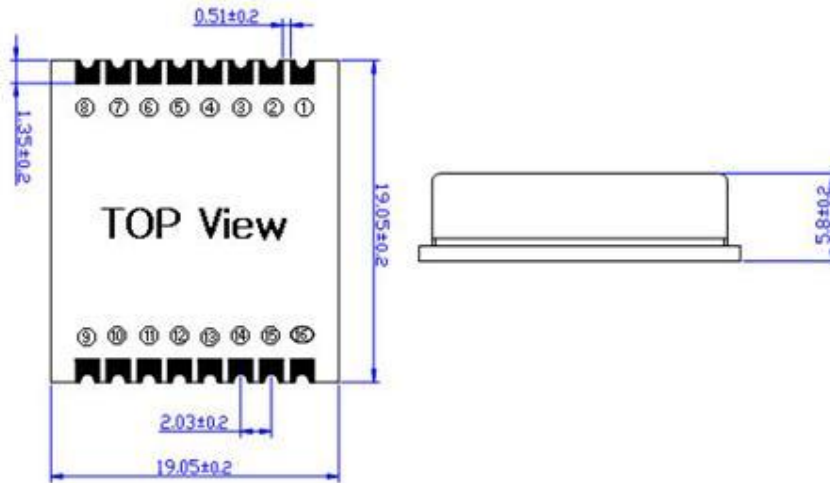
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302-716, Korea

Outline Drawing

Type	Dimension
PLL IC + VCO + ROM + TCXO	19 x 19 x 5.8



Pin Out for PLL			
Pin No.	Application	Pin No.	Application
1	GROUND	9	VCC (VCO)
2	GROUND	13	RF OUT
3	GROUND	15	VCC (PLL)
4	GROUND	16	LOCK DETECT
All other Pins are Grounded / Internal TCXO and ROM			

