APL1581

DUAL INPUT LOW DROPOUT REGULATOR

Features

- **Adjustable or Fixed Output**
- **520mV typ. Dropout at 5A in Dual Power Voltage Mode**
- **Remote Sense Pin Available**
- **2% Accuracy Over Temperature Range**
- **Build-In Over-Temperature Protection**
- **Build-In Current Limit**
- **5 Pin TO-263 and TO-252, SOP-8P Packages**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **Microprocessor Supplies**
- **Chip Set Supplies**
- **VGA Card Power**
- **LCD Monitor Power**

General Description

The APL1581 series of high performance positive voltage regulators are designed for use in applications requiring very low dropout voltage at 5Amp.

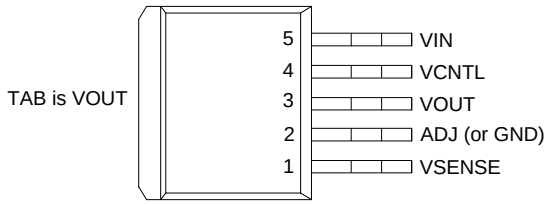
The APL1581 can provide a output voltage at the range of 1.25V to 2.55V where both 5V and 3.3V voltage supplies are available.

The superior dropout characteristics result in reducing heat dissipation compared to regular LDOs. The APL1581 also provides excellent regulation over line, load, and temperature variations.

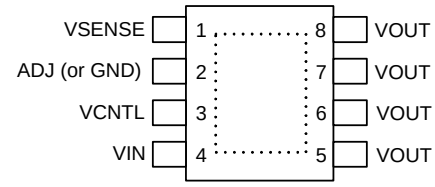
Current limit is trimmed to ensure specified output current and controlled short-circuit current. On-chip thermal limiting provides protection against any combination of overload that would create excessive junction temperature.

The APL1581 is available in both the through-hole and surface mount versions of the industry standard 5-Pin TO-263 and TO-252, SOP-8P power packages.

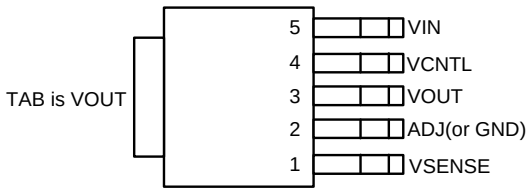
Pin Configuration



Front View of TO-263-5



SOP-8P (Top View)



Front View of TO-252-5

NC = No internal connection

= Thermal Pad (connected to VOUT plane for better heat dissipation)

Pin 5~8 must be connected together by a shortest wide track or plane.

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

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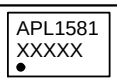
Ordering and Marking Information

APL1581 □□□□□-□□□ Assembly Material Handling Code Temperature Range Package Code Voltage Code	Package Code G5 : TO-263-5 U5 :TO-252-5 KA : SOP-8P Temperature Range C : 0 to 70 °C Handling Code TR : Tape & Reel Voltage Code : 15 : 1.5V 18 : 1.8V 25 : 2.5V Blank : Adjustable Version Assembly Material G : Halogen and Lead Free Device
APL1581-15 G5/U5 : 	XXXXX - Date Code
APL1581-15 KA : 	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1, 2)

Symbol	Parameter	Rating	Unit
V_{IN}	Input Voltage	7	V
V_{CNTL}	Control Voltage	7	V
P_D	Power Dissipation	Internally Limited	W
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note 1 : Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2 : The maximum allowable power dissipation at any T_A (ambient temperature) is calculated using: P_D (max) = $(T_J - T_A) / \theta_{JA}$; T_J = 125°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 3) TO-263-5 (Toplayer plane size : 15mm x 15 mm) TO-252-5 (Toplayer plane size : 10mm x 10 mm) SOP-8P (Toplayer plane size : 10mm x 10 mm)	 28 42 68	°C/W

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Thermal Characteristics (Cont.)

Symbol	Parameter	Typical Value	Unit
θ_{JC}	Junction-to-Case Resistance (Note 4) TO-263-5 TO-252-5	 4 5	°C/W

Note 3 : θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The sizes of the rectangular plane, where the devices are mounted, are shown in the table.

Note 4: The case temperature is measured on the TAB of the device mounted on the test board described in Note 3 except the package TO-220-5. The case temperature of the TO-220-5 is measured on the bottom of the case directly below the die.

Electrical Characteristics

Unless otherwise noted , these specifications apply over C_{IN} = 10µF, C_{CNTL} = 1µF, C_{OUT} = 10µF, and T_A = 0 to 70°C. Typical values refer to T_A = 25°C. $V_{OUT} = V_{SENSE}$.

Symbol	Parameter	Test Conditions	APL1581			Unit
			Min.	Typ.	Max.	
V_{REF}	Reference Voltage APL1581	V_{CNTL}=2.75~5.5V, V_{IN}=2.05~5.5V, I_O =10mA~5A, V_{ADJ}=0V	1.225	1.250	1.275	V
V_{OUT}	Output Voltage APL1581-15 APL1581-18 APL1581-25	(I_O =0~5A for fixed versions) V_{CNTL}=3~5.5V , V_{IN}=2.3~5.5V V_{CNTL}=3.3~5.5V , V_{IN}=2.6~5.5V V_{CNTL}=4~5.5V , V_{IN}=3.3~5.5V	 1.470 1.764 2.450	 1.500 1.800 2.500	 1.530 1.836 2.550	V
REG_{LINE}	Line Regulation APL1581 APL1581-15 APL1581-18 APL1581-25	(I_O =0A for fixed versions) V_{CNTL}=2.75~5.5V, V_{IN}=1.75~5.5V, I_O =10mA, V_{ADJ}=0V V_{CNTL}=3~5.5V, V_{IN}=2.3~5.5V V_{CNTL}=3.3~5.5V, V_{IN}=2.6~5.5V V_{CNTL}=4~5.5V, V_{IN}=3~5.5V	-	-	3	mV
REG_{LOAD}	Load Regulation (Note 5) APL1581 APL1581-15 APL1581-18 APL1581-25	(I_O =0~5A for fixed versions) V_{CNTL}=2.75V, V_{IN}=2.1V, V_{ADJ} =0V, I_O =10mA~5A V_{CNTL}=3V, V_{IN}=2.35V V_{CNTL}=3.3V, V_{IN}=2.65V V_{CNTL}=4V, V_{IN}=3.35V	-	-	5	mV
V_{CNTL}-V_{OUT}	Dropout Voltage (Note 6) APL1581 APL1581-15 APL1581-18 APL1581-25	I_O =5A for all versions V_{IN}=2.05V, V_{ADJ} =0V V_{IN}=2.3V V_{IN}=2.6V V_{IN}=3.3V	-	1.20	1.35	V
V_{IN}-V_{OUT}	Dropout Voltage (Note 6) APL1581 APL1581-15 APL1581-18 APL1581-25	I_O =5A for all versions V_{CNTL}=2.75V, V_{ADJ} =0V V_{CNTL}=3V V_{CNTL}=3.3V V_{CNTL}=4V	-	0.52	0.75	V
I_{LIMIT}	Current Limit	V_{CNTL}-V_{OUT}=1.5V, V_{IN}-V_{OUT}=0.6V	5	-	-	A
I_{LMIN}	Minimum Load Current (Note7) APL1581	V_{CNTL}=5V, V_{IN}=3.3V, V_{ADJ} =0V	-	0.8	10	mA
$REG_{THERMAL}$	Thermal Regulation	30ms Pulse	-	0.01	-	%/W
PSRR	Power Supply Ripple Rejection APL1581 APL1581-15 APL1581-18 APL1581-25	V_{RIPPLE}=1V_{PP} at 120Hz, I_O=5A V_{CNTL}=5V, V_{IN}=5V, V_{ADJ} =0V V_{CNTL}=5.25V, V_{IN}=5.25V V_{CNTL}=5.55V, V_{IN}=5.55V V_{CNTL}=6.25V, V_{IN}=6.25V	60	70	-	dB

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Electrical Characteristics (Cont.)

Unless otherwise noted , these specifications apply over C_{IN}= 10µF, C_{CNTL} = 1µF, C_{OUT} = 10µF, and T_A = 0 to 70°C. Typical values refer to T_A = 25°C. V_{OUT} = V_{SENSE}.

Symbol	Parameter	Test Conditions	APL1581			Unit
			Min.	Typ.	Max.	
I_{CNTL}	CNTL Pin Current	V_{CNTL}-V_{OUT}=1.5V, V_{IN}-V_{OUT}=0.8V, I_O =5A	-	45	120	mA
I_{GND}	Ground Pin Current APL1581-15 APL1581-18 APL1581-25	 V_{CNTL} =3V, V_{IN} =2.3V V_{CNTL} =3.3V, V_{IN} =2.6V V_{CNTL} =4V, V_{IN} =3.3V	-	8	13	mA
I_{ADJ}	Adjust Pin Current APL1581	 V_{CNTL}=2.75V, V_{IN}=2.05V , V_{ADJ} =0V	-	50	120	µA

Note 5 : Low duty cycle pulse test with Kelvin connections are required to maintain data accuracy .

Note 6 : Dropout voltage is defined as the minimum difference between V_{IN} and V_{OUT} required to maintain 1% V_{OUT} regulation.

Note 7 : Minimum load current is defined as the minimum current required at the output to maintain V_{OUT} regulation.

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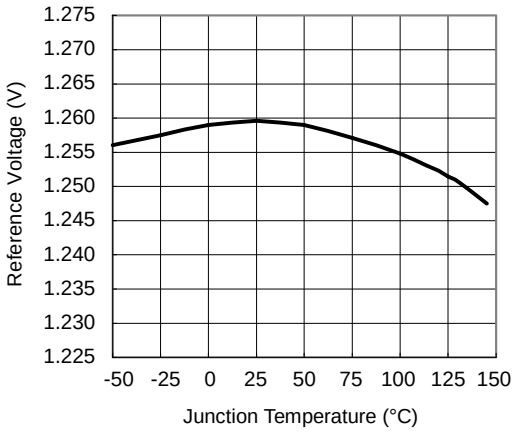
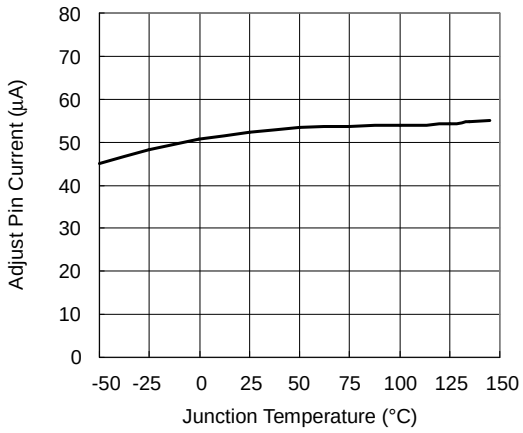
Typical Operating Characteristics

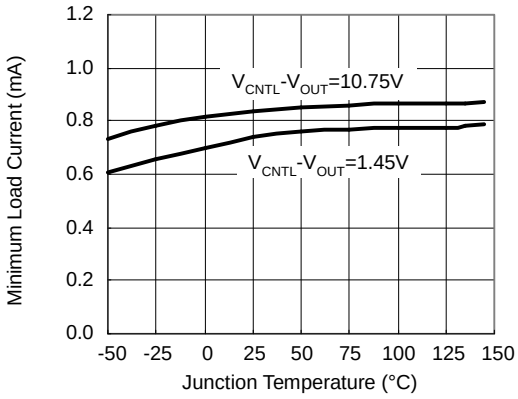
Reference Voltage vs. Junction Temperature



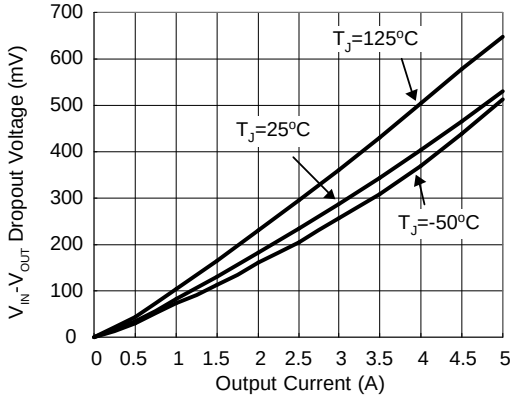
Adjust Pin Current vs. Junction Temperature



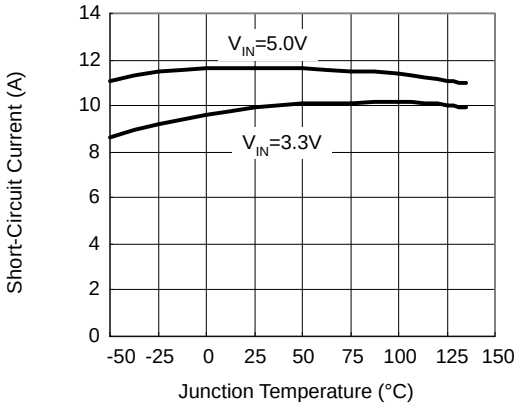
Minimum Load Current vs. Junction Temperature



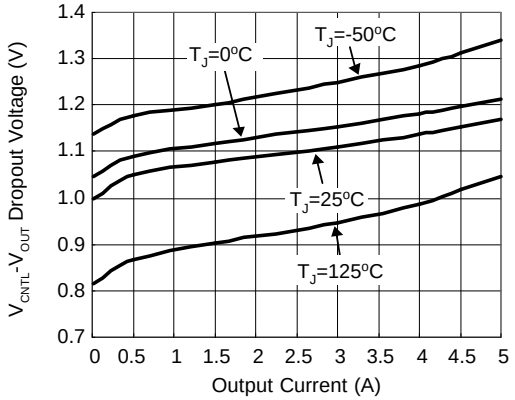
V_{IN}-V_{OUT} Dropout Voltage vs. Output Current



Short-Circuit Current vs. Junction Temperature



$V_{CONTROL}$-V_{OUT} Dropout Voltage vs. Output Current



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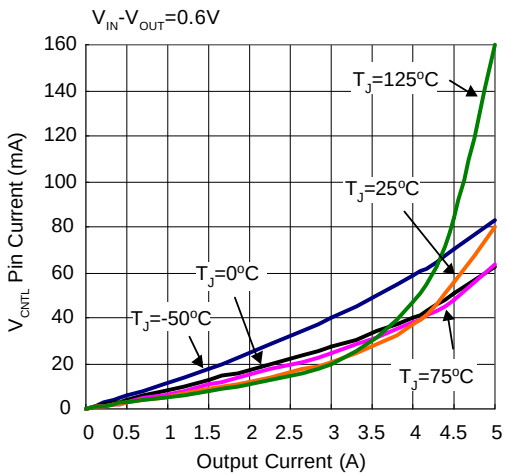
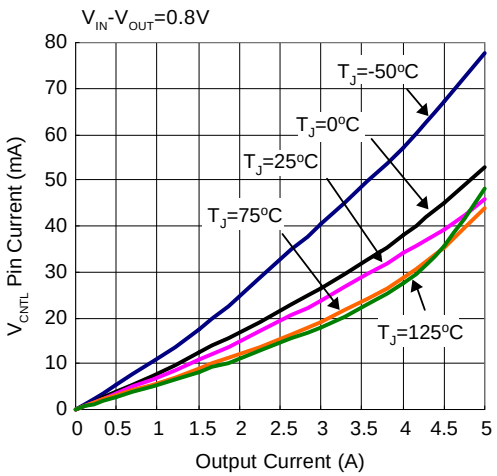
Typical Operating Characteristics (Cont.)

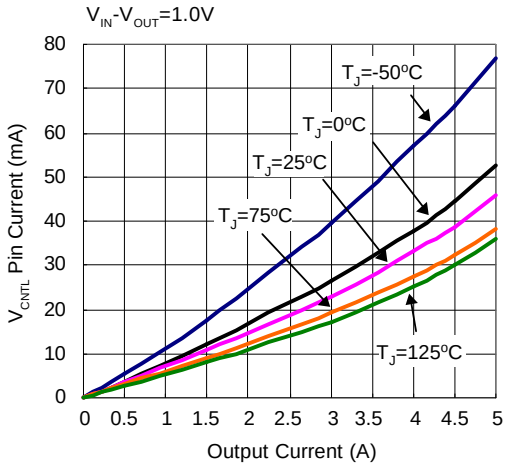
Control Pin Current vs. Output Current



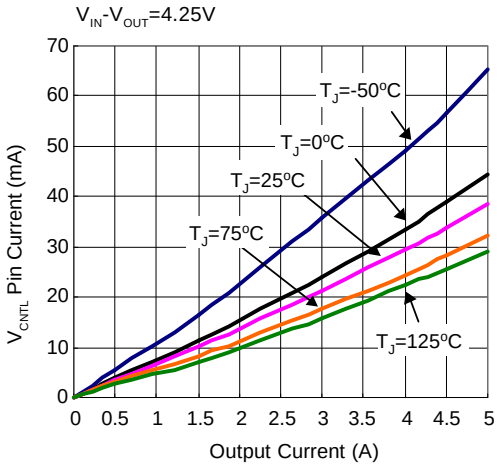
Control Pin Current vs. Output Current



Control Pin Current vs. Output Current



Control Pin Current vs. Output Current



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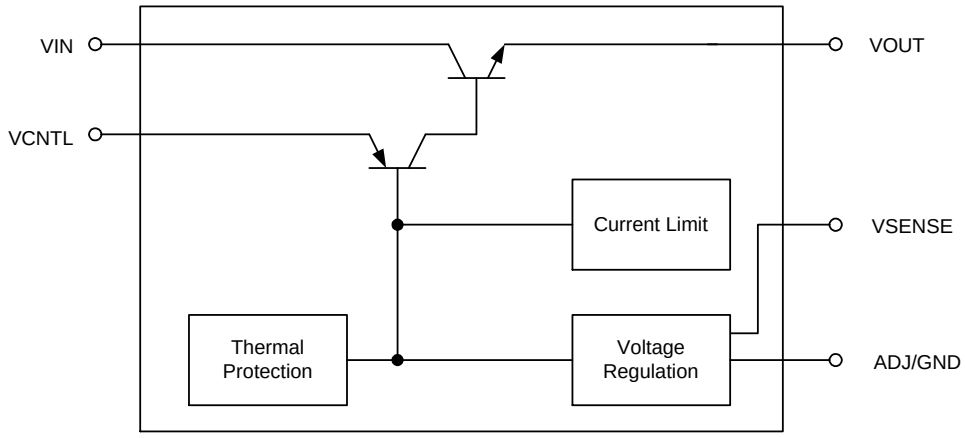
Pin Description

PIN		FUNCTION
NAME	I/O	
VSENSE	I	Positive side of the reference voltage, which allows remote sensing to obtain excellent load regulation.
ADJ	O	Negative side of the reference voltage, which allows to use resistor divider to set an expect output voltage. A small bypass capacitor can be connected from this pin to ground to improve PSRR performance.
GND	O	For fixed voltage devices this is the bottom of the resistor divider that sets the output voltage.
VOUT	O	Output pin of the regulator, which connects to the TAB. A minimum of 10μF capacitor must be connected from this pin to ground to ensure the stability.
VCNTL	I	Supply pin of the control circuitry, which must be always higher than VOUT for the device to regulate. (See electrical characteristics)
VIN	I	Power input pin of the regulator, which must be always higher than VOUT for the device to regulate. (See electrical characteristics)

Block Diagram



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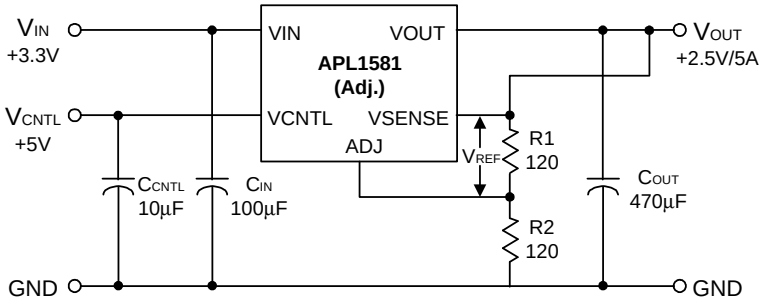
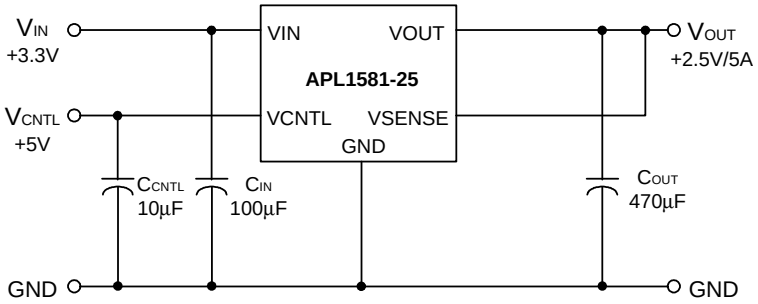
Typical Application Circuit

(1) Adjustable Output Voltage Device

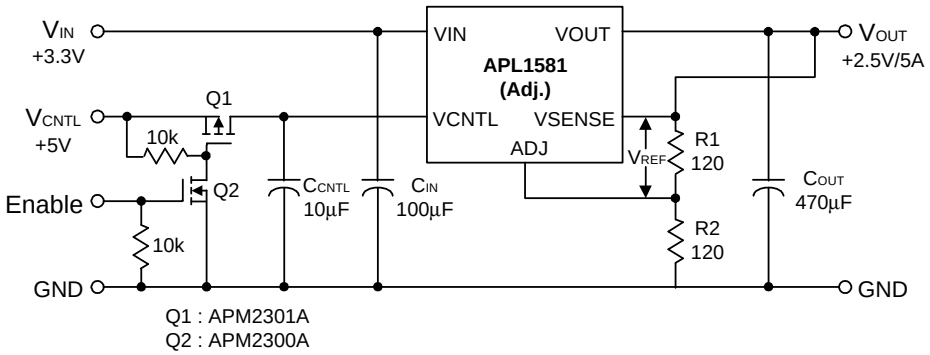


* $V_{OUT} = V_{REF} (1+ R2 / R1) + I_{ADJ} \times R2$
where V_{REF} =1.25V (typical)
I_{ADJ}=50µA (typical)
* R1 is typically in range of 100Ω to 125Ω to satisfy the minimum load current requirement.

(2) Fixed Output Voltage Device



(3) With Enable Control Application



Q1 : APM2301A
Q2 : APM2300A

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Application Information

General

The APL1581 (adjustable or fixed) regulator is a 5 terminal device designed specifically to provide extremely low dropout voltages comparable to the PNP type without the disadvantage of the extra power dissipation due to the base current associated with PNP regulators. This is done by bringing out the control pin of the regulator that provides the base current to the power NPN and connecting it to a voltage that is greater than the voltage present at the VIN pin. This flexibility makes APL1581 ideal for applications where dual inputs are available, such as a computer motherboard with an ATX power supply that provides 5V and 3.3V to the board.

APL1581 is equipped with a 1.25V reference, precision and fast voltage regulations, on-chip current and thermal limits, and remote sensing capability to reduce system total cost.

APL1581 is available in SOP-8P, TO-252-5, and TO-263-5 packages to meet different power dissipation applications.

Output Voltage Setting

See Figure 1 Adjustable APL1581 develops a 1.25V reference voltage between the VSENSE pin and the ADJ pin. Placing a resistor between these two terminals causes a constant current to flow through R1 and down through R2 to set the overall output voltage. In general, R1 is chosen so that this current is the specified minimum load current of 10mA. The current out of the ADJ pin is small, typically 50µA and itadds to the current from R1. Because IADJ is very small, it needs to be considered only when very precise output voltage setting is required. For best regulation, the top of the resistor divider should be connected directly to the SENSE pin. The adjustable APL1581 can be programmable to any voltages in the range of 1.25V to 5.5V according to the following formula:

$$V_{OUT} = V_{REF} \times (1 + \frac{R2}{R1}) + I_{ADJ} \times R2$$

where

V_{REF} = 1.25V (typical)

I_{ADJ} = 50µA (typical)

The recommended R1 is in range of 100Ω to125Ω to satisfy the minimum load current requirement. Proper sizes of R2 and R1 are also concerned for power dissipation.

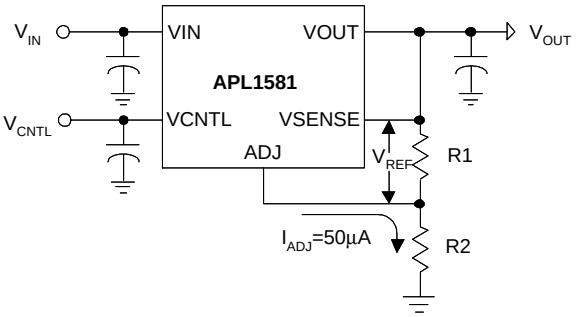
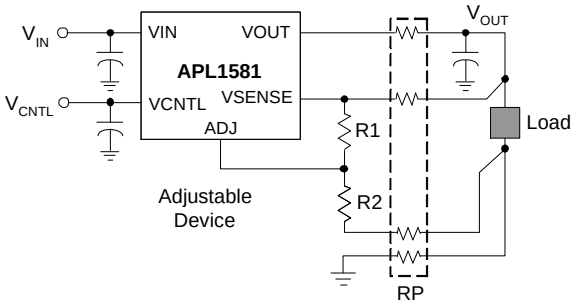


Figure 1. Setting Output Voltage

Grounding and Output Sensing

The APL1581 allows true Kelvin sensing for both the high and low side of the load. Figure 2 shows the device connected to take advantage of the remote sense feature. The SENSE pin and the top of the resistor divider are connected to the top of the load; the bottom of the resistor divider is connected to the bottom of the load. Typically the load is a microprocessor and parasitic resistance RP is made up of the PC traces and /or connector resistance between the regulator and the processor. RP is now connectedinside the regulation loop of the APL1581 and for reasonable values of RP the load regulation at the load will be negligible. Voltage drops due to RP are not eliminated; they will add to the dropout voltage of the regulator regardless of whether they are inside or outside the regulation loop.



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Application Information (Cont.)

Grounding and Output Sensing (Cont.)

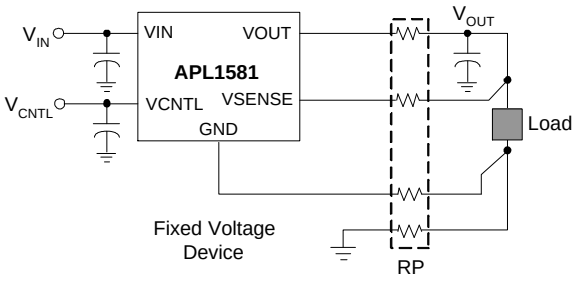
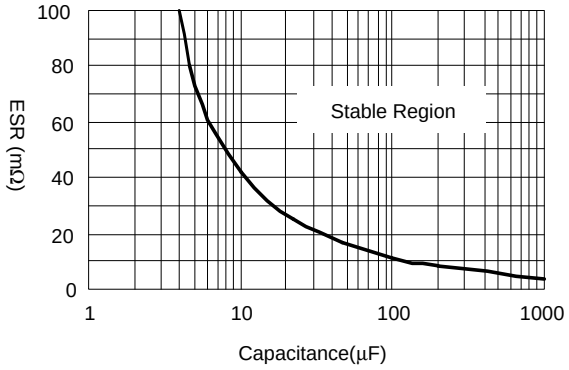


Figure 2. Remote Voltage Sensing

Stability and Output Capacitors

The circuit design of using the APL1581 series requires an output capacitor as part of the device frequency compensation. The following chart shows a stable region to select output capacitor for APL1581. This region above the curve indicates minimum required ESR and capacitance to maintain stability. However, the output capacitor should have an ESR less than 1Ω.



A low-ESR solid tantalum and aluminum electrolytic capacitor (ESR<1Ω) works extremely well and provides good transient response and stability over temperature. Ultra-low-ESR capacitors, such as ceramic chip capacitors, may promote unstable or under-damped transient response, but proper ceramic chip capacitors placed near loads can be used as decoupling capacitors.

The output capacitors are also used to reduce the slew rate of load current and help the APL1581 to minimize variations of the output voltage, improving transient response. For this purpose, the low-ESR capacitors are recommended.

Input Capacitors

The input capacitors of VCNTL and VIN pins are not required for stability but for supplying surge currents during large load transients, and this will prevent the input rail from drooping and improve the performance of the APL1581. Because parasitic inductors from voltage sources or other bulk capacitors to the VCNTL and VIN pins will limit the slew rate of the surge currents during large load transients, resulting in voltage drop at VIN and VCNTL pins.

A capacitor of 1μF (ceramic chip capacitor) or greater (aluminum electrolytic capacitor) is recommended and connected near VCNTL pin. For VIN pin, an aluminum electrolytic capacitor (>33μF) is recommended. It is not necessary to use low-ESR capacitors. More capacitance reduces the variations of the input voltage at VIN pin.

Layout and Thermal Consideration

The APL1581 series have internal power and thermal limiting (T_J=150°C typical) circuitry designed to protect the device under overload conditions. However, maximum junction temperature ratings should not be exceeded under continuous normal load conditions. Careful consideration must be given to all sources of thermal resistance from junction to ambient, including junction-to-case, case-to-heat sink interface, and heat sink resistance itself. See Figure 3 The SOP-8P is a cost-effective package featuring a small size as a standard SOP-8 and a bottom thermal pad to minimize the thermal resistance of the package, being applicable to high current applications. The thermal pad is soldered to the top VOUT plane which may be connected to internal or bottom VOUT plane by vias to reduce the heat sink thermal resistance. Therefore, the printed circuit board (PCB) forms a heat sink and dissipates heat into ambient air.

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Application Information (Cont.)

Layout and Thermal Consideration (Cont.)

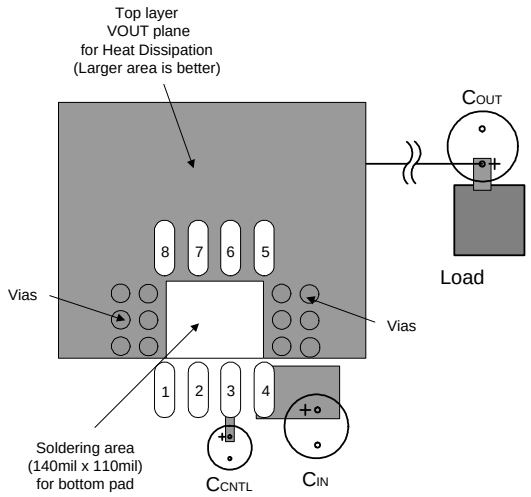

Figure 3. Recommended SOP-8P Layout

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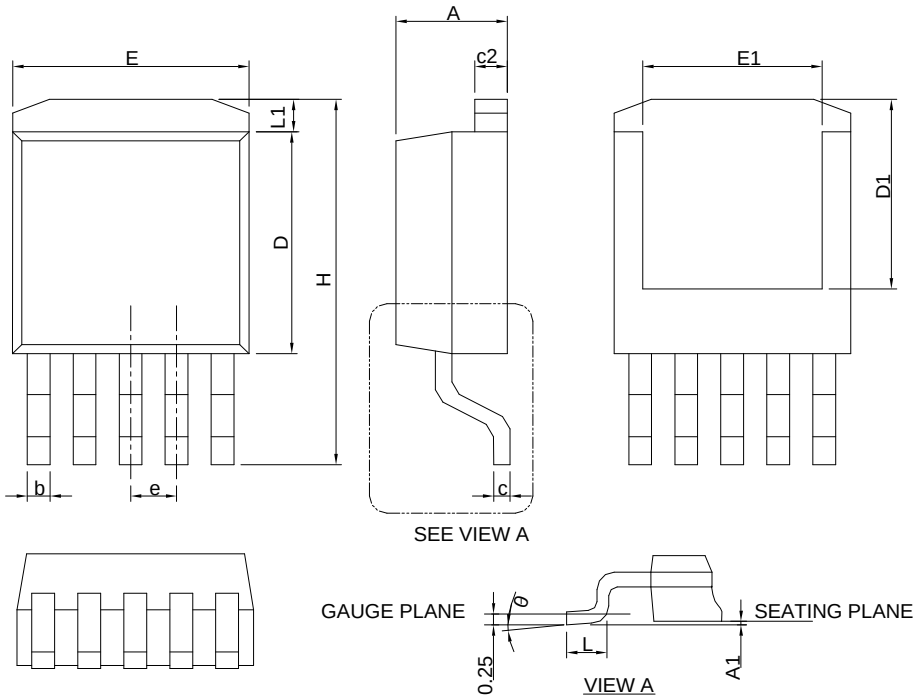
Package Information

TO-263-5



SYMBOL	TO-263-5			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
c	0.38	0.74	0.015	0.029
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380
D1	6.00	9.00	0.236	0.354
E	9.65	11.43	0.380	0.450
E1	6.22	9.00	0.245	0.354
e	1.70 BSC		0.067 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1		1.68		0.066
θ	0°	8°	0°	8°

Note : Follow from JEDEC TO-263 BB.

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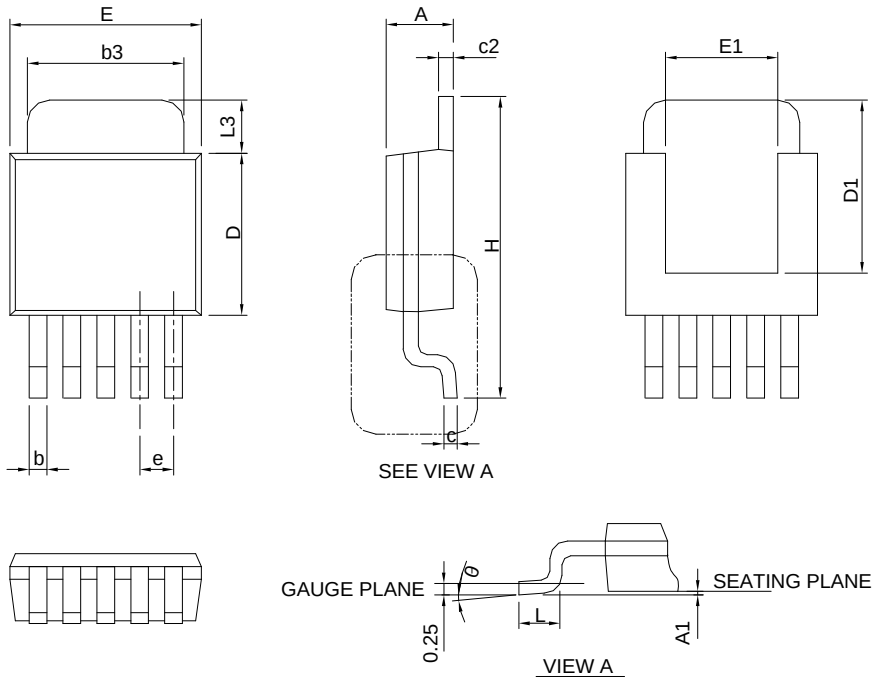
Package Information

TO-252-5



SYMBOL	TO-252-5			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.39	0.086	0.094
A1		0.13		0.005
b	0.50	0.89	0.020	0.035
b3	4.32	5.46	0.170	0.215
c	0.46	0.61	0.018	0.024
c2	0.46	0.89	0.018	0.035
D	5.33	6.22	0.210	0.245
D1	4.57	6.00	0.180	0.236
E	6.35	6.73	0.250	0.265
E1	3.81	6.00	0.150	0.236
e	1.27 BSC		0.050 BSC	
H	9.40	10.41	0.370	0.410
L	1.40	1.78	0.055	0.070
L3	0.89	2.03	0.035	0.080
θ	0°	8°	0°	8°

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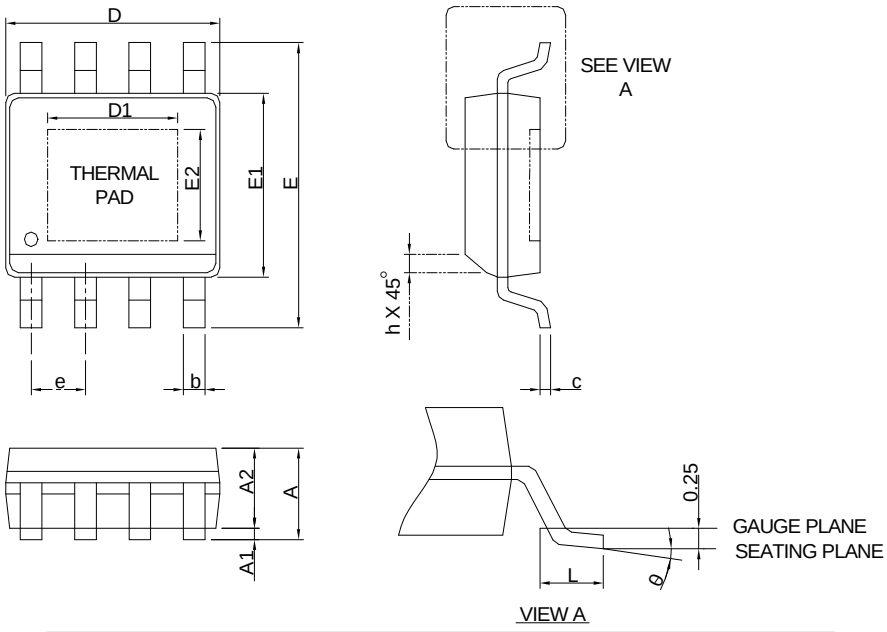
Package Information

SOP-8P



SYMBOL	SOP-8P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.60		0.063
A1	0.00	0.15	0.000	0.006
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
D1	2.25	3.50	0.098	0.138
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
E2	2.00	3.00	0.079	0.118
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note : 1. Follow JEDEC MS-012 BA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .

3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

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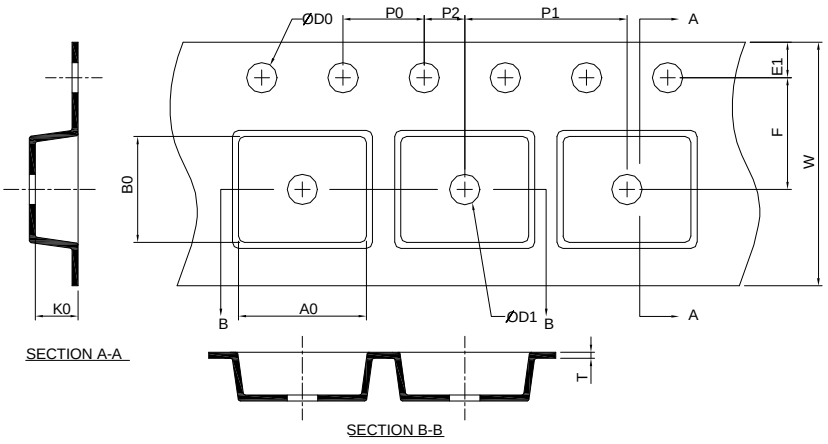
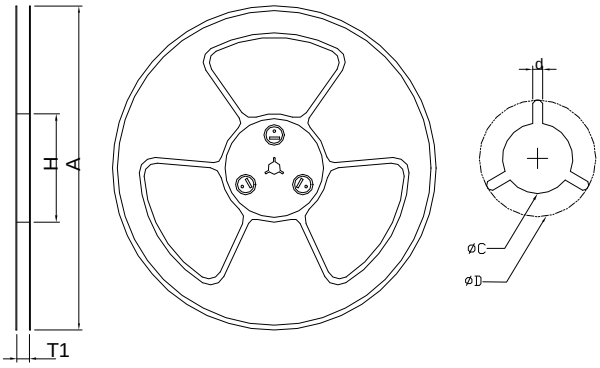
Carrier Tape & Reel Dimensions





Application	A	H	T1	C	d	D	W	E1	F
TO-263-5	330.0±2.00	50 MIN.	24.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	24.0±0.30	1.75±0.10	11.5±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	16.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	10.8±0.20	16.1±0.20	5.2±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
TO-252-5	330.0±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	16.0±0.30	1.75±0.10	7.50±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.80±0.20	10.40±0.20	2.50±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
SOP-8P	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20

(mm)

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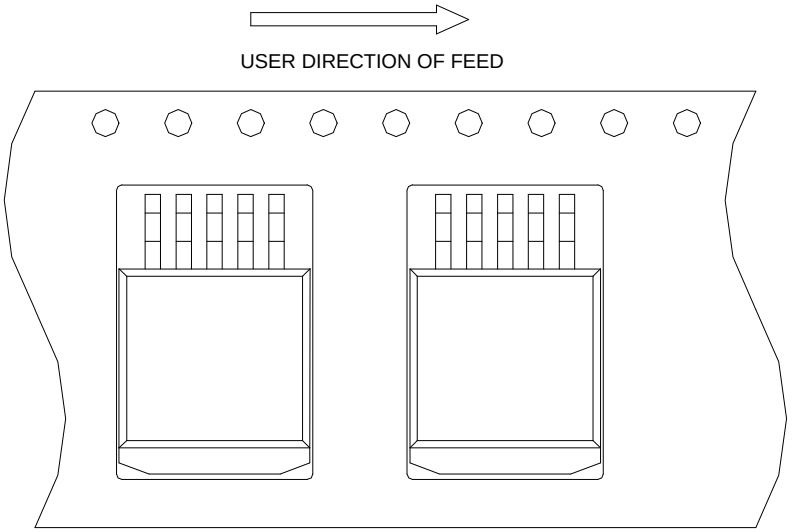
Devices Per Unit

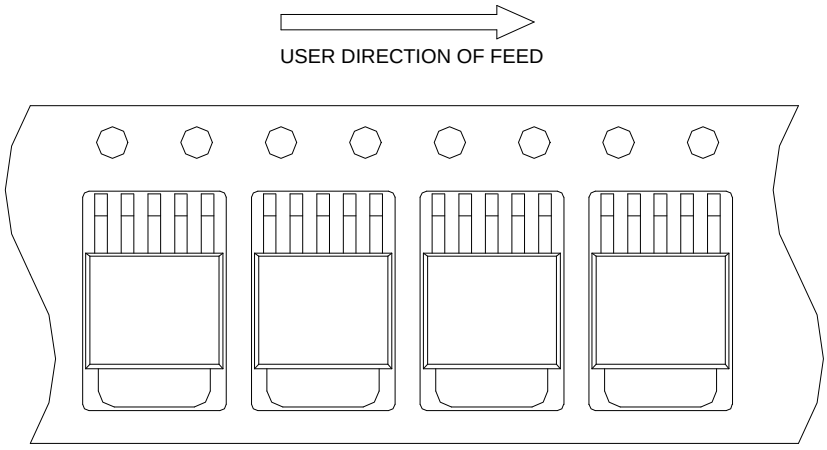
Package Type	Unit	Quantity
TO-252-5	Tape & Reel	2500
TO-263-5	Tape & Reel	800
SOP-8P	Tape & Reel	2500

Taping Direction Information

TO-263-5



TO-252-5



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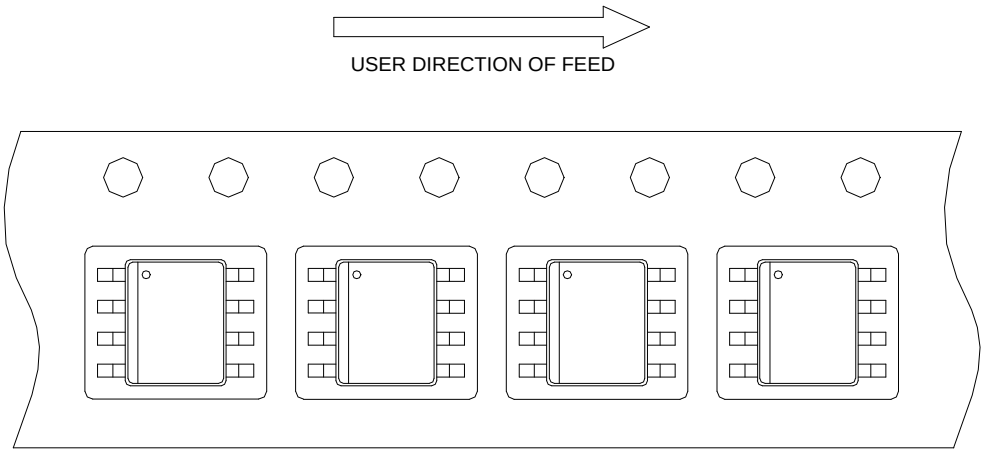
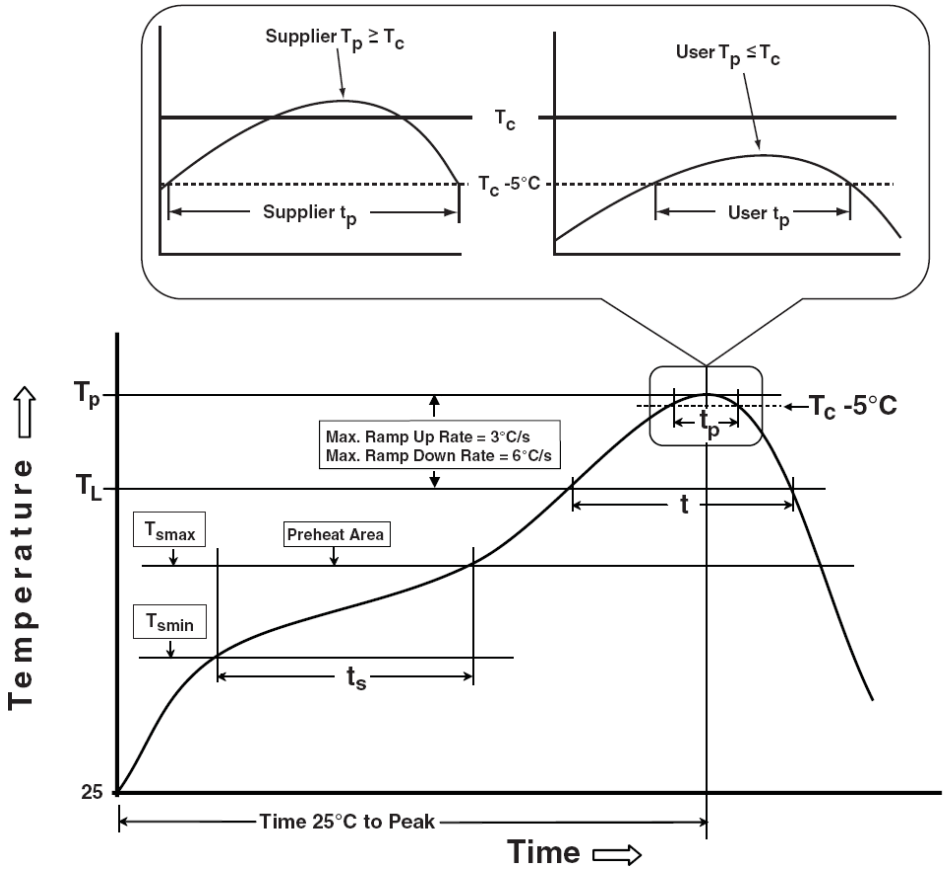
Taping Direction Information

SOP-8P



Classification Profile



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Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ 125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
ESD	MIL-STD-883-3015.7	VHBM≧2KV, VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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