

600mA Linear Regulator for DC Fan Speed Control

Features

- **Low Dropout Voltage: 220mV (typical) @ 600mA**
- **Low Quiescent Current: 140mA**
- **Enable/Shutdown function**
- **Output Voltage / VSET Voltage: 1.6 times**
- **Stable with Low ESR Ceramic Capacitors**
- **Over-Temperature Protection**
- **Current Limit Protection with Foldback Current**
- **Internal Soft-start**
- **SOP-8 Package**
- **Lead Free Available (RoHS Compliant)**

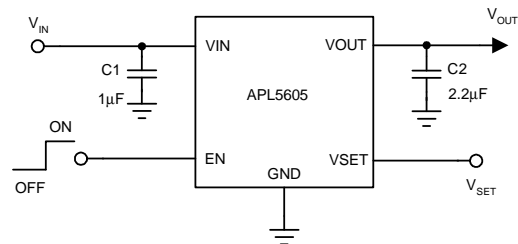
General Description

The APL5605 is a low quiescent current and low dropout linear regulator which is designed to power a DC fan and delivers up to 600mA output current. The output voltage follows the 1.6 times of VSET voltage and typical dropout voltage is only 220mV (typical) at 600mA output current. The APL5605 with low 140µA quiescent current is ideal for battery-powered system appliances and stable with a 2.2µF ceramic output capacitor. The features of current limit (with foldback current) and over-temperature protection protect the device against current over-loads and over temperature. The APL5605 is available in a SOP-8 package.

Applications

- **Notebook Fan Driver**
- **Motherboards**
- **PC Peripherals**
- **Battery-Powered System**

Simplified Application Circuit



Ordering and Marking Information

<p>APL5605 □□-□□□</p> <div style="margin-left: 20px;"> <p>└─ Lead Free Code</p> <p>└─ Handling Code</p> <p>└─ Temperature Range</p> <p>└─ Package Code</p> </div>	<p>Package Code K : SOP-8</p> <p>Operating Ambient Temperature Range I : -40 to 85°C</p> <p>Handling Code TR : Tape & Reel</p> <p>Lead Free Code L : Lead Free Device</p>
<p>APL5605 K :</p> <div style="border: 1px solid black; padding: 2px; display: inline-block; margin-left: 20px;"> <p>APL5605 XXXXX</p> </div>	<p>XXXXX - Date Code</p>

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldering operations. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

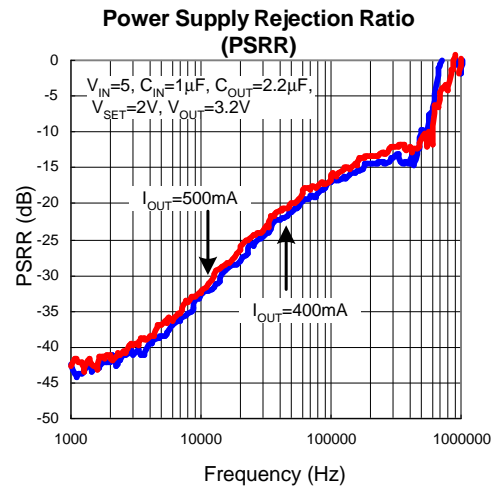
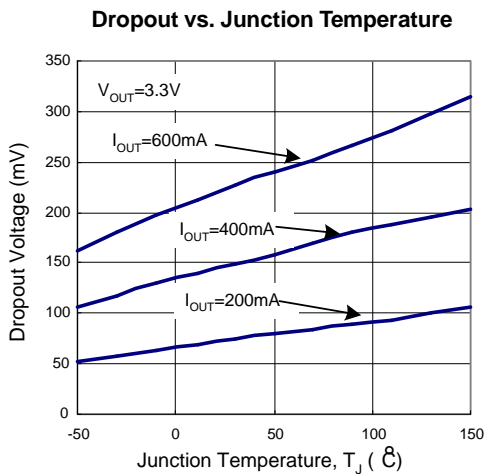
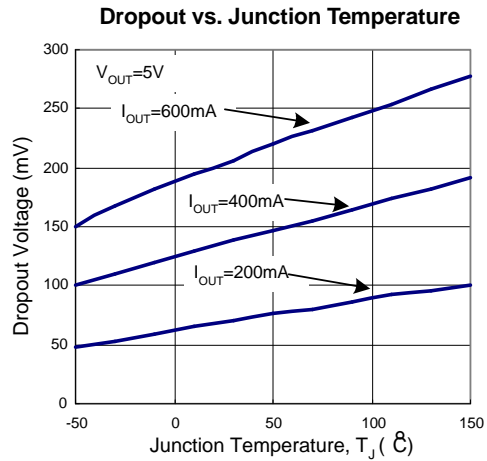
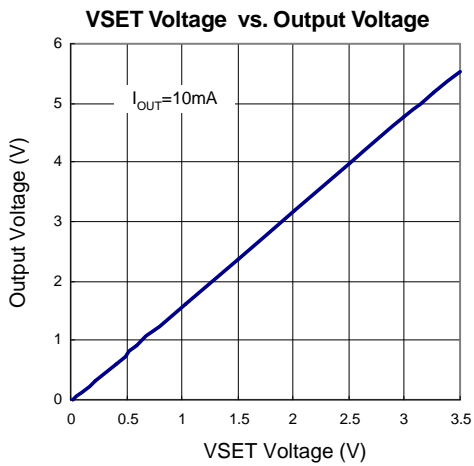
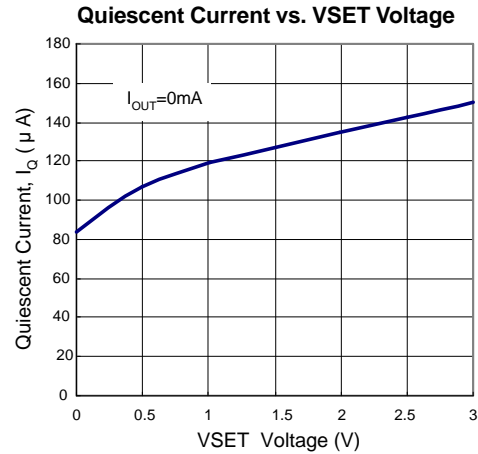
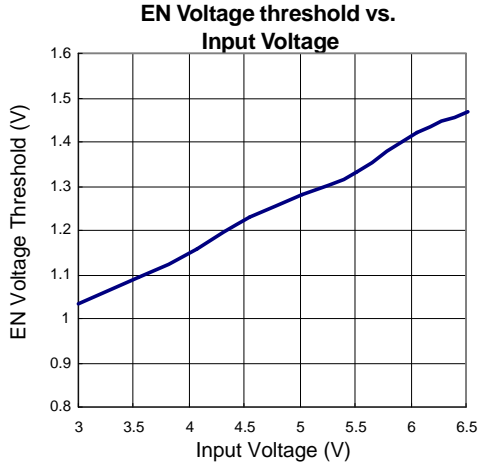
Electrical Characteristics

Refer to the typical application circuit. $V_{IN} = 5V$, $V_{EN} = V_{IN}$, $I_{OUT} = 1mA \sim 600mA$, $T_J = -40$ to $125^\circ C$, $T_A = -40$ to $85^\circ C$, unless otherwise specified. Typical values are at $T_A = 25^\circ C$.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
SUPPLY CURRENT						
I_Q	Quiescent Current	$V_{EN} = 0V$	-	-	1	μA
		$V_{EN} = 5V, I_{OUT} = 0A$	-	140	200	μA
UNDER-VOLTAGE-LOCKOUT (UVLO)						
	VIN UVLO Threshold	V_{IN} rising	2.1	2.5	2.9	V
	VIN UVLO Hysteresis		-	0.15	-	V
OUTPUT VOLTAGE						
	VOUT Voltage / VSET Voltage	$T_J = 25^\circ C, V_{IN}=5.5V, I_{OUT}=1mA, V_{SET}=3.3V$	1.552	1.6	1.648	V/V
	VOUT Voltage / VSET Voltage	$T_J = 40 \sim 125^\circ C, V_{IN}=5.5V, I_{OUT}=1mA, V_{SET}=1 \sim 3.3V$	1.504	1.6	1.696	V/V
	VSET pin Current	$V_{SET}=5V$	-	0.05	1	μA
	Load Regulation	$I_{OUT} = 1mA$ to $600mA$	-	60	100	mV
V_{DROP}	Dropout Voltage	$I_{OUT}=600mA, V_{OUT}=2.5V$	-	250	400	mV
		$I_{OUT}=600mA, V_{OUT}=3.3V$	-	220	350	mV
		$I_{OUT}=600mA, V_{OUT}=5V$	-	200	320	mV
PROTECTION AND SOFT-START						
	Output Current Limit		700	-	-	mA
	Thermal Shutdown Temperature		-	150	-	$^\circ C$
	Thermal Shutdown Hysteresis		-	40	-	$^\circ C$
	Foldback Current Limit	$V_{OUT} < 0.6V$	-	250	-	mA
T_{SS}	Soft-Start Time		-	130	300	μs
	VOUT Pull Low Resistance	$V_{EN}=0V, V_{OUT}=0.5V$	-	60	-	Ω
LOGIC INPUT						
	EN Logic Input-High Level		1.6	-	-	V
	EN Logic Input-Low Level		-	-	0.4	V
	EN Pull-Low Resistance	$V_{EN}<3V$	-	2	-	M Ω

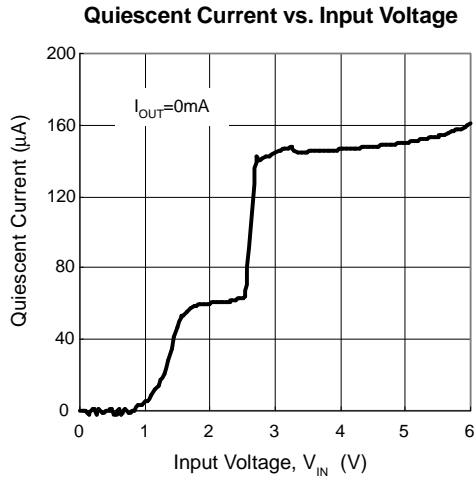
Typical Operating Characteristics

$V_{IN}=5V$, $V_{SET}=2V$, $V_{OUT}=3.2V$, $C_{IN}=1\mu F$, $C_{OUT}=2.2\mu F$, unless otherwise specified.



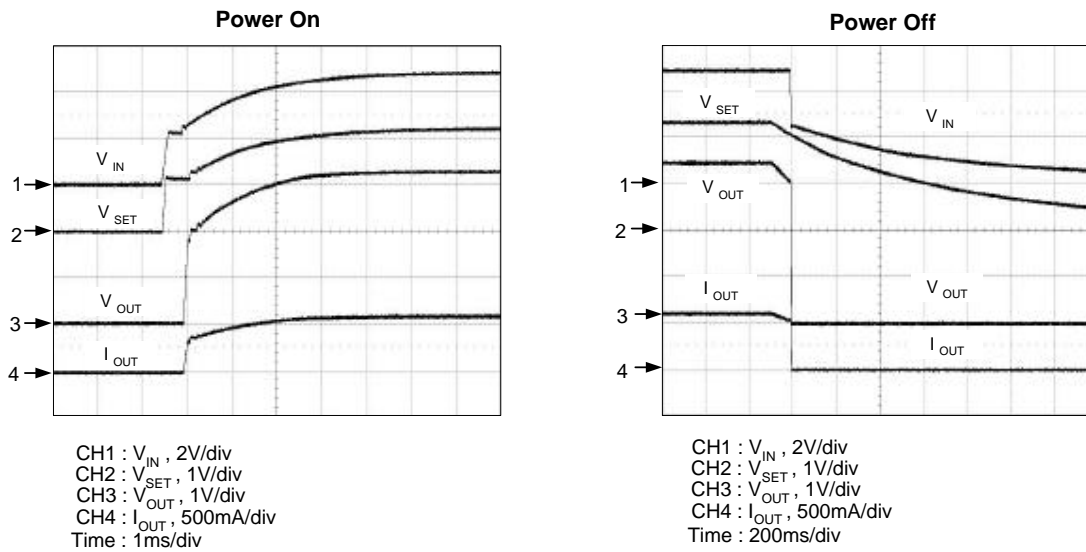
Typical Operating Characteristics (Cont.)

$V_{IN}=5V$, $V_{SET}=2V$, $V_{OUT}=3.2V$, $C_{IN}=1\mu F$, $C_{OUT}=2.2\mu F$, unless otherwise specified.



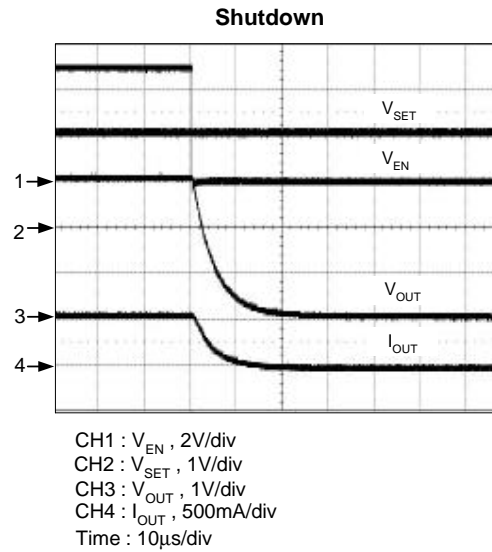
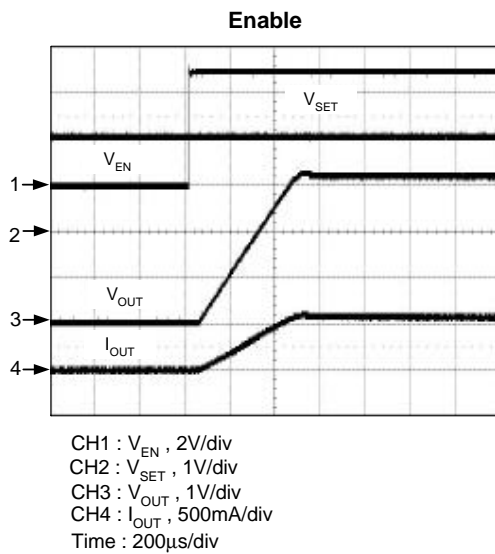
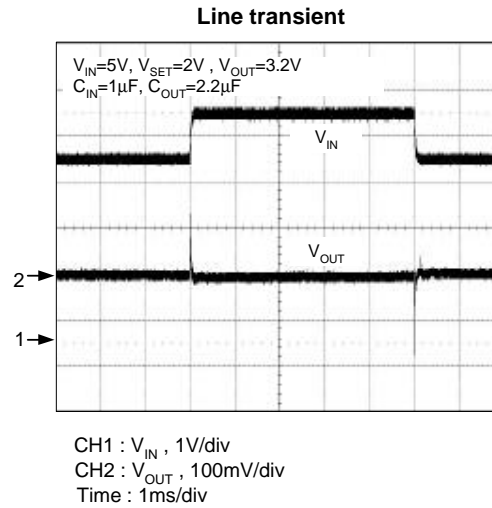
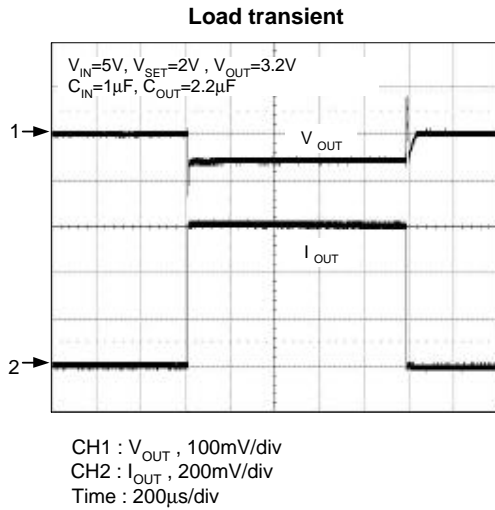
Operating Waveforms

$V_{IN}=5V$, $V_{SET}=2V$, $V_{OUT}=3.2V$, $C_{IN}=1\mu F$, $C_{OUT}=2.2\mu F$, unless otherwise specified.



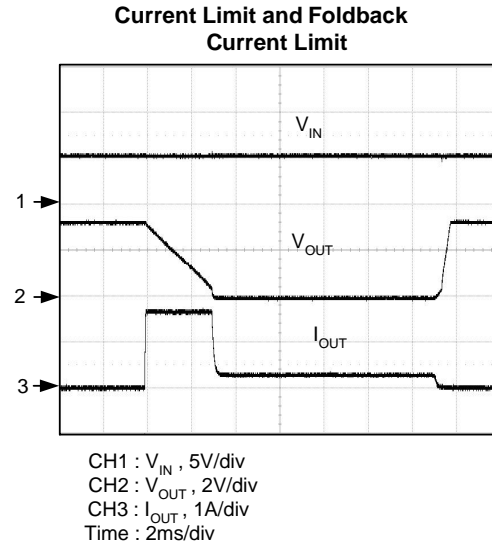
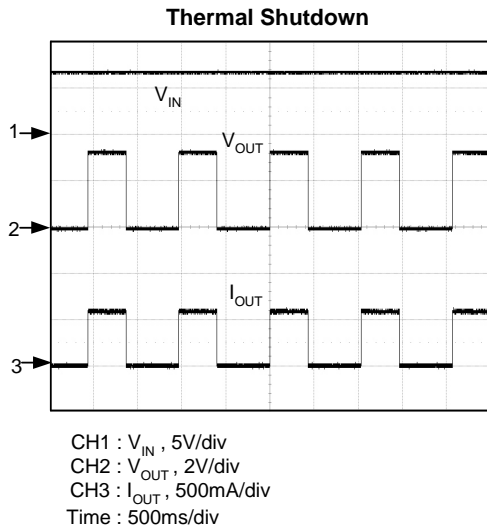
Operating Waveforms (Cont.)

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Operating Waveforms (Cont.)

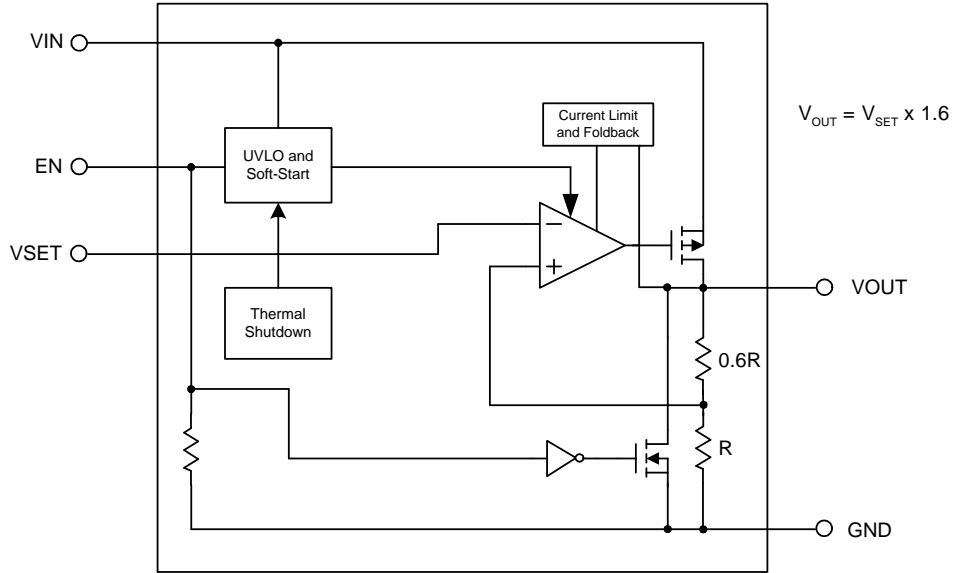
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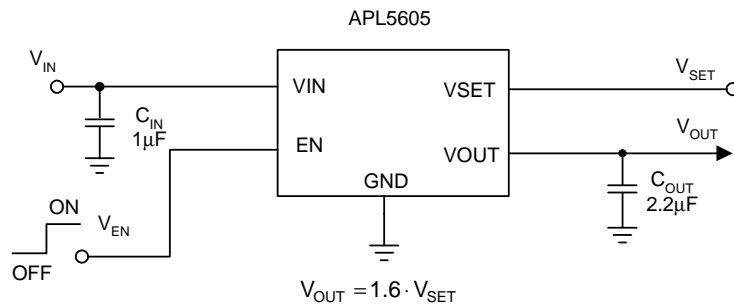
Pin Descriptions

Pin		Function Descriptions
No.	Name	
1	EN	Enable Control Input. Driving the EN high turns on the regulator. Pulling the EN low turns the regulator into shutdown mode. The EN is pulled low by an internal resistor.
2	VIN	Supply Voltage Input Pin. Supply voltage can range from 4.5V to 6V. Bypass with a 1μF (typical) capacitor to GND
3	VOU	Regulator Output. Sources up to 600mA. A small capacitor is needed from this pin to ground to assure stability.
4	VSET	Output Voltage-Set Input. The output voltage follows the 1.6 times of the VSET voltage.
5,6,7,8	GND	Ground. These pins are internally connected with the internal leadframe. Connect these pins to a wide ground plane for good heat dissipation.

Block Diagram



Typical Application Circuit



Function Descriptions

Under-Voltage Lock-Out (UVLO)

The APL5605 has a built-in under-voltage lock-out circuit to keep the output off until the internal circuitry is operating properly. The UVLO function initiates a soft start process after input voltage exceeds its rising UVLO threshold during power on. Typical UVLO threshold is 2.5V with 0.15V hysteresis.

Soft-Start

The APL5605 provides an internal soft-start circuitry to control rise rate of the output voltage and limit the current surge during start-up. Approximate 20 μ s delay time after the V_{IN} is over the UVLO threshold, the IC starts a soft-start. The typical soft-start interval is about 130 μ s.

Enable/Shutdown

Driving the EN high turns on the regulator, driving the EN low puts the regulator into shutdown mode. A logic low also causes the output voltage to discharge to GND. The EN is pulled low by an internal resistor.

Current Limit

The APL5605 provides a current limit circuitry, which monitors the output current and controls P-MOS's gate voltage to limit the output current at 700mA.

Foldback Current Limit

When the output voltage drops below 0.6V (typical), which is caused by over load or short circuit, the foldback current limit circuitry limits the output current to 250mA. The foldback current limit is used to reduce the power dissipation during short circuit condition. The foldback current limit is disabled for 0.8ms (typical) after UVLO threshold is reached, so that the IC has normal 700mA (typical) current limit level during start-up.

Thermal Shutdown

A thermal shutdown circuit limits the junction temperature of APL5605. When the junction temperature exceeds +150°C, the thermal shutdown circuitry disables the output, allowing the device to cool down. The output circuitry is enabled again after the junction temperature cools down by 40°C, resulting in a pulsed output during continuous thermal overload conditions.

Application Information

Input Capacitor

The APL5605 requires proper input capacitors to supply surge current during stepping load transients to prevent the input rail from dropping. Because the parasitic inductor from the voltage sources or other bulk capacitors to the VIN limits the slew rate of the surge current, place the Input capacitors near VIN as close as possible. Input capacitors should be larger than 0.82μF.

Output Capacitor

The APL5605 needs a proper output capacitor to maintain circuit stability and to improve transient response over temperature and current. In order to insure the circuit stability, the proper output capacitor value should be larger than 1μF. With X5R and X7R dielectrics, 2.2μF is sufficient at all operating temperatures. Maximum output capacitor should be less than 330μF to insure the system can be powered on effectively.

Operation Region and Power Dissipation

The APL5605 maximum power dissipation depends on the thermal resistance and temperature difference between the die junction and ambient air. The power dissipation P_D across the device is:

$$P_D = \frac{(T_J - T_A)}{\theta_{JA}}$$

where $(T_J - T_A)$ is the temperature difference between the junction and ambient air. θ_{JA} is the thermal resistance between Junction and ambient air. Assuming the $T_A = 25^\circ\text{C}$ and maximum $T_J = 150^\circ\text{C}$ (typical thermal limit threshold), the maximum power dissipation is calculated as:

$$P_{D(max)} = (150 - 25) / 80 = 1.56(W)$$

For normal operation, do not exceed the maximum junction temperature rating of $T_J = 125^\circ\text{C}$. The calculated power dissipation should less than:

$$P_D = (125 - 25) / 80 = 1.25(W)$$

The GND provides an electrical connection to ground and channels heat away. Connect the GND to ground by using a large pad or ground plane.

PCB Layout Considerations

Figure 1 illustrates the layout. Below is a checklist for your layout:

1. Please place the input capacitors close to the VIN
2. Ceramic capacitors for load must be placed near the load as close as possible
3. To place APL5605 and output capacitors near the load is good for performance.
4. Large current paths, the bold lines in figure 1, must have wide tracks.

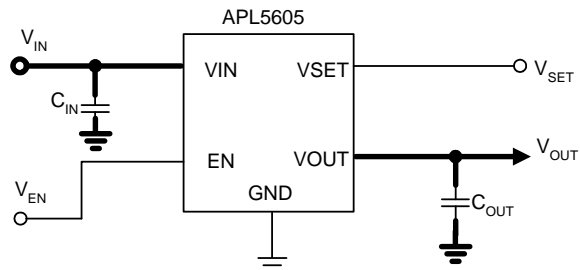


Figure 1

Optimum performance can only be achieved when the device is mounted on a PC board according to the SOP-8 Board Layout diagram.

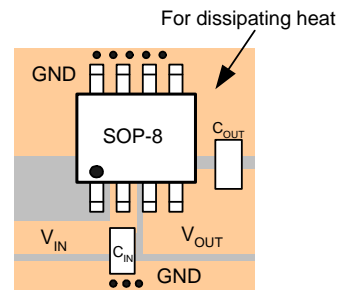
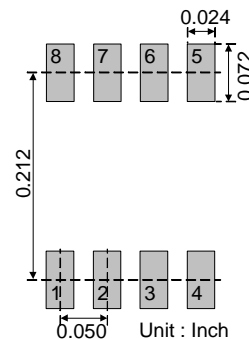


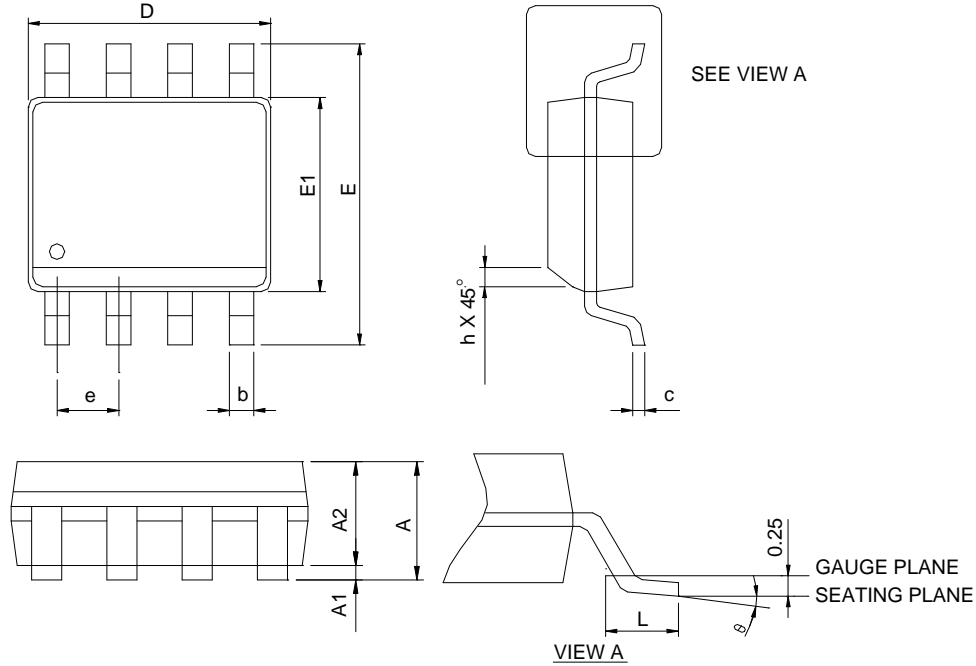
Figure 2

Recommended Minimum Footprint



Package Information

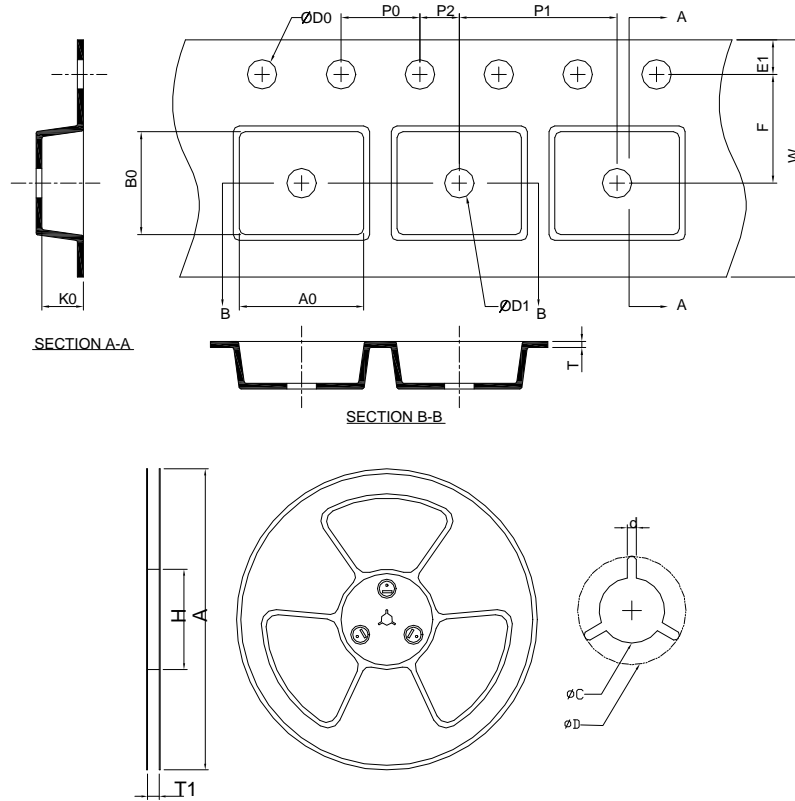
SOP-8



SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

- Note: 1. Follow JEDEC MS-012 AA.
 2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
 3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



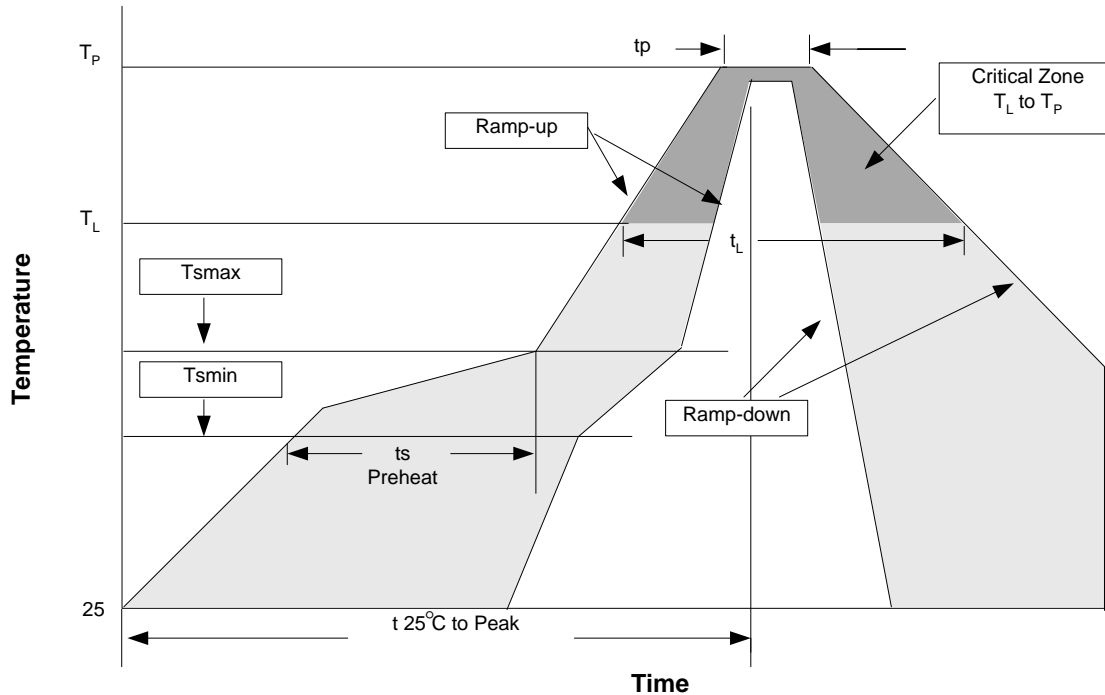
Application	A	H	T1	C	d	D	W	E1	F
SOP-8	330.0 ±0.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0 ±0.30	1.75 ±0.10	5.5 ±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0 ±0.10	8.0 ±0.10	2.0 ±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40 ±0.20	5.20 ±0.20	2.10 ±0.20

(mm)

Devices Per Unit

Package Type	Unit	Quantity
SOP-8	Tape & Reel	2500

Reflow Condition (IR/Convection or VPR Reflow)



Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 sec
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B, A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1 _{tr} > 100mA

Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T _L to T _P)	3°C/second max.	3°C/second max.
Preheat		
- Temperature Min (T _{min})	100°C	150°C
- Temperature Max (T _{max})	150°C	200°C
- Time (min to max) (t _s)	60-120 seconds	60-180 seconds
Time maintained above:		
- Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak/Classification Temperature (T _p)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (t _p)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Note: All temperatures refer to topside of the package. Measured on the body surface.

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm ³ <350	Volume mm ³ ≥350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm ³ <350	Volume mm ³ 350-2000	Volume mm ³ >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*

* Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.

Customer Service

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