AN1116
APPLICATION NOTE

Changing from the ST95P08 to the M95080 in Your Application Using a Simple Software Recognition Method

The members of the new M95xxx, SPI serial-bus, EEPROM chips offer features that were not available with the ST95xxx family. Table 1 summarizes the main differences between the new 8 Kbit M95080 memory, and the ST95P08, by way of example.

This document is aimed at helping the designer to convert designs from using the ST95P08 to using the M95080. It concludes by indicating a simple algorithm that can be used in the application software to detect which of the two devices is being used.

Table 1. Differences and Improvements (Functional and Electrical) Between the ST95P08 and the M95080

	ST95P08	M95080
Memory capacity	8 Kbit	8 Kbit
Supply range (V_{CC})	3 V to 5.5 V	4.5 V to 5.5 V 2.5 V to 5.5 V 1.8 V to 3.6 V
Clock frequency (f_{MAX})	2 MHz	5 MHz
Temperature range	-40 to 85 °C	-40 to 85 °C (6) -20to 85 °C (5) -40 to 125 °C (3)
Page size	16 Bytes	32 Bytes
Number of address bytes	1	2
Block protection (BP1,BP0)	yes	yes
I_{CC} stand-by	50 µA at 5.5 V 10 µA at 3 V	10 µA at 5 V 2 µA at 2.5 V 1 µA at 1.8 V
I_{CC} operating	2 mA at 2 MHz	4 mA at 2 or 5 MHz at 5 V 2 mA at 2 MHz at 5 V 2 mA at 1 MHz at 1.8 V
$\overline{W}$ feature (write control)	Hardware write protection of the entire memory array.	Hardware write protection of the BPn protected area, and of the status register
Status register format	1 1 1 1 BP1 BP0 WEL WIP	SRWD XXX BP1 BP0 WEL WIP
Write cycle time (max.)	10 ms	10 ms
Instruction format	0 0 0 X_2 X_1 I_2 I_1 I_0	0 0 0 0 0 I_2 I_1 I_0

The $\overline{W}$ feature

Both the ST95P08 and M95080 support the software protection mode using the BP1 and BP0 status register bits. However, their behaviors are different with the use of the $\overline{W}$ pin.

On the ST95P08, the $\overline{W}$ pin controls the write access to the memory array:

- $\overline{W}$=1: write enabled throughout the entire memory array that is not software write-protected
- $\overline{W}$=0: write disabled throughout the entire memory array

On the M95080, the $\overline{W}$ pin provides hardware write protection of the status register (SR), except for the WIP and WEL bits. When bit 7 (SRWD, the Status Register Write Disable bit) of the status register is '0' (the initial delivery state), it is possible to write to the status register once the WEL (Write Enable Latch) has been set, and regardless of the status of pin $\overline{W}$ (high or low).

Once bit 7 (SRWD) of the status register has been set to '1', the possibility to rewrite the SR depends on the logical level present at pin $\overline{W}$:

– If $\overline{W}$ pin is high, it is possible to write to the status register after setting the WEL (Write Enable Latch).

– If $\overline{W}$ pin is low, any attempt to modify the status register is ignored by the device, even if the WEL is set. Consequently, all the data bytes in the EEPROM area that are protected by the BPn bits of the status register, are also hardware protected against data corruption, and become a Read Only EEPROM area from the microcontroller. This mode is called the Hardware Protected Mode (HPM).

It is possible to enter the Hardware Protected Mode (HPM) by setting the SRWD bit after pulling down the $\overline{W}$ pin, or by pulling down the $\overline{W}$ pin after setting SRWD bit.

The only way to return from the Hardware Protected Mode, once entered, is to pull the $\overline{W}$ pin high.

If the $\overline{W}$ pin is permanently tied high, the Hardware Protected Mode cannot be activated, and the Memory only allows the user to software-protect a part of the memory using the BPn bits of the status register. The protection features of the device are summarized in Table 2.

Table 2. Write Protection Control on the M95080

$\overline{W}$	SRWD Bit	Mode	Status Register	Data Bytes	
				Protected Area	Unprotected Area
1	0	Software Protected (SPM)	Writeable after setting WEL	Software write protected by the BPn of the status register	Writeable after setting the WEL
0	0				
1	1				
0	1	Hardware Protected (HPM)	Hardware write protected	Hardware write protected	Writeable after setting the WEL

Instruction code

Using the two standard address bytes, M95080 instructions take the following format:

0 0 0 0 0 I_2 I_1 I_0

(where I_2, I_1 and I_0 are the instruction bits).

The ST95P08, on the other hand, does not support the standard two byte addressing mode for high densities. Instead, the A8 and A9 address bits are placed beside the instruction bits, according to the following format:

0 0 0 X_2 X_1 I_2 I_1 I_0

(where X_2 and X_1 are respectively A9 and A8 for Read and Write operations, and are Don't Care bits for others).

SOFTWARE RECOGNITION ALGORITHM

This last difference can be used by the application software to differentiate between the two types of memory device. (For a further summary, please see the comparison of the instruction formats of the two devices, in Table 3).

The WREN instruction is used, prior to any write attempt to the memory, to set an internal logical bit of the status register which has to be set to 1 to try a write access to the memory.

As described above in the "instruction format" section, 0001 1101 is a valid WREN instruction code for the ST95P08, and is not a valid WREN instruction for the M95080.

The following algorithm is short, and easy to insert in the MCU code. It is also safe to use, inasmuch that it does not attempt to write to any non volatile bits.

– Master sends the WREN instruction "0001 1110" to the memory (note that b3 and b4 are "1").
– Master sends the RDSR instruction "0000 0101" to the memory (note that b3 and b4 are "0" to avoid the High-Z state on the Q-bus during WEL bit read) and stores the value of the WEL bit in a variable that we will refer to as WEL1.
– Master sends the WRDI instruction "0001 1100" to the memory (note that b3 and b4 are "1").
– Master sends the RDSR instruction "0000 0101" to the memory (again, b3 and b4 are "0" to avoid the High-Z state on the Q-bus during WEL bit read) and stores the value of the WEL bit in a variable that we will refer to as WEL2.
– If (WEL1,WEL2)= (1,0)

  then the EEPROM device is a ST95P08

  else the EEPROM device is an M95080

Table 3. Differences Between the ST95P08 and the M95080 Instruction Formats

Instruction	Description	Instruction Format	
		ST95P08	M95080
WREN	Set Write Enable Latch	000X X110	0000 0110
WRDI	Reset Write Enable Latch	000X X100	0000 0100
RDSR	Read Status Register	000X X101	0000 0101
WRSR	Write Status Register	000X X001	0000 0001
READ	Read Data from Memory Array	000A A011	0000 0011
WRITE	Write Data to Memory Array	000A A010	0000 0010

Notes: 1. A = 1 indicates that the upper page is selected; A = 0 indicates that the lower page is selected
2. X = Don't Care

If you have any questions or suggestions concerning the matters raised in this document, please send them to the following electronic mail addresses:

apps.eeprom@st.com (for application support)

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Please remember to include your name, company, location, telephone number and fax number.