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A Balanced Summing Amplifier

The summing amplifier circuit shown in Figure 1 represents an excellent virtual ground summing amplifier using a balanced differential design that includes extremely low noise and wide bandwidth as featured by the SSM-2015. Any size audio mixing system can benefit from balanced virtual node mixing (summing). The low cost and exceptional performance of this design can be incorporated in any system with balanced or mixed balanced and unbalanced input sources.

IC_2, the PMI OP-41, serves as a DC servo-amplifier that is referenced to signal ground. The circuit functions as an integrator with a long time constant that retains the integrity of low frequency audio signals down to 5Hz, and keeps $e_{OUT} = 0V_{DC}$, ($\pm 10mV_{DC}$). The OP-41 is a FET input amplifier, with low input offset voltage (V_{OS}) and high input impedance. Although many low performance JFET/CMOS operational amplifiers can be employed, the summing output V_{DC} is a function of the servo's input offset voltage and its temperature coefficient ($\Delta V_{OS}/\Delta T$), which must be kept low for direct coupled summing applications.

In this design, the following facts predominate: $e_S = 0$, and $i_S = 0$. e_{IN} is the algebraic sum of the input(s) e_{IN1}, e_{IN2}, e_{IN3}, e_{INn} and etc. $e_{OUT} = [e_{IN1}(R_F/R_{IN1}) + e_{IN2}(R_F/R_{IN2}) + e_{IN3}(R_F/R_{IN3}) + e_{INn}(R_F/R_{INn})]$, etc. The input impedance therefore equals R_{IN1}, R_{IN2}, R_{IN3}, R_{INn}, etc. The overall gain of the circuit is set by R_F, and the gain of the individual channels can be adjusted independently by the values of R_{IN1}, R_{IN2}, R_{IN3}, R_{INn}, etc.

For individual source input(s), gain is $A_O = R_F/R_{IN}$.

The circuit configuration produces linear signal mixing at the summing nodes (IC_1 pins 10,11), whereas $e_S = 0$; therefore, no interaction occurs between the source inputs. Owing to the fact that the SSM-2015 is a bipolar transistor device, the noise is low ($1.3nV/\sqrt{Hz}$). The commonly used values of 10kΩ for R_F and R_{IN} are optimal for both minimum noise and previous stage loading, eliminating the need for buffer amplifiers and their noise contribution.

The input common-mode rejection for the SSM-2015 is typically 100dB as a result of true differential input topology. The differential thermal noise and DC offset drift is nearly eliminated by the common substrate construction employed. To exploit the high CMR of the SSM-2015, all signal resistors should be matched resistor networks or should employ 0.5% or better resistor tolerances.

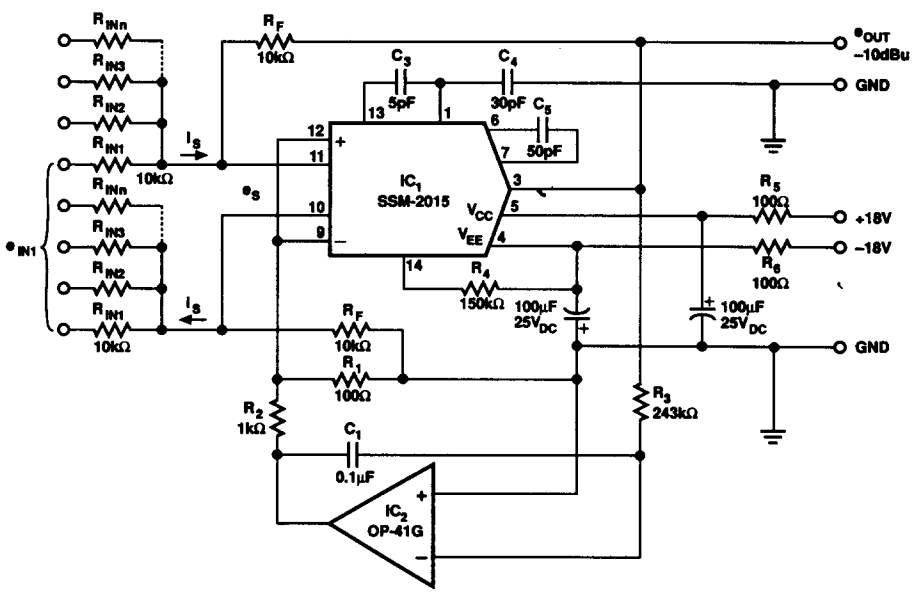

FIGURE 1

The output circuit topology of the SSM-2015 is complementary bipolar producing overall performance of 6V/μs slew rate, and is able to drive a 2kΩ unbalanced load. The circuit described can be directly coupled, eliminating coloration and distortion associated with coupling capacitors. The circuitry following this amplifier could be AC (capacitor) coupled if the DC servo IC_2 offset voltage of $\pm 10mV_{DC}$ is objectionable.

Audio performance challenges the best test equipment that might be used to measure high performance analog designs. For example: worst case THD for this circuit measures less than 0.008%, and IMD less than 0.02% over a band-width of 10Hz to 20kHz. See Table 1 for more performance details.

TABLE 1: Circuit Performance Specifications

Frequency Response (dB 20Hz to 20kHz)	±0.02
S/N Ratio @ +23dBu	103dB
TMD + Noise (@ +23dBu 20Hz to 20kHz)	0.008%
IMD (@ +23dBu SMPTE 60Hz & 4kHz, 4:1)	0.015%
CMRR (60Hz)	100dB
Slew Rate	6V/μs
Output Voltage (2kΩ load)	+23dBu or $11V_{RMS}$