
HA13631T

CD-ROM Combo Driver

HITACHI

ADE-207-320 (Z)
1st Edition
Feb. 2000

Description

The HA13631T is combination of Spindle, Focus, Tracking, Slide, Tray designed for CD-ROM and have following functions and features.

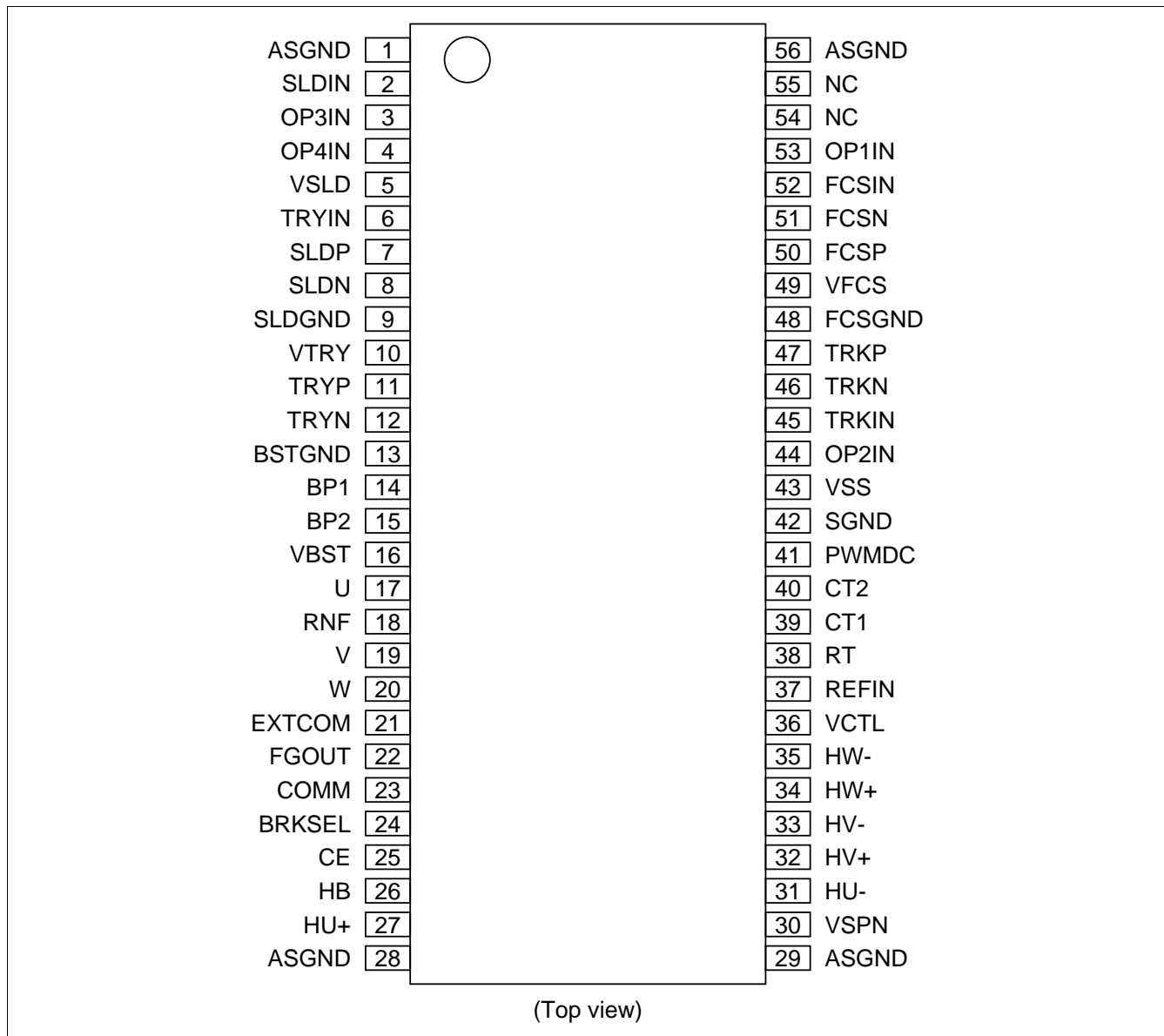
Functions

- 1.5 A spindle driver
- 0.75 A focus driver
- 0.75 A tracking driver
- 1.0 A slide driver
- 0.75 A tray driver
- Over temperature shut down (OTSD)

Features

- Corresponds to both of sensor motor and sensorless motor
- All direct PWM drive
- Low on resistance
- Low power dissipation
- Small thin surface mount package

Pin Arrangement



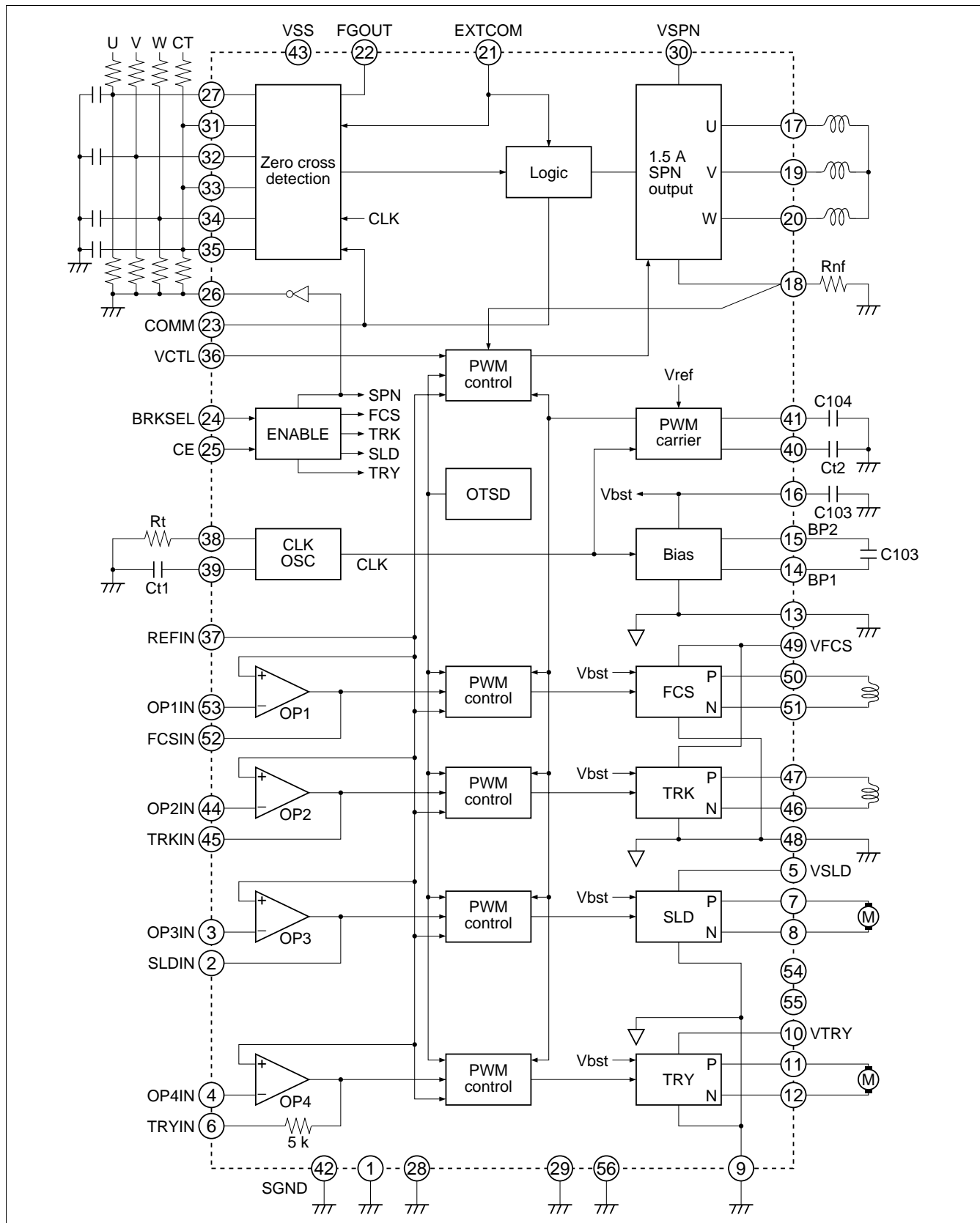
Pin Description

Pin No.	Pin Name	Function
1	ASGND	Actuator small signal GND
2	SLDIN	SLD driver control input
3	OP3IN	Inverted input of OP amp. 3 for SLD driver control
4	OP4IN	Inverted input of OP amp. 4 for TRY driver control
5	VSLD	SLD driver power supply
6	TRYIN	TRY driver control input
7	SLDP	SLD driver P output
8	SLDN	SLD driver N output
9	SLDGND	SLD and TRY driver GND
10	VTRY	TRY driver power supply
11	TRYP	TRY driver P output
12	TRYN	TRY driver N output
13	BSTGND	Booster GND
14	BP1	Booster pumping capacitor connection
15	BP2	Booster pumping capacitor connection
16	VBST	Booster output pin. This circuit generates a voltage about two times of the VSPN pin.
17	U	U phase output
18	RNF	SPN driver current detection
19	V	V phase output
20	W	W phase output
21	EXTCOM	COMM signal on/off control and FGOUT switching. (Refer to the Timing Chart)
22	FGOUT	FG output (Refer to the Timing Chart) open drain
23	COMM	Start-up clock input pin for sensorless (Refer to the Timing Chart)
24	BRKSEL	To select the brake mode (Refer to the Truth Table)
25	CE	Chip enable (Refer to the Truth Table)
26	HB	Hall bias switch
27	HU+	U-phase Hall +input, and U-phase B-EMF connection pin for sensorless
28	ASGND	Actuator small signal GND
29	ASGND	Actuator small signal GND
30	VSPN	SPN driver power supply
31	HU-	U-phase Hall -input, and center tap connection pin for sensorless
32	HV+	V-phase Hall +input, and V-phase B-EMF connection pin for sensorless
33	HV-	V-phase Hall -input, and center tap connection pin for sensorless

Pin Description (cont)

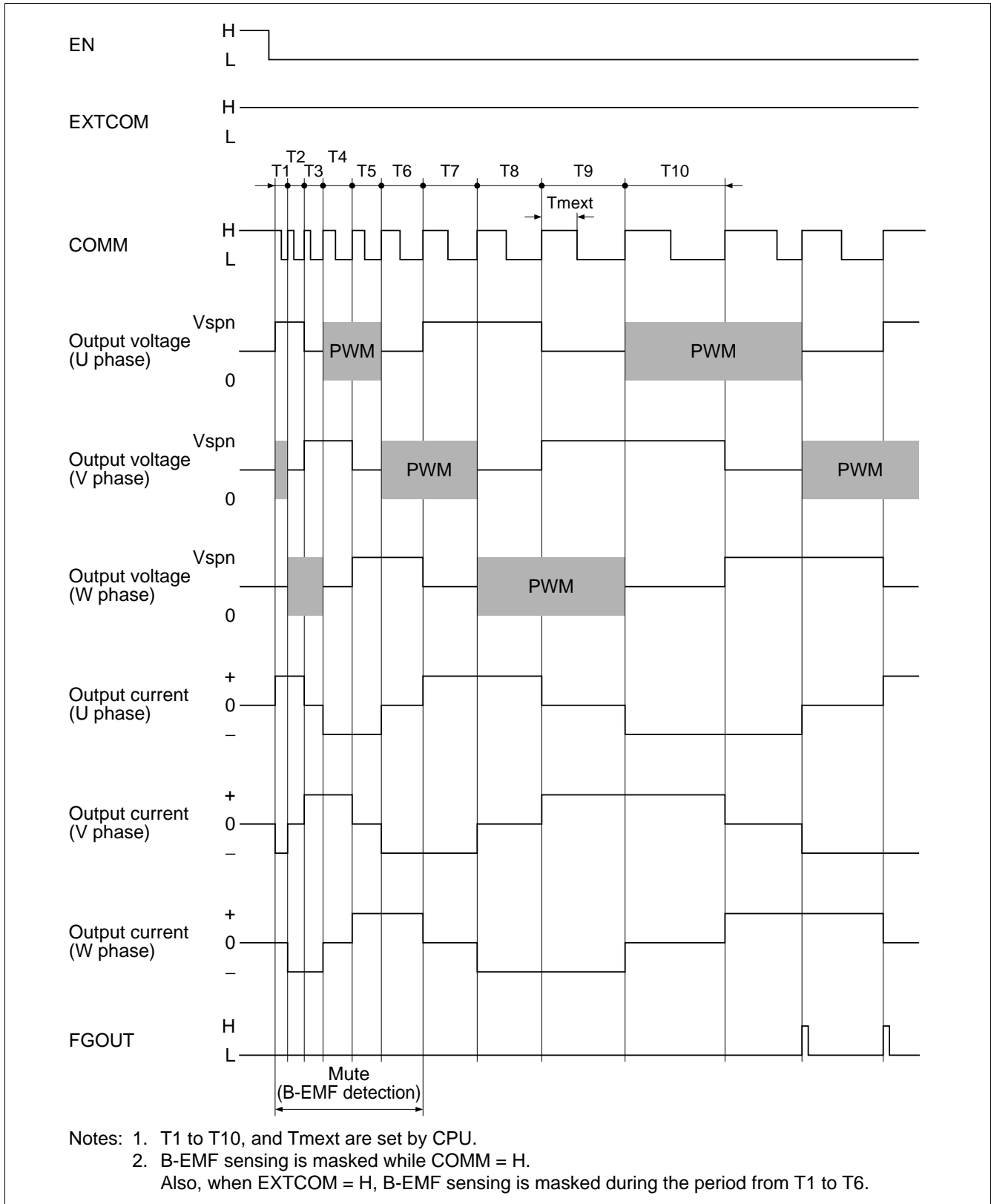
Pin No.	Pin Name	Function
34	HW+	W-phase Hall +input, and W-phase B-EMF connection pin for sensorless
35	HW-	W-phase Hall -input, and center tap connection pin for sensorless
36	VCTL	SPN driver control input
37	REFIN	Reference voltage for control inputs. Common to all drivers.
38	RT	Reference voltage. The IC's internal reference current is determined by this voltage and the external resistor Rt.
39	CT1	Time constant for clock oscillation. The oscillator frequency is determined by the external capacitor and resistor Ct1 and Rt.
40	CT2	Time constant for PWM carrier. The amplitude is determined by the value of the external capacitor Ct1.
41	PWMDC	Phase compensation connection pin for matching PWM carrier DC level with REFIN
42	SGND	SPN small signal GND
43	VSS	Control block power supply. 5 V
44	OP2IN	Inverted input of OP amp. 2 for TRK driver control
45	TRKIN	TRK driver control input
46	TRKN	TRK driver N output
47	TRKP	TRK driver P output
48	FCSGND	FCS and TRK driver GND
49	VFCS	FCS driver power supply
50	FCSP	FCS driver P output
51	FCSN	FCS driver N output
52	FCSN	FCS driver control input
53	OP1IN	Inverted input of OP amp. 1 for FCS driver control
54	NC	No connection
55	NC	No connection
56	ASGND	Actuator small signal GND

Block Diagram

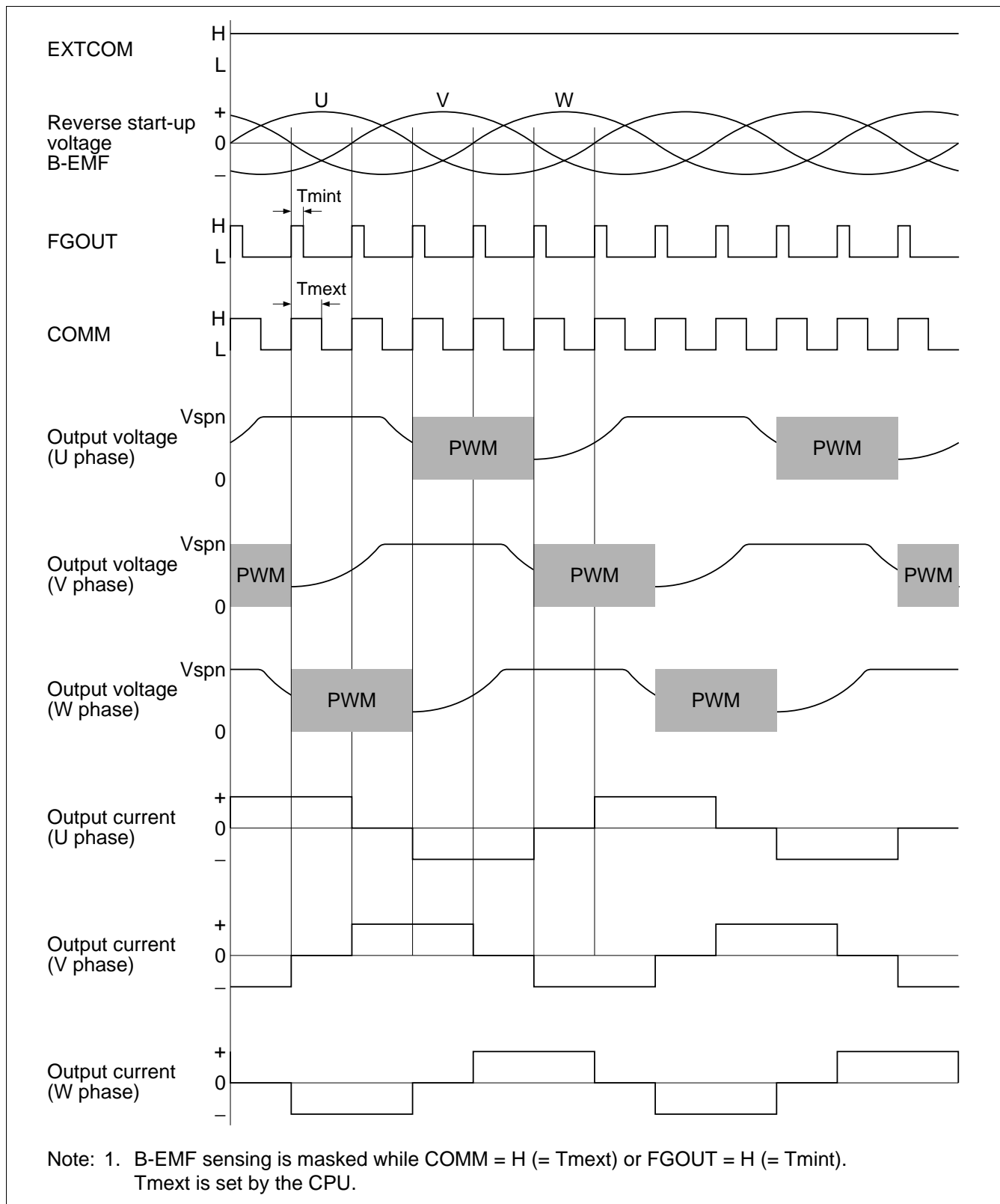


Timing Chart

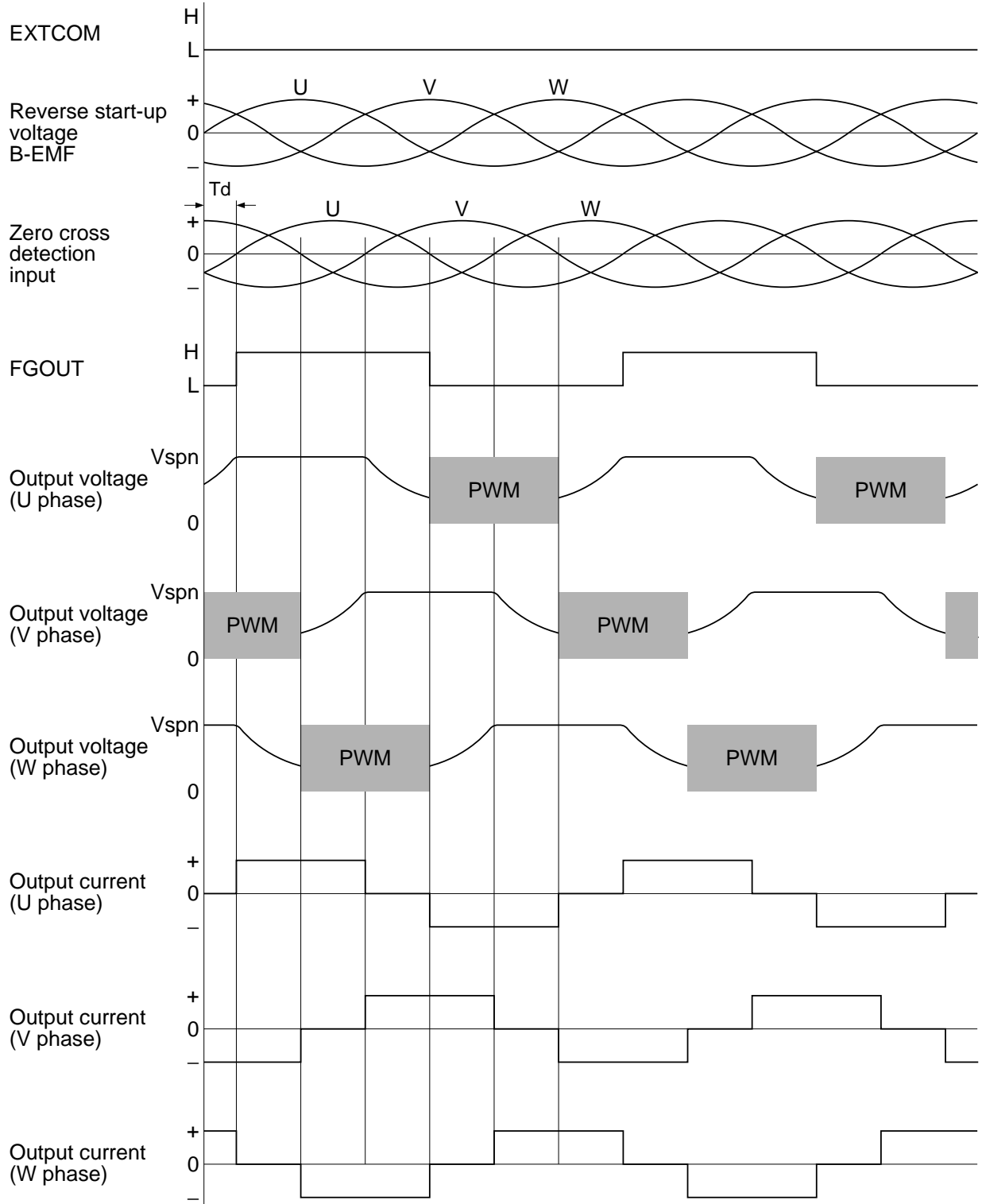
1. Start-up



2. Acceleration



3. Running



- Notes:
1. Delay time T_d is determined by C105 to C107, and R109 to R116. Refer to the section of External Components.
 2. B-EMF sensing is masked while $FGOUT = H$ ($= T_{mint}$). The T_{mint} time is set internally. Refer to the Electrical Characteristics.

Truth Table

Table 1 CE and BRKSEL

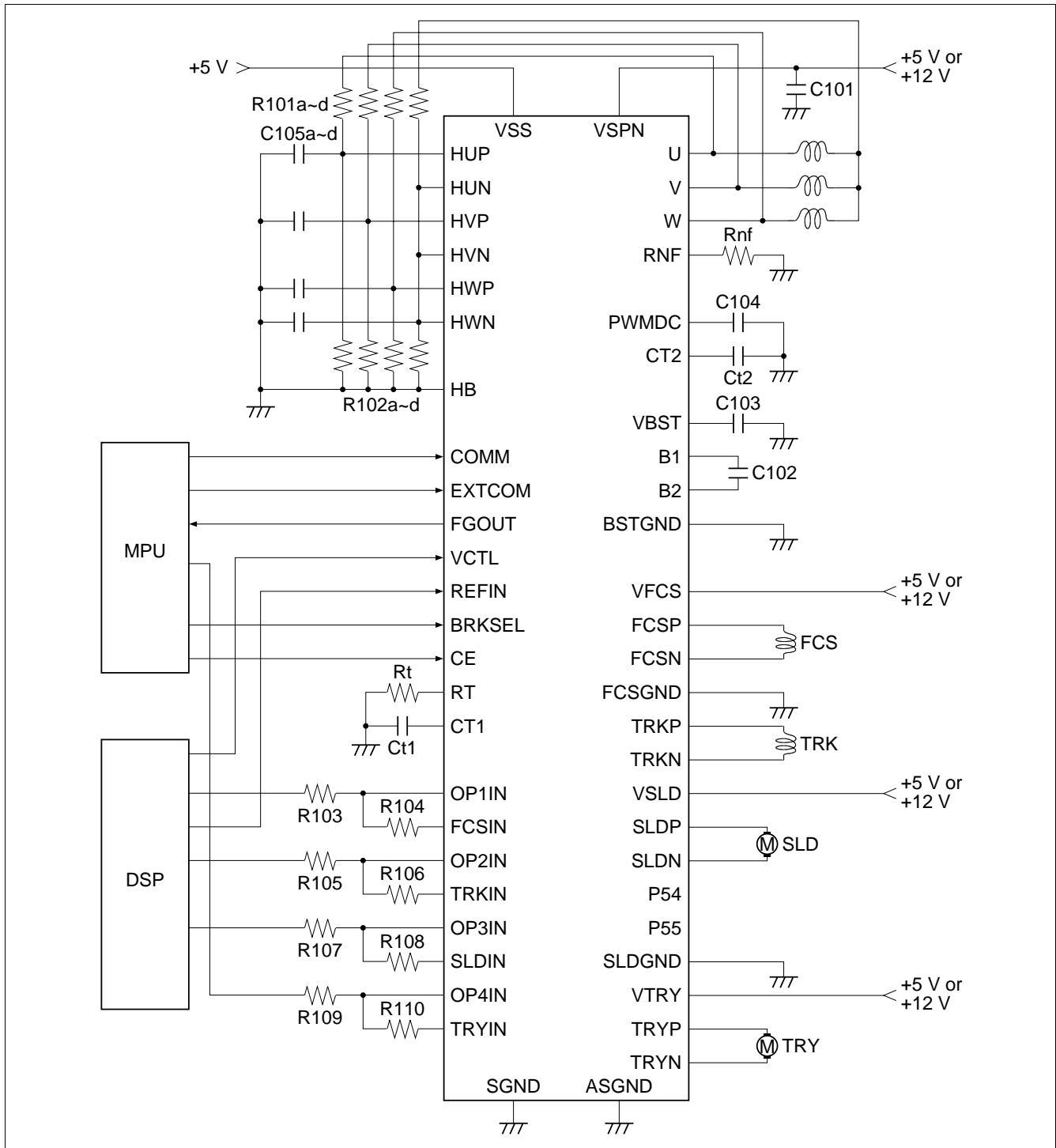
CE	BRKSEL	SPN Driver	FCS Driver	TRK Driver	SLD Driver	TRY Driver
L	L	Z	Z	Z	Z	Z
	H	Enable *2	Enable	Enable	Z	Enable
H	L	Enable *3	Enable	Enable	Enable	Z
	H	Enable *2	Enable	Enable	Enable	Z

Notes: 1. Z: Hi impedance
 2. Short brake mode
 3. Reverse brake mode

Table 2 EXTCOM and COMM

EXTCOM	COMM	T1~T6 Mask	T7~ Mask	FGOUT (@P = 12)	Logic
L	L	OFF	Internal	6 cycle/rotation	Corresponds to sensor
	H	OFF	Internal		Corresponds to sensorless
H	L	ON	Internal	36 pulse/rotation	
	H	ON	External		

Application



External Components

Parts No.	Reccomended Value	Reccomended Range	Purpose	Note
R101a~d	2.4 kΩ	≤ 22 kΩ	Filter resistor and atenuation for B-EMF	1
R102a~d	7.5 kΩ	≤ 22 kΩ	Filter resistor and atenuation for B-EMF	1
R103, R104	—	≤ 220 kΩ	for FCS driver gain setting	
R105, R106	—	≤ 220 kΩ	for TRK driver gain setting	
R107, R108	—	≤ 220 kΩ	for SLD driver gain setting	
R109, R110	—	≤ 220 kΩ	for TRY driver gain setting	5
Rnf	0.25 Ω	≥ 0.25 Ω	SPN driver current detection resistor	2
Rt	6.8 kΩ	≥ 5 kΩ	Reference current setting	
C101	—	≥ 0.1 μF	for Power supply by passing	
C102	0.1 μF	—	for Booster pumping	
C103	0.47 μF	—	for Booster output smoothing	
C104	2200 pF	—	for PWM carrier oscillation DC level adjustment	
C105a~d	0.1 μF	—	for B-EMF filter	1
Ct1	100 pF	—	Time constant for CLK oscillation	3, 4
Ct2	400 pF	—	PWM carrier generation time constant	3, 4

Notes: 1. The values of R101a~d, R102a~d, and C105a~d are determined by the following equation.

Where, N_{omax} : Maximum rotation speed (rpm)

P : Number of spindle motor poles (Total number of S poles and N poles)

$$\frac{R101}{R102} \geq \frac{1}{4} \quad (\text{at } V_{spn} = 5 \text{ V})$$

$$C105x = \frac{11}{N_{omax} P} \left(\frac{1}{R101x} + \frac{1}{R102x} \right)$$

2. The output current maximum value $I_{ospnmax}$ of SPN driver is controlled according to the following equation. However, V_{spncl} is the current limiter reference voltage. (See the electrical characteristics)

$$I_{ospnmax} = \frac{V_{spncl}}{R_{nf}}$$

3. The CLK oscillation frequency f_{clk} and $Rt1 \cdot Ct1$ are related by the following equation.

$$f_{clk} = \frac{V_{rt}}{2 Ct1 Rt (V_{ct1h} - V_{ct1l})}$$

Where, V_{rt} : RT pin voltage (See the electrical characteristics)

V_{ct1h} : CT1 pin high voltage (See the electrical characteristics)

V_{ct1l} : CT1 pin low voltage (See the electrical characteristics)

4. The PWM carrier frequency f_{pwm} and the amplitude A_{pwm} are determined by the following equation.

$$f_{pwm} = \frac{V_{rt}}{8 C_{t1} R_t (V_{ct1h} - V_{ct1l})}$$

$$A_{pwm} = \frac{4 C_{t1}}{C_{t2}} (V_{ct1h} - V_{ct1l})$$

However, $C_{t2} = 4 C_{t1}$

5. As $5\text{ k}\Omega$ appears as an internal resistance at TRYIN (pin 6), caution is required when marking the gain setting.

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit	Note
Control block supply voltage	Vss	7	V	1
SPN supply voltage	Vspn	7	V	1
FCS & TRK supply voltage	Vfcs	9.5	V	1
SLD supply voltage	Vsld	7	V	1
TRY supply voltage	Vtry	9.5	V	1
Input voltage	Vin	0 to Vss	V	2
SPN output current	Iospn	1.5 (2.5)	A	3
FCS output current	Iofcs	0.75 (1.5)	A	3
TRK output current	Iotrk	0.75 (1.5)	A	3
SLD output current	Iosld	1.0 (1.5)	A	3
TRY output current	Iotry	0.75 (1.5)	A	3
Power dissipation	Pt	2.5	W	4
Junction temperature	Tj	150	°C	1
Storage temperature range	Tstg	-55 to +125	°C	

Note: 1. Operating range is shown below.

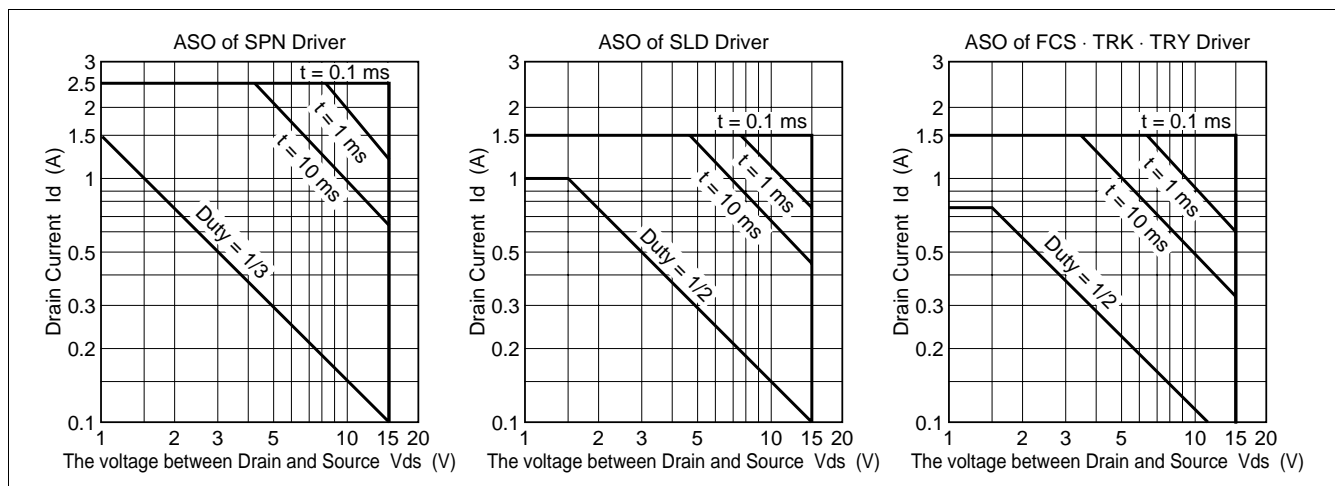
Vss = 4.5 to 5.5 V, Vspn = 4.25 to 5.75 V, Vfcs = 4.25 to 8.5 V, Vsld = 4.25 to 5.75 V, Vtry = 4.25 to 8.5 V, Tjopr = -20 to +135°C

When operating with Vfcs > Vss, it is necessary to set Vtry = Vfcs. Also, settings must be made that satisfy the following condition:

$$Vtry + Vss - Vsld \leq 8.5 \text{ V}$$

2. Applied to analog and logic input.

3. Values in parentheses are peak values. ASO (Area of Safety Operation) is shown below.



4. Thermal resistance is shown below.

$$\theta_{j-tab} \leq 6^\circ\text{C/W} \text{ (back side tab soldering area is 70\% or more)}$$

$$\theta_{j-a1} \leq 30^\circ\text{C/W} \text{ (mounted on 4 layer glass-epoxy board, back side tab soldering area is 70\% or more)}$$

Electrical Characteristics

($T_a = 25^\circ\text{C}$, $V_{SS} = 5\text{ V}$, $V_{SPN} = 12\text{ V}$, $V_{FCS} = 5\text{ V}$, $V_{SLD} = 12\text{ V}$)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Applicable Pins	Note	
Quiescent current	I _{SS0}	—	0.2	0.5	mA	CE = L	VSS		
	I _{SPN0}	—	0.1	0.2	mA		VSPN		
	I _{FCS0}	—	—	0.1	mA		VFCS		
	I _{SLD0}	—	—	0.1	mA		VSLD		
	I _{TRY0}	—	—	0.1	mA		VTRY		
	I _{SS1}	—	25	35	mA	CE = H	VSS		
	I _{SPN1}	—	—	1.0	mA	All load open	VSPN		
	I _{FCS1}	—	—	1.0	mA		VFCS		
	I _{SLD1}	—	—	1.0	mA		VSLD		
	I _{TRY1}	—	4.0	6.0	mA		VTRY		
Logic input	Input current	I _{IN}	—	—	±10	μA	V _{IN} = 0 to V _{SS}	EXTCOM,	
	Low level voltage	V _{IL}	—	—	0.8	V		COMM,	
	High level voltage	V _{IH}	2.0	—	—	V		BRKSEL, CE	
Logic output 1	Low level voltage	V _{OL}	—	0.2	0.4	V	I _O = 1 mA	FGOUT	
	Leakage current	I _{CER1}	—	—	±10	μA	V _{CE} = 5.5 V		
Logic output 2	Low level voltage	V _{OL}	—	0.3	0.6	V	I _O = 15 mA	HB	
	Leakage current	I _{CER1}	—	1.2	1.5	μA	V _{CE} = 5.5 V		
SPN driver	Output on resistance	R _{ONSPN}	—	1.2	1.5	Ω	I _O = 1.0 A	U, V, W	1
	Leakage current	I _{OFFSPN}	—	—	±100	μA	V _{SPN} = 15 V		
	Slew rate	SR _{SPN}	—	60	—	V/μs	Load open		5
	Current limiter voltage	V _{SPNCL}	—	0.25	±10%	V	R _{NF} = 0.25 Ω	RNF	
FCS/ TRK driver	Output on resistance	R _{ONFCS}	—	3.0	3.75	Ω	I _O = 0.5 A	FCSP/N, TRKP/N	1
	Leakage current	I _{OFFFCS}	—	—	±100	μA	V _{FCS} = 15 V		
	Slew rate	SR _{FCS}	—	60	—	V/μs	Load open		5
SLD driver	Output on resistance	R _{ONSLD}	—	2.0	2.5	Ω	I _O = 1.0 A	SLDP/N	1
	Leakage current	I _{OFFSLD}	—	—	±100	μA	V _{SLD} = 15 V		
	Slew rate	SR _{SLD}	—	60	—	V/μs	Load open		5

Electrical Characteristics

(Ta = 25°C, V_{SS} = 5 V, V_{spn} = 12 V, V_{fcs} = 5 V, V_{sld} = 12 V) (cont)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Applicable Pins	Note
TRY driver	Output on resistance	Rontry	—	3.0	3.75	Ω	I _o = 0.5 A	TRYP/N	1
	Leakage current	Iofftry	—	—	±100	μA	V _{try} = 15 V		
	Slew rate	SRtry	—	125	—	V/μs	Load open		5
CLK OSC	RT voltage	V _{rt}	—	1.37	±5%	V		RT	
	CT1 charge current	I _{ct1p}	—	180	±10%	μA	R _t = 6.8 kΩ	CT1	
	CT1 discharge current	I _{ct1n}	—	-180	±10%	μA	R _t = 6.8 kΩ		
	CT1 high voltage	V _{ct1h}	—	2.7	±0.1	V			
	CT1 low voltage	V _{ct1l}	—	1.47	±0.1	V			
	CLK oscillation frequency	f _{clk}	—	460	±10%	kHz	C _{t1} = 100 pF		
Bias	Drive frequency	f _{bst}	—	f _{clk} /2	—	kHz		BP1	
	Output voltage	V _{bst}	16.0	16.5	—	V	V _{spn} = 12 V	VBST	
			9.0	9.5	—	V	V _{spn} = 5 V		
PWM carrier	PWM frequency	f _{pwm}	—	f _{clk} /4	—	kHz		CT2	
	CT2 charge current	I _{ct2p}	—	180	±10%	μA	R _t = 6.8 kΩ		
	CT2 discharge current	I _{ct2n}	—	-180	±10%	μA	R _t = 6.8 kΩ		
	DC feedback resistance	R _{dc}	—	20	±20%	kΩ		PWMDC	
	Offset voltage	V _{ospwm}	—	—	±30	mV			
Zero cross detection	Common mode input voltage range	V _{czd}	0	—	4.0	V		HU+/-, HV+/-, HW+/-	
	Input voltage range	V _{inzd}	50	—	—	mV _{pp}			
	Hysteresis	V _{hyszd}	11	16	21	mV _{pp}			
	FGOUT pulse width	T _{mint}	—	64/ f _{clk}	±4/ f _{clk}	μs		FGOUT	
SPN control	Input current	I _{ctl}	—	—	±3.0	μA	V _{ctl} = 0.5 to 4.5 V	VCTL	
	Dead zone voltage	V _{dzctl}	±50	—	±200	mV			2
	REFIN voltage range	V _{ref}	1.0	—	2.65	V		REFIN	4
	Control gain	D _{spn}	119	139	159	%/V	C _{t2} = 680 pF, C _{t1} = 100 pF	U, V, W	2

Electrical Characteristics

($T_a = 25^\circ\text{C}$, $V_{SS} = 5\text{ V}$, $V_{SPN} = 12\text{ V}$, $V_{FCS} = 5\text{ V}$, $V_{SLD} = 12\text{ V}$) (cont)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Applicable Pins	Note
OP1~ OP4	Input current	I _{inop}	—	—	±0.1	μA	V _{in} = 0 to V _{SS}	OP1~4IN	
	Offset voltage	V _{osop}	—	—	±60	mV		FCSIN,	
	Open loop gain	G _{volop}	—	64	—	dB	f = 1kHz	TRKIN,	5
	Gain bandwidth	B _{op}	—	1.6	—	MHz		SLDIN, TRYIN	5
OP1~ OP3	Output low voltage	V _{oopl}	—	—	0.5	V	I _o = -0.2 mA	FCSIN, TRKIN, SLDIN	
	Output high voltage	V _{ooph}	V _{SS} -1.0	—	—	V	I _o = 0.2 mA		
OP4	Output low voltage	V _{oopl}	—	—	0.5	V	I _o = -0.03 mA	TRYIN	
	Output high voltage	V _{ooph}	V _{SS} -1.7	—	—	V	I _o = 0.03 mA		
FCS/ TRK/ SLD/ TRY control	Quiescent offset duty	D _{qfcs}	—	—	±2	%	FCS/TRK/SLD/ TRYIN = REFIN	FCSP/N, TRKP/N, SLDP/N, TRYP/N	3
	Control gain	D _{fcs}	63	68	73	%/V	C _{t2} = 680 pF, C _{t1} = 100 pF		
OTSD	Operating temperature	T _{sd}	135	180	—	°C			5
	Hysteresis	Th _{ys}	—	80	—	°C			

- Note: 1. Specified by sum of the upper and lower saturation voltages.
 2. See figure 1. Where,

$$D_{spn} = \frac{\Delta D}{\Delta V_{ctl}}$$

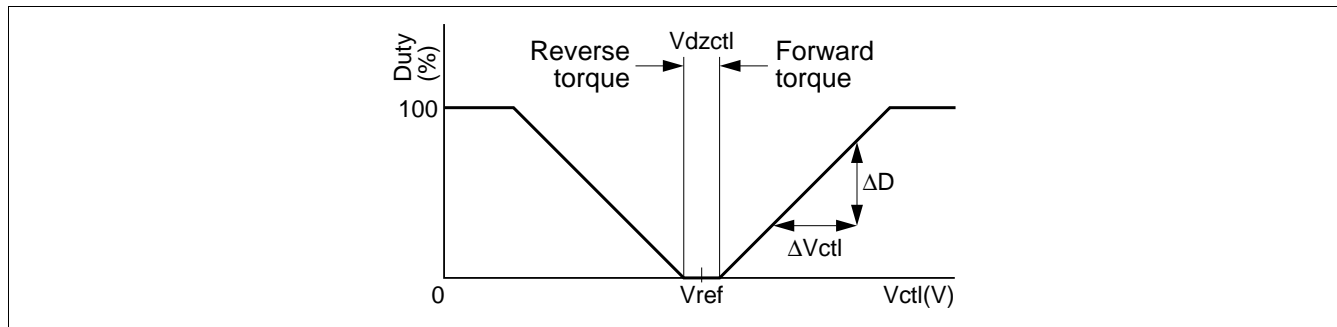


Figure 1

3. See figure 2. Where, x = fcs, trk, sld, try.

$$D_x = \frac{\Delta D}{\Delta V_{xin}}$$

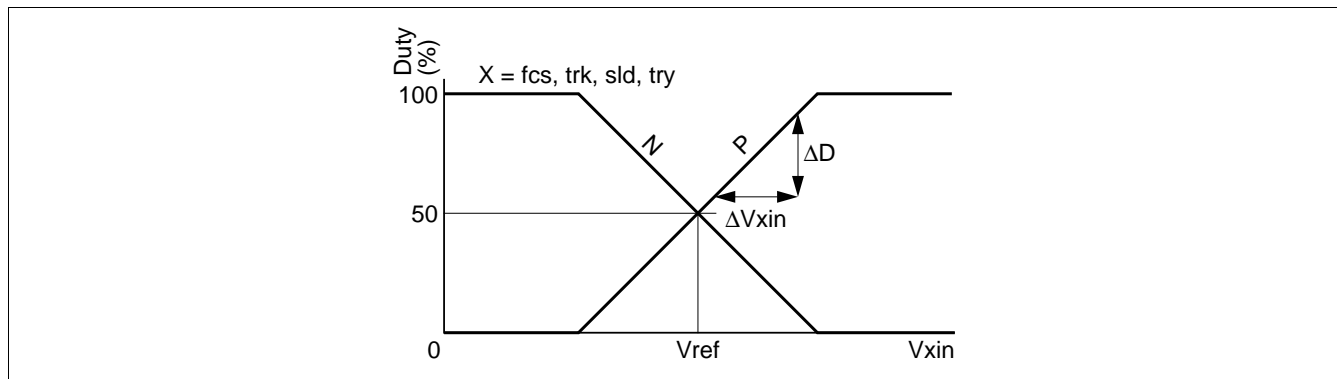
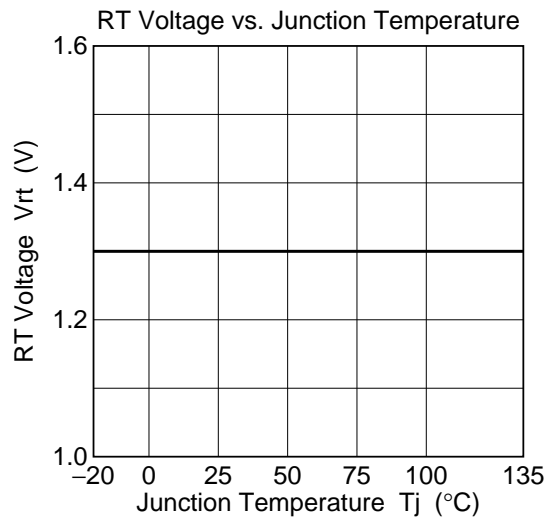
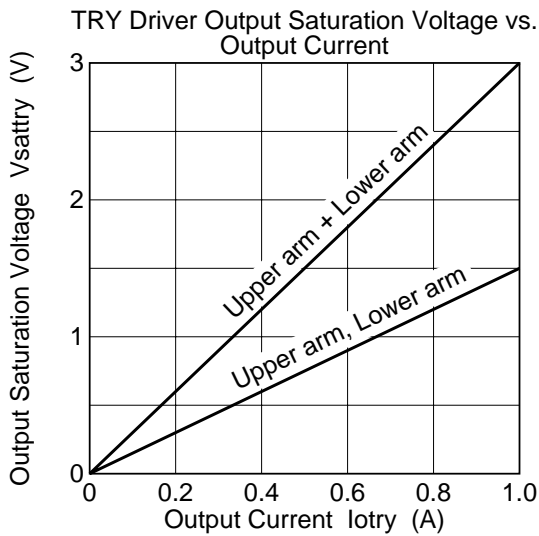
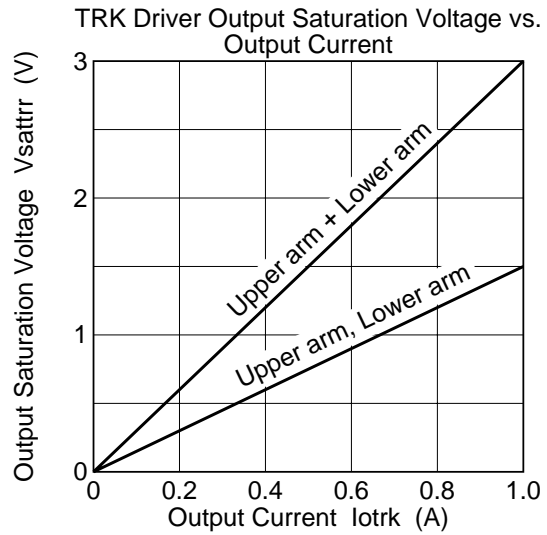
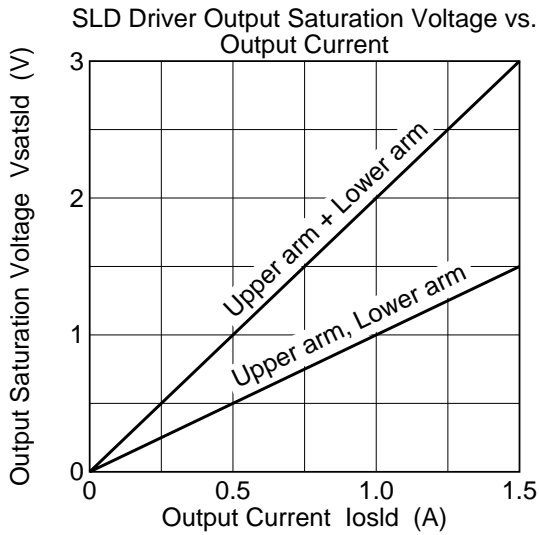
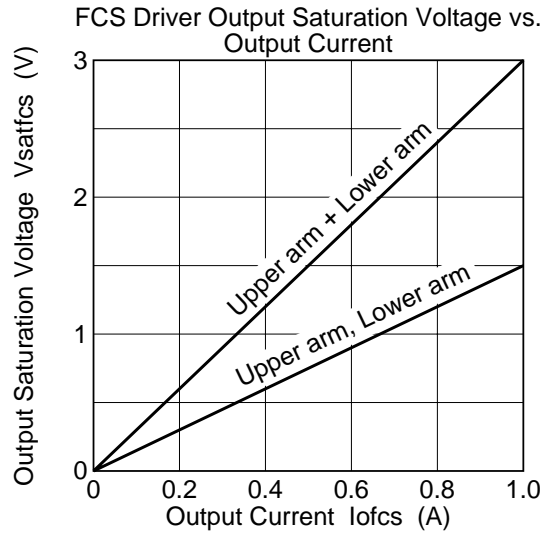
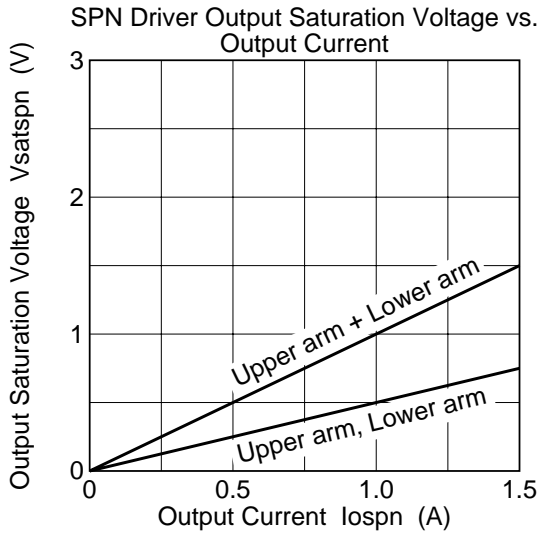


Figure 2

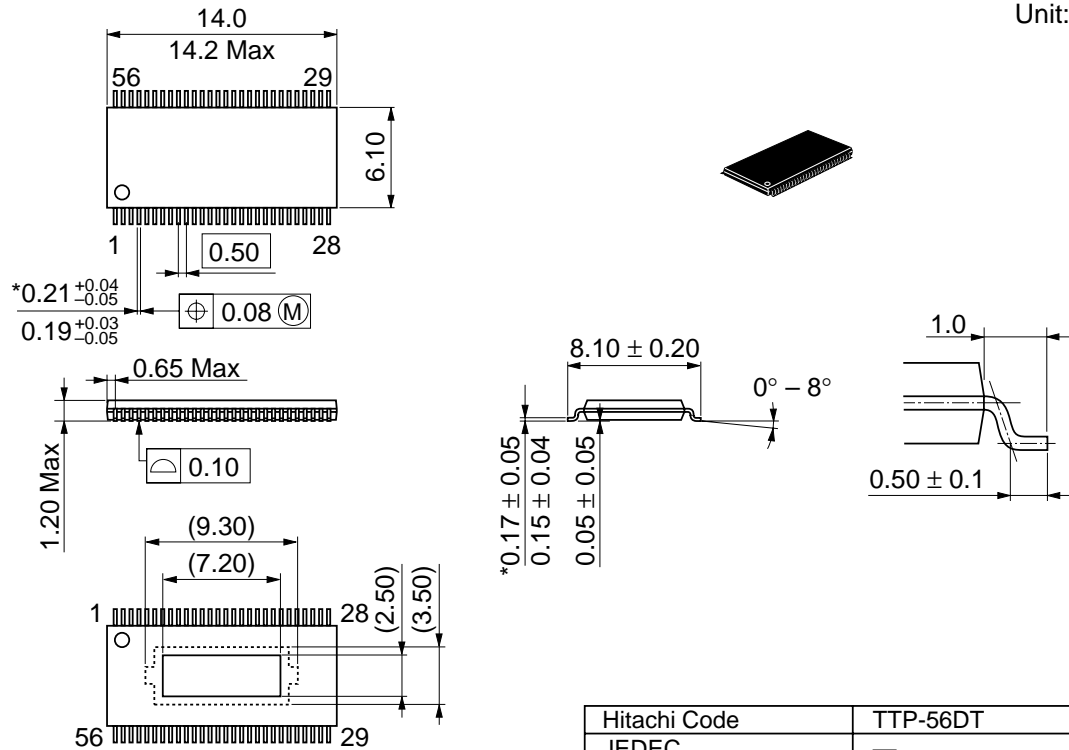
4. If $V_{ref} < 1.5\text{ V}$, 100% PWM duty control may not be possible.
 5. Design guide only.

Reference Data



Package Dimensions

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-56DT
JEDEC	—
EIAJ	—
Weight (reference value)	0.32 g

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