

CM6126

Single-Channel Transient Voltage Suppressor

Product Description

The CM6126 is an *Application Specific Integrated Passive™* (ASIP™) component in a 2 x 2, 4-bump, 0.5 mm pitch, CSP form factor. This device is designed for:

- Transient Voltage Suppression
- Electrostatic Discharge Protection
- Electrical Overstress Protection

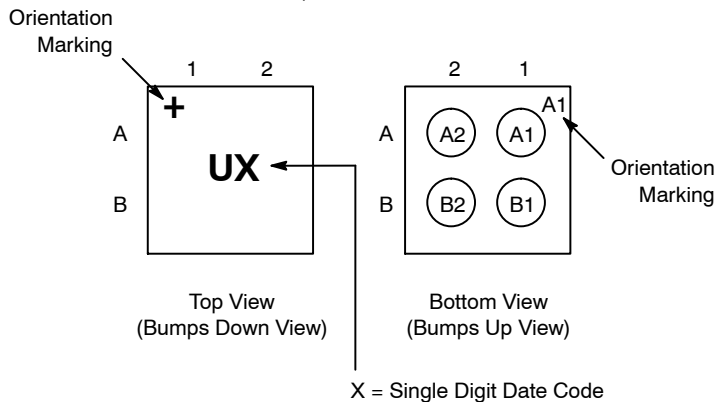
Features

- 4-Bump, 0.96 mm X 0.96 mm Footprint Chip Scale Package (CSP)
- These Devices are Pb-Free and are RoHS Compliant

Table 1. PIN DESCRIPTIONS

4-bump CSP Package	
Pin	Description
A1 and A2	TVS Channel
B1 and B2	Device Ground

PACKAGE / PINOUT DIAGRAMS



4-Bump CSP Package



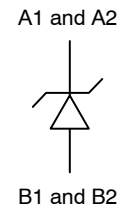
ON Semiconductor®

<http://onsemi.com>



**WLCSP4
CASE 567AW**

ELECTRICAL SCHEMATIC



MARKING DIAGRAM



U = CM6126
X = Single Digit Date Code

ORDERING INFORMATION

Device	Package	Shipping†
CM6126	WLCSP4 (Pb-Free)	5000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

CM6126

ELECTRICAL SPECIFICATIONS AND CONDITIONS

Table 2. PARAMETERS AND OPERATING CONDITIONS

Parameter	Rating	Units
Storage Temperature Range	-55 to +150	°C
Operating Temperature Range	-30 to +85	°C

Table 3. ABSOLUTE RATINGS

Parameter	Rating	Units
Failing to nonconductive, I^2t (Maximum I_{PP} value using 10/1000 μ s pulse). See Notes 1 and 2.	100	A

1. The device must not burn to open-circuit, when the value is below maximum I_{PP} .
2. This parameter is characterized using an ON Semiconductor-specific test board.

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OFF}	Stand-off quiescent current	Stand-off voltage $V_{OFF} = 10$ V			500	nA
V_{BR}	Break down voltage	Break down current $I_{BR} = 15$ mA	16			V
V_{CL}	Clamping voltage during transient	Clamping current $I_{CL} = 1$ A (Note 3)			20	V
V_F	Forward voltage	Forward current $I_F = 850$ mA			1.3	V
C_{L1}	Line capacitance	$V_{BIAS} = 0$ V		280		pF
C_{L2}		$V_{BIAS} = 5$ V; $T_A = 25^\circ\text{C}$	100	135		pF
V_{ESD}	ESD Protection Peak Discharge Voltage at any channel input a) Contact Discharge per IEC 61000-4-2 standard b) Air Discharge per IEC 61000-4-2 standard	$T_A = 25^\circ\text{C}$ (Note 2)				kV
f_C	Minimum Attenuation Freq = 80 MHz - 1 GHz Freq = 1 - 4 GHz	$R_{SOURCE} = R_{LOAD} = 50 \Omega$ $T_A = 25^\circ\text{C}$		11 20		dB

1. All parameters specified for $T_A = -30^\circ\text{C}$ to 85°C unless otherwise noted.
2. Standard IEC 61000-4-2 with $C_{Discharge} = 150$ pF, $R_{Discharge} = 330 \Omega$.
3. Transient: 8 x 20 μ s current pulse.

CM6126

RF CHARACTERISTICS

$T_A = 25^\circ\text{C}$, DC bias = 0 V/ 5 V, 50 Ω Environment

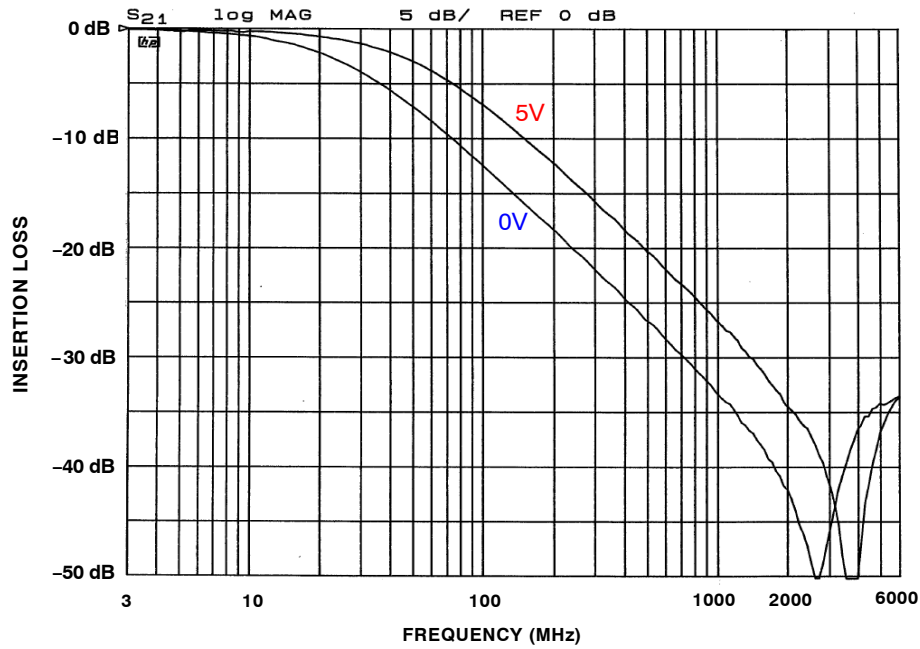


Figure 1. Insertion Loss (0 V and 5 V Bias)

MECHANICAL SPECIFICATION

Table 5. VERTICAL STRUCTURE DIMENSIONS (nominal)

Ref.	Parameter	Material	Dimension
a	Die Thickness	Silicon	406 μm
b	Bump Standoff		240 μm
d	UBM-(Ti/Cu)	Plated Cu	7 μm
		Sputtered Cu	0.4 μm
		Sputtered Ti	0.1 μm
e	UBM Wetting Area Diameter		280 μm
f	Solder Bump Diameter after Bump Reflow		320 μm
c	Metal Pad	AlSiCu	1.5 μm
g	Metal Pad Diameter		324 μm
D2			0.406 mm
D1	Finished Thickness		0.650 mm

Vertical Structure Specification*

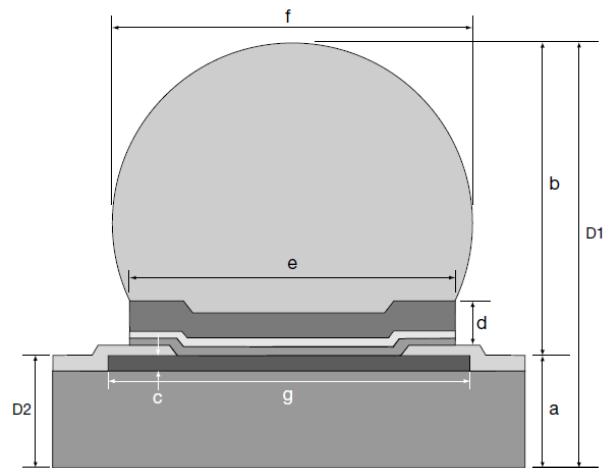


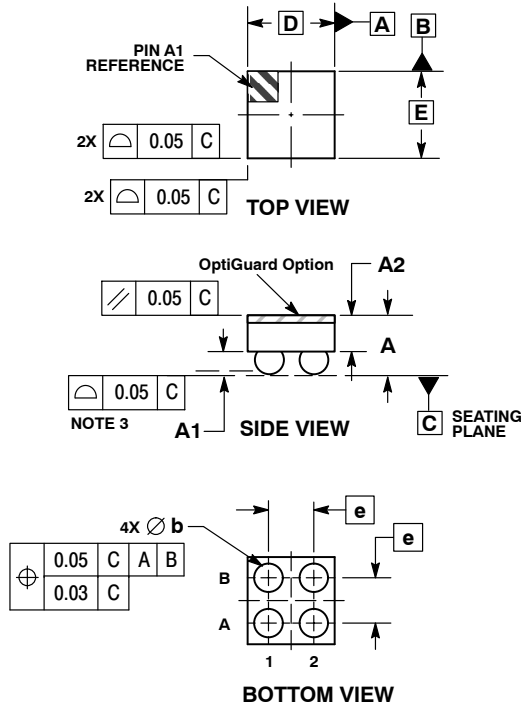
Figure 2. Sectional View

* Daisy Chain CM6010

CM6126

PACKAGE DIMENSIONS

WLCSP4, 0.96x0.96
CASE 567AW-01
ISSUE O

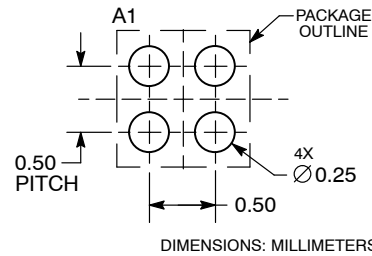


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.56	0.72
A1	0.21	0.27
A2	0.42 REF	
b	0.29	0.35
D	0.96 BSC	
E	0.96 BSC	
e	0.50 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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