CM6308 USB Audio Chip Specification

Datasheet

Version 1.91

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1. Description and Overview

The C-Media CM6308 provides an ideal solution for USB headphone, handset, and display phone products, as well as other PC audio and instant messaging applications. It is a highly integrated chip with a wide range of USB audio and telecom voice control capabilities. The CM6308 combines the audio controller and codec, and also integrates I2C and SPI interfaces, for interfacing with external MCU, LCM or DSP chips. Furthermore, the manufacturer string, product string, serial number, product ID, vendor ID, and initial playback and recording volumes can all be customized by interfacing with an external EEPROM.

Instant messaging and VoIP software are gaining widespread popularity, as they provide real-time audio/video communication in a cost-effective manner. C-Media not only provides the single chip hardware solution for audio peripherals, but also software middleware that enhances instant messaging programs.

All essential analog and digital modules are embedded in the CM6308, including a stereo DAC and stereo ADC, headphone/speaker driving capability, Dynamic Range Compression, Linear microphone gain control, PLL, regulator, USB transceiver, 12 MHz crystal, and power on reset circuit. The CM6308 supports sampling rates of 8KHz, 16Khz, 44.1KHz and 48KHz, with high quailty 16 bit resolution.

Vendors can use the 12 GPIO pins to create a 36 key matrix scan for keypad control functions, saving additional componment cost. Many features are programmable with the external EEPROM and MCU interfaces. Furthemore, MCU/EEPROM/GPIO can easily be controlled through the HID software interface. The buzzer output pin can be easily controlled and changed through software for different frequencies and patterns. In addition, audio adjustments can be made through HID volume control pins. 3 LED indicator pins are supported, to provide more flexible status reporting (On / Off / Operation / playback mute / recording mute) and controllable flash times (using PWM).

Applications：

- High end USB headphone set
- USB interface hub, integrated with multi-media audio features
- USB handset for VOIP and IM applications
- USB display phone for VOIP and Instant Messaging applications
- Proprietary USB wireless audio speakers or headphone set
- Versatile USB audio accessories (adapter, ducking system integration, etc.)

2.Features

- USB spec. 2.0 full speed compatible and USB IF certified
- USB audio device class spec. 1.0 and USB HID class spec. 1.1 compliant
- Supports control, interrupt and isochroous data transfers
- USB suspend/resume and remote wake-up support
- Embedded USB transceiver and power-on reset circuit
- Single 12MHz Crystal Input with On-chip PLL
- Bus-power and self-power mode options supported
- High-power (500mA) and Low-power (100mA) mode options supported
- For Mixer disable mode, USB Audio Function Topology has 3 input Terminals, 2 Output Terminals, one Mixer Unit, one Selector Unit and 4 Feature Units.
- Supports one Control Endpoint, one Isochroous Out Endpoint, one Isochroous In Endpoint, and one Interrupt In Endpoint
- Serial EEPROM programming interface supported for customization of PID/VID/Product string/Manufacturer string
- Supports serial number string (16 Bytes) for operating system detection
- EEPROM interface supports the popular 24C02 data format
- 2 CH DAC output

  DAC sampling rate from 8 KHz, 16 KHz, 44.1 KHz to 48 KHz with 16-bit resolution

  Dynamic Range 95dB, THD+N -85dB ~ -91dB

  Headphone output buffer

  I/F format: Left justified, SPI control interface

  1.2 Vrms biased at 2.25V output swing
- 2 CH ADC Input

  ADC sampling rate from 8Khz, 16KHz, 44.1KHz to 48KHz with 16-bit resolution

  Dynamic Range 88db, THD+N -79dB ~ -84dB

  I/F format:Left justified, SPI control interface

  Digital Linear Microphone Gain Control function (-6dB~33dB)

  1.0 Vrmsbiased at 2.25V input swing

- Supports Stereo Microphone / Playback with soft-mute function
- Microsoft HID Volume control with Vol_Up, Vol_Dn, Playback_Mute and Record_Mute
- Support SPI & I2C (Master/Slave) control interface for interfacing with external controllers
- MCU read/write support for 8 byte data transfer with 3-wire serial interface
- MCU / EEPROM / GPIO control via HID / Vendor command interface
- Embedded Buzzer Function controlled through registers, supporting different patent and frequency settings
- 3 LED indicator pins:
  1. On / Off / Operation
  2. Playback mute
  3. Recording mute
- Supports 12 GPIO pins via HID for 36 key matrix application
- Embedded Power-On-Reset Block
- Single 5V power supply with embedded 5V to 3.3V regulator
- Embedded Anti-Pop Circuit with Internal Feedback Structure
- Industry standard LQFP 64 Pin package
- Compatible with Win2000 SP1~SP4 / WinXP SP1~SP2 / Vista Basic & Premium logo without additional driver
- Plug and play support for MAC OS X
- Plug and play support for Red Hat and Fedora Linux
- Supports Hardware SDK tool for third-party software or soft-phone development
- Instant Message software middleware supporting with：

  Advanced middleware for Windows with AM, VM, Call-forward and Magic voice functions

  Basic middleware application for MAC OSX and Linux platforms

  IM support for Skype, MSN, Yahoo, GoogleTalk, AIM and QQ, ..etc.

  Xear 3D Sound technology on Windows platform (with C-Media's patented driver)

  HRTF 3D, EnvironmentFX, Speaker Shifter and Virtual 7.1CH effects

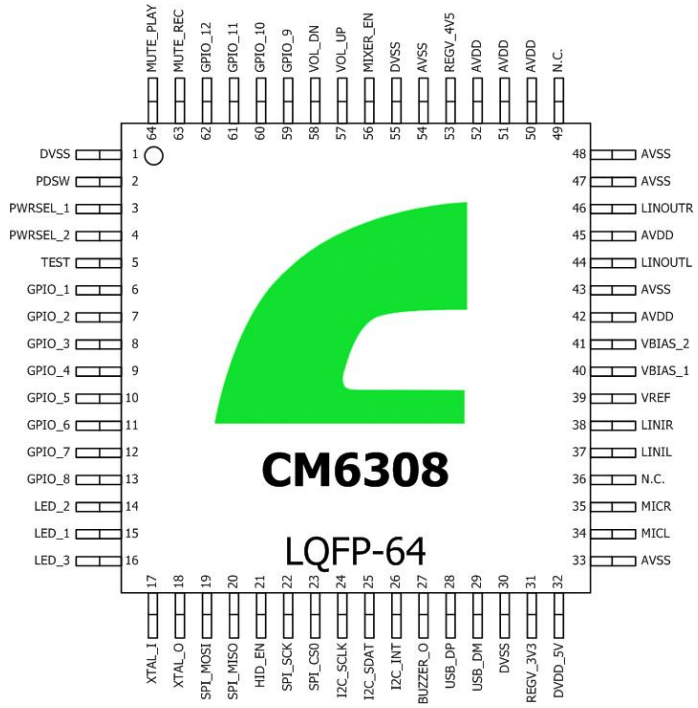
  10 band Equalizer and karaoke functions

3.Pin Descriptions

3.1 PIN ASSIGNMENT BY PIN NUMBER

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	DVSS	17	XTAL_I	33	AVSS	49	N.C.
2	PDSW	18	XTAL_O	34	MICL	50	AVDD
3	PWRSEL_1	19	SPI_MOSI	35	MICR	51	AVDD
4	PWRSEL_2	20	SPI_MISO	36	N.C.	52	AVDD
5	TEST	21	HID_EN	37	LINIL	53	REGV_4V5
6	GPIO_1	22	SPI_SCK	38	LINIR	54	AVSS
7	GPIO_2	23	SPI_CS0	39	VREF	55	DVSS
8	GPIO_3	24	I2C_SCLK	40	VBIAS_1	56	MIXER_EN
9	GPIO_4	25	I2C_SDAT	41	VBIAS_2	57	VOL_UP
10	GPIO_5	26	I2C_INT	42	AVDD	58	VOL_DN
11	GPIO_6	27	BUZZER_0	43	AVSS	59	GPIO_9
12	GPIO_7	28	USB_DP	44	LNOUTL	60	GPIO_10
13	GPIO_8	29	USB_DM	45	AVDD	61	GPIO_11
14	LED_2	30	DVSS	46	LNOUTR	62	GPIO_12
15	LED_1	31	REGV_3V3	47	AVSS	63	MUTE_REC
16	LED_3	32	DVDD_5V	48	AVSS	64	MUTE_PLAY

3.2 PIN-OUT DIAGRAM



3.3 PIN SIGNAL DESCRIPTIONS

No.	Symbol	Type	Description
1	DVSS	P	Digital Ground
2	PDSW	OD, 5V	Power Down Switch Output (0:Normal Operation; 1:Suspend)
3	PWRSEL_1	DIO, PU	Bus/Self Power Selector (0: Self Power; 1: Bus Power)
4	PWRSEL_2	DIO, PU	Power Consumption Selector (0:500mA; 1:100mA)
5	TEST	DI, PD	TEST Mode Select (0: Normal Mode; 1: Test Mode)
6	GPIO_1	DIO	General Purpose I/O Pin
7	GPIO_2	DIO	General Purpose I/O Pin
8	GPIO_3	DIO	General Purpose I/O Pin
9	GPIO_4	DIO	General Purpose I/O Pin
10	GPIO_5	DIO	General Purpose I/O Pin
11	GPIO_6	DIO	General Purpose I/O Pin
12	GPIO_7	DIO	General Purpose I/O Pin
13	GPIO_8	DIO	General Purpose I/O Pin
14	LED_2	DO	LED (Mute Play)
15	LED_1	DO	LED (Play or Record)
16	LED_3	DO	LED (Mute Record)
17	XTAL_I	DI	Input Pin for 12MHz Oscillator
18	XTAL_O	DO	Output Pin for 12MHz Oscillator
19	SPI_MOSI	DIO	SPI
20	SPI_MISO	DIO	SPI
21	HID_EN	DI, PU	HID bottom function enable (0:Disable; 1:Enable)
22	SPI_SCK	DIO	SPI
23	SPI_CS0	DIO	SPI
24	I2C_SCLK	OD, DIO	I2C Serial Clock / EEPROM 24c02 Serial Clock
25	I2C_SDAT	OD, DIO	I2C Serial Data / EEPROM 24c02 Serial Data

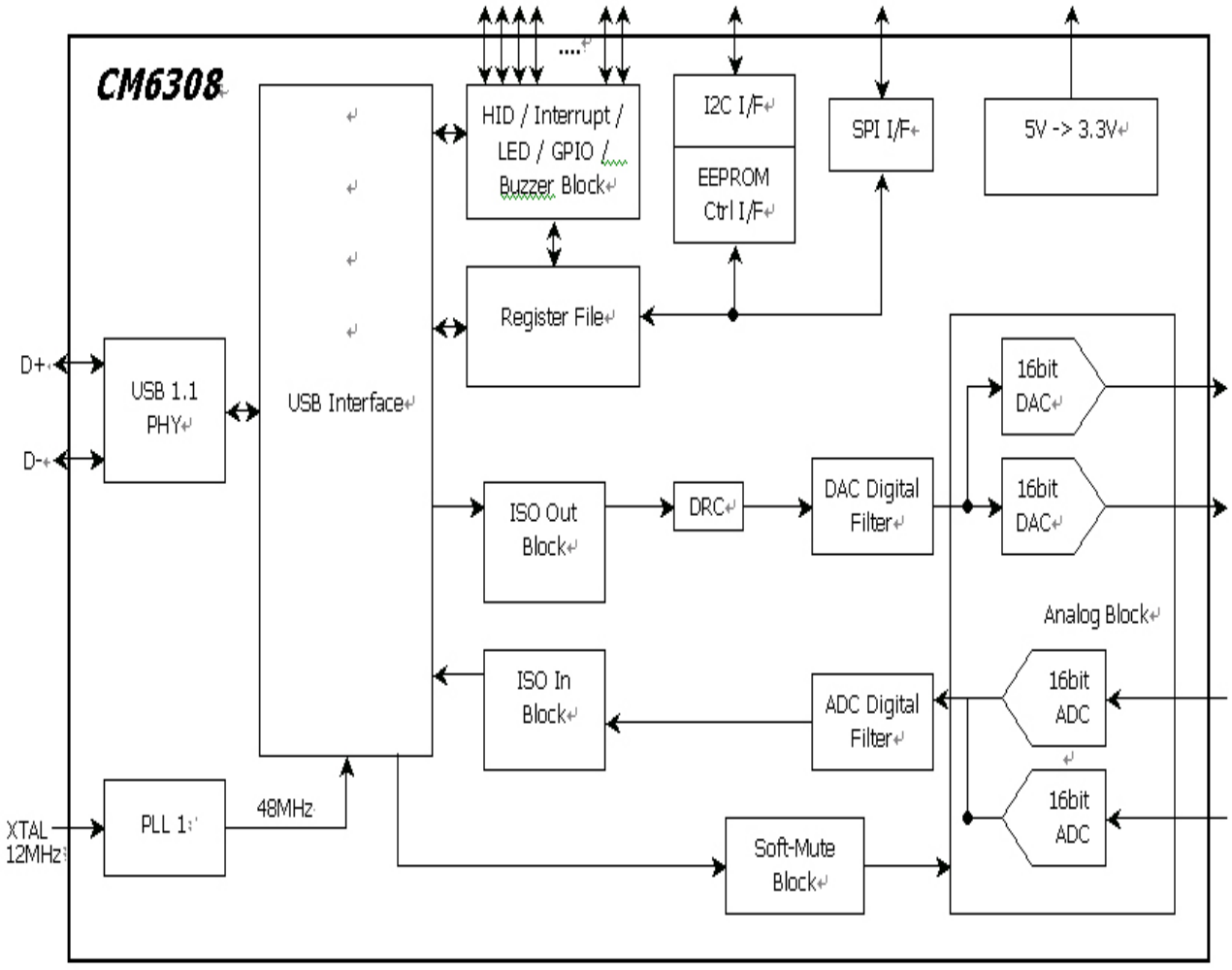
No.	Symbol	Type	Description
26	I2C_INT	DO	I2C Interrupt Output
27	BUZZER_0	DO	Buzzer Output
28	USB_DP	AIO	USB D+
29	USB_DM	AIO	USB D-
30	DVSS	P	Digital Ground
31	REGV_3V3	AO	5V->3.3V Regulator Output
32	DVDD_5V	P	5V Power Supply to Internal Regulator
33	AVSS	P	Analog Ground
34	MICL	AI	MIC0 in left channel
35	MICR	AI	MIC0 in right channel
36	N.C.		
37	LINIL	AI	Differential Line in left channel
38	LINIR	AI	Differential Line in right channel
39	VREF	AO	Bandgap Reference Output 2.25V
40	VBIAS_1	AO	MIC bias Voltage 2.25V/4.5V
41	VBIAS_2	AO	MIC bias Voltage 2.25V/4.5V
42	AVDD	P	5V Analog Power for Analog Circuit
43	AVSS	P	Analog Ground
44	LNOUTL	AO	Line out for left channel
45	AVDD	P	5V Analog Power for Analog Circuit
46	LNOUTR	AO	Line out for right channel
47	AVSS	P	Analog Ground
48	AVSS	P	Analog Ground
49	N.C.		
50	AVDD	P	5V Analog Power for Analog Circuit
51	AVDD	P	5V Analog Power for Analog Circuit
52	AVDD	P	5V Analog Power for Analog Circuit
53	REGV_4V5	AO	4.5V regulator output
54	AVSS	P	Analog Ground
55	DVSS	P	Digital Ground
56	MIXER_EN	DI, PU	Mixer AA-Path enable (0:Disable; 1:Enable)
57	VOL_UP	DI, PU	HID Volume Up
58	VOL_DN	DI, PU	HID Volume Down
59	GPIO_9	DIO	General Purpose I/O Pin

No.	Symbol	Type	Description
60	GPIO_10	DIO	General Purpose I/O Pin
61	GPIO_11	DIO	General Purpose I/O Pin
62	GPIO_12	DIO	General Purpose I/O Pin
63	MUTE_REC	DI, PU	HID (Record Mute)
64	MUTE_PLAY	DI, PU	HID (Playback Mute)

*Notes:
DI -> Digital Input
AI -> Analog Input
OD -> Open Drain
5V -> 5V Torrent
DO -> Digital Output
AO -> Analog Output
PU -> Internal Pull Up
P -> Power
DIO -> Digital I/O
AIO -> Analog I/O
PD -> Internal Pull Down

PWRSEL_1 means that customer may determine which power source will be used on CM6308. For example, the power source of CM6308 can be given from USB port or external adaptor or independent power circuits.
PWRSEL_2 means that customers may select how much current will be limited on CM6308. For most of USB Hub or host controller, each of single USB port may acquire 500mA maximally for CM6308.

4.Block Diagram

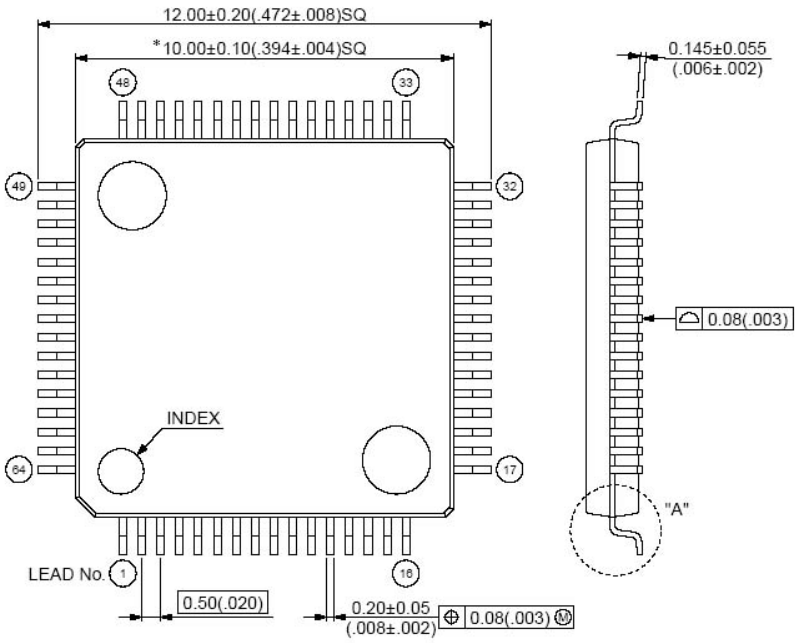


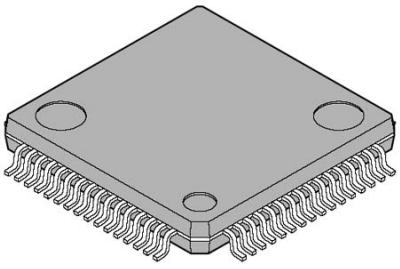
5.ORDERING INFORMATION

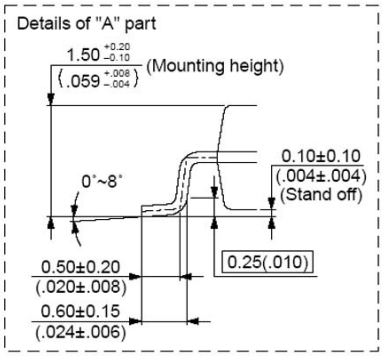
Model Number	Package	Operating Ambient Temperature	Supply Range
CM6308	64-Pin LQFP 10mm×10mm×1.7mm (Plastic)	0°C to +70°C	DVdd = 5V, AVdd = 5V

Physical Dimensions *Dimensions shown in inches and (mm)

64- Lead Thin Plastic Quad Flatpack (LQFP)

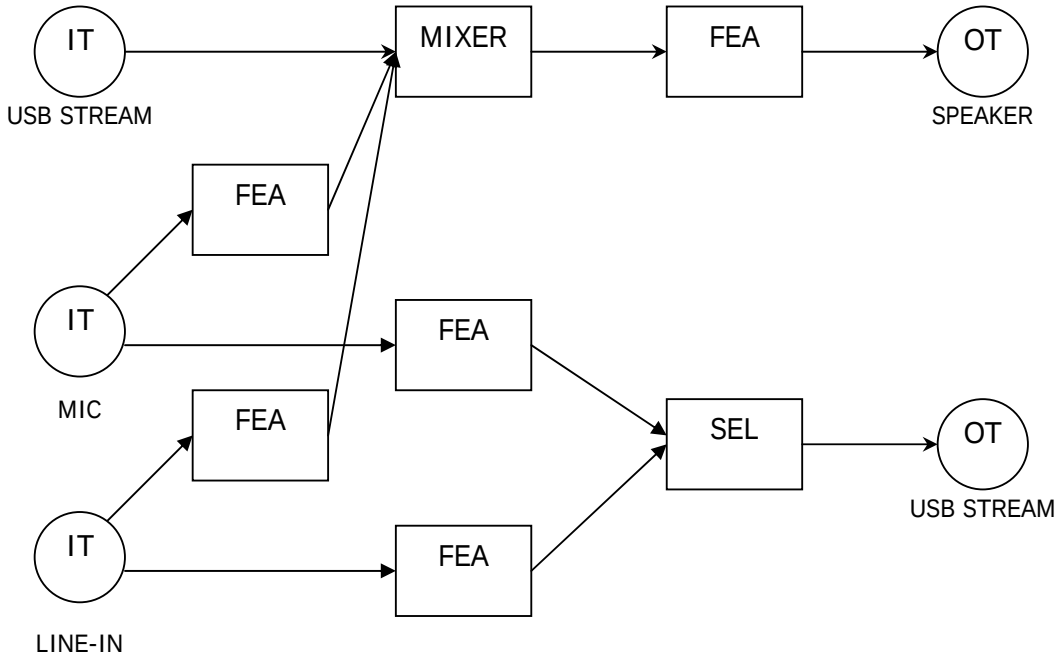






6.USB Audio Topology and Descriptors

6.1 USB Topology



6.2 Device Descriptor

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	12	Descriptor length
1	bDescriptorType	1	01	Device Descriptor
2	bcdUSB	2	0110	USB 1.1 compliant
4	bDeviceClass	1	00	Device class specified by interface
5	bDeviceSubClass	1	00	Device subclass specified by interface
6	bDeviceProtocol	1	00	Device protocol specified by interface
7	bMaxPacketSize0	1	40	Endpoint zero packet size
8	idVendor	2	0d8c	Vendor ID
10	idProduct	2	010F	Product ID
12	bcdDevice	2	0100	Device release number
14	iManufacturer	1	03	Index of string descriptor describing manufacturer
15	iProduct	1	01	Index of string descriptor describing product
16	iSerialNumber	1	00 or 02(*)	Index of string descriptor describing serial number
17	bNumConfigurations	1	01	Number of configuration

Note 1: When a valid EEPROM is detected, the Vendor ID and Product ID will be replaced with the contents of the EEPROM.

Note 2: iSerialNumber is valid only if the external EEPROM contains this information.

6.3 Configuration Descriptor

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	02	Configuration Descriptor
2	wTotalLength	2	0131	Total length of data returned for this configuration: 305 bytes
4	bNumInterfaces	1	04	Number of interfaces supported by this Configuration: 00: Control 01: ISO-Out 02: ISO-In 03: INT-IN (HID)
5	bConfigurationValue	1	01	Configuration value
6	iConfiguration	1	00	Index of string descriptor describing this configuration
7	bmAttributes	1	a0 or 80 or e0 or c0	Bus Power and support Remote Wakeup: 8'ha0 (PWRSEL_1 = 1, HID_EN = 1) Bus Power and no Remote Wakeup: 8'h80 (PWRSEL_1 = 1, HID_EN = 0) Self Power and support Remote Wakeup: 8'he0 (PWRSEL_1 = 0, HID_EN = 1)) Self Power and no Remote Wakeup: 8'hc0 (PWRSEL_1 = 0, HID_EN = 0))
8	bMaxPower	1	32 or fa	Maximum power consumption from bus = 100mA: 8'h32 (50x2 mA) (PWRSEL_2 = 1) Maximum power consumption from bus = 500mA: 8'hfa (250x2 mA) (PWRSEL_2 = 0)

6.4 Standard HID Interface Descriptor

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	04	Interface Descriptor
2	bInterfaceNumber	1	03	Interface number: 03
3	bAlternateSetting	1	00	Alternate interface
4	bNumEndpoints	1	01	Number of endpoints used by this interface
5	bInterfaceClass	1	03	HID Interface Class
6	bInterfaceSubClass	1	00	Subclass code
7	bInterfaceProtocol	1	00	Protocol code
8	iInterface	1	00	Index of string descriptor describing this interface

6.5 Class-specific HID Interface Descriptor

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	21	HID descriptor type
2	bcdHID	2	0100	HID class version
4	bCountryCode	1	00	No country code
5	bNumDescriptors	1	01	One HID class descriptor
6	bDescriptorType	1	22	Report Descriptor
7	wDescriptorLength	2	0032 / 001a	HID class descriptor length in byte: 50 / 26 bytes (Enable / Disable HID Button)

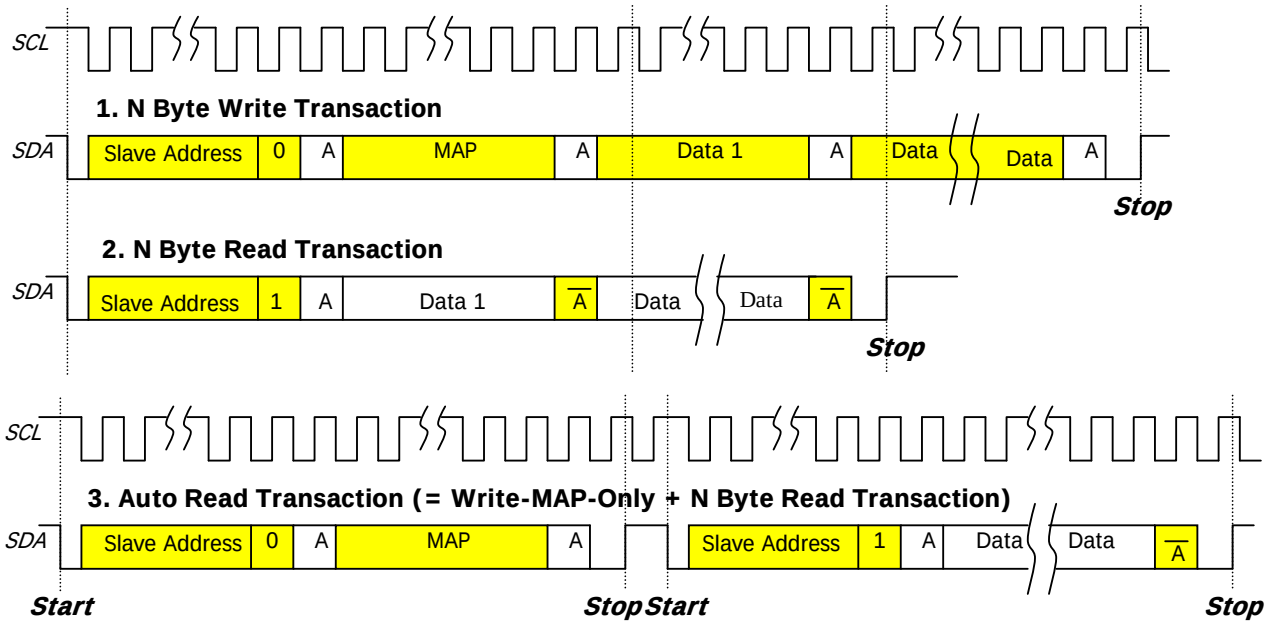
6.6 Standard HID Interrupt In Endpoint Descriptor

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	07	Descriptor length
1	bDescriptorType	1	05	Endpoint Descriptor
2	bEndpointAddress	1	87	IN Endpoint, Endpoint number: 7
3	bmAttributes	1	03	Interrupt Endpoint
4	wMaxPacketSize	2	0010	Maximum packet size: 16 bytes
6	bInterval	1	01	1ms

7.Function Block Descriptions

7.1 I²C Interface

7.1.1 Master Mode:



from master to slave

from slave to master

$A = acknowledg\ e\ (SDA\ Low)$

$\overline{A} = not\ acknowledg\ e\ (SDA\ High)$

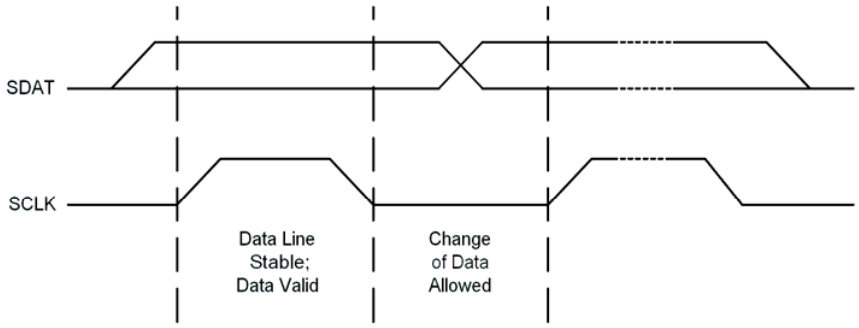
MAP: Memory Address Pointer
(The target register address
in slave device)

7.1.2 Slave Mode:

"7-bit slave address = 7'b0111000"

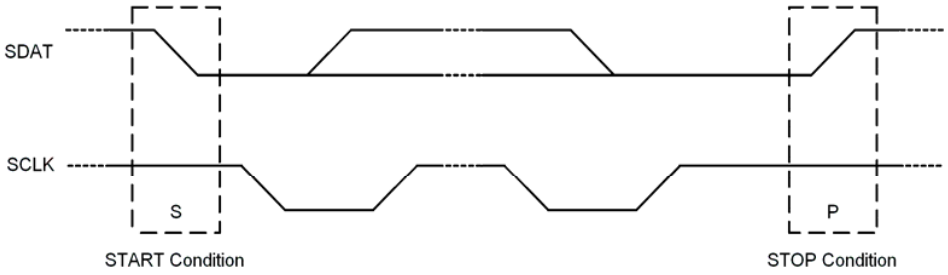
On the MCU serial interface, the CM6308 can serve as a slave device with bit rates up to 400Kbps (in fast mode). The MCU can write data to the CM6308 or read data from the CM6308 (No size limitations when using the I2C Interface). Since the host side and MCU can both access to the internal registers, access contention- when both host and MCU try to access the same register- should be avoided by the application. The 7-bit slave address of the CM6308 is assigned as 7'b0111000. When data is written by the MCU, the CM6308 will NOT transfer any interrupt to the PC until the INT bit of the I2C control Register has been set by the MCU.

The USB host will keep polling the upward HID report every 1ms. When any button is pressed or released, or MCU data is incoming, the CM6308 will transfer 16 bytes of HID report to the USB host. In I2C Slave Mode, the CM6308 has one open-drain input pin 'SCLK' where it receives the serial clock from the MCU, and one open-drain I/O pin 'SDAT' where it sends or receives serial signals to/from the MCU. As shown below, 'SDAT' should be stable when 'SCLK' is high, and can transition only when 'SCLK' is low.



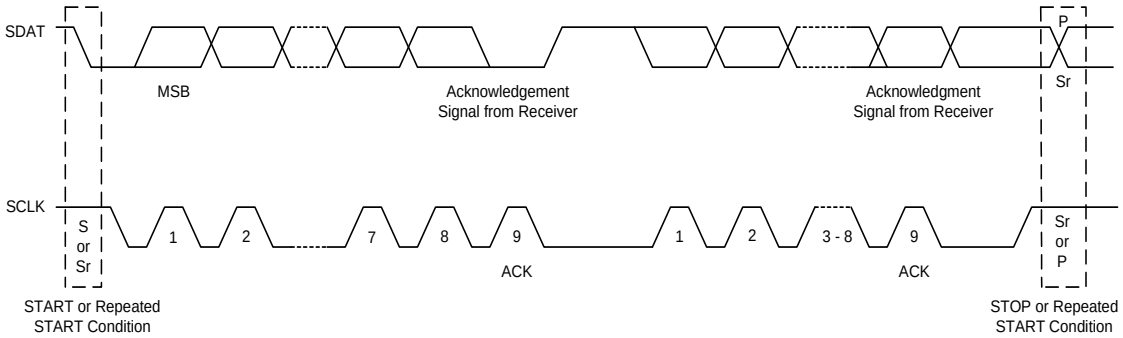
Bit Transfer on the MCU Interface

START and STOP conditions shown below are the exception. Every transaction begins from a START, and ends with a STOP, or another START (repeated START).

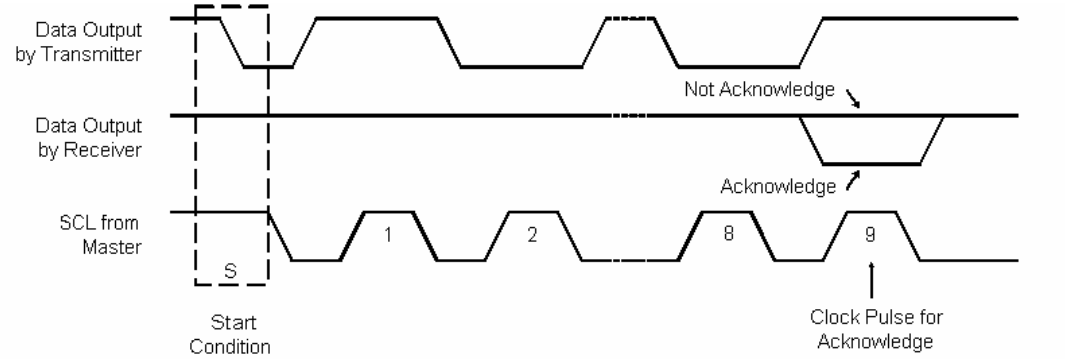


START and STOP Conditions

The figure below demonstrates a typical transaction. After every 8 bits sent by the transmitter, the receiver should send one bit low for positive acknowledgement or one bit high for negative acknowledgement. After the negative acknowledgement, a STOP or repeated START should follow. The next figure shows more details about the acknowledgement bit. Note that 'SCLK' is always driven by the master.

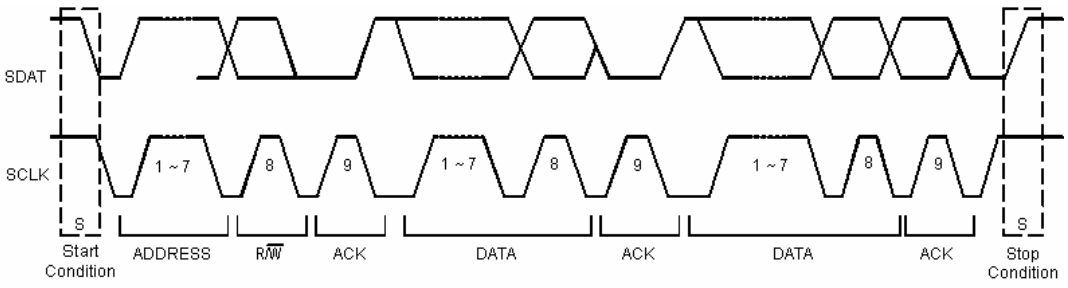


Data Transfer on the MCU Interface



Acknowledge on the MCU Interface

The figure below shows a complete data transfer. After a START, the MCU should send 7-bit slave address (7'b0111000) first, and then the 8th bit denotes a read transfer when it's high; or a write transfer when it's low. The first acknowledgement always comes from the CM6308.



A Complete Data Transfer

In the write transfer, the MCU continues to act as the master and the transfer direction is not changed. The following figure gives an example of a write transfer.

MCU write:

S	0x70	0	addr	0	Byte 0	0	Byte 1	0	….	0	Byte N	0	P

	From CM6308 to MCU		From MCU to CM6308
S	START condition	P	STOP condition
0	Positive acknowledge	1	Negative acknowledge
Byte N	One byte data		

0x70 is the slave address of CM6308, and it also tells CM6308 that it's receiving a write command. CM6308 regards the first coming DATA byte as the register address. The second DATA byte is the DATA content that MCU writes at the register address. CM6308 will auto-increment the register address to the next register address for the following writes DATA. The figure below shows an example of read transfer. The MCU read command can not set the register address, so the MCU may use a write command to set the register address first and then start the read command. Because the CM6308 auto-increments the register address, the second DATA byte will be the register data on the next address.

MCU read:

S	0x70	0	addr	0							
S	0x71	0	Byte 0	0	Byte 1	0	…..	0	Byte N	1	P

	From CM6308 to MCU		From MCU to CM6308
S	START condition	P	STOP condition
0	Positive acknowledge	1	Negative acknowledge
Byte n	One byte data		

The figure below gives a complete picture of a typical transaction between the MCU and CM6308. After a START, the MCU should send a 7-bit slave address (7'b0111000) first, and then the 8th bit denotes a read transfer when it's high; or a write transfer when it's low.

MCU write:

S	0x70	0	addr	0	Byte 0	0	Byte 1	0	…..	0	Byte N	0	P

MCU read:

S	0x70	0	addr	0								
S	0x71	0	Byte 0	0	Byte 1	0	…..	0	Byte N	1	P	

	From CM6308 to MCU		From MCU to CM6308
S	START condition	P	STOP condition
0	Positive acknowledge	1	Negative acknowledge
Byte N	One byte data		

During a write transfer, the MCU continues acting as the transmitter. The CM6308 regards the first DATA byte as the start register address. The following DATA bytes are the content of the registers that the MCU requests. In a read transfer, two transactions are necessary. The MCU resets the start register address by the first transaction, then direction changes to get N of data..

7.2 Serial Peripheral Interface

The SPI interface is used to transfer control data between the CM6308 and external codecs. It is not a standard interface. Every vendor has its own slightly different implementation, but generally speaking, all of them comprise four signals, spi_cen, spi_clock, spi_data_o, spi_data_i. Their meanings are as follows.

- ***spi_cen***: the SPI chip enable signal that is used to inform a codec when it should latch onto the data.
- ***spi_clock***: the SPI clock signal.
- ***spi_data_o***: the SPI data output to codec.
- ***spi_data_i***: the SPI data input from codec.

7.2.1 The SPI Design Goal and SPI Transactions

Our goal is to design a robust SPI interface that can be suitable for all existing codecs. After analyzing the SPI interfaces of several codecs, we have written down the following differences among them.

1). An SPI interface that can read data from and write data to a codec has 4 wires, but some codecs only support input data. In other words, the data in the codec registers can not be retrieved by audio processor. This kind of codec only requires 3 wires.

2). An SPI transaction length is 2 or 3 bytes depending on the codec.

3). Some codecs latch control data on the SPI clock's high state, but others latch control data on the SPI clock's low state

4). The highest SPI clock frequencies are different for many codecs.

For difference 1 listed above, we have designed a 4-wire SPI interface, which is able to accommodate the 3-wire SPI interfaces as well. For difference 2 and 3, control bits in the SPI interface of the CM6308 are used to be initiated a 2-byte or 3-byte data transfer, and maintain SPI clock high or low at codec latching data. All of these can be observed in Figs. A ~ E.

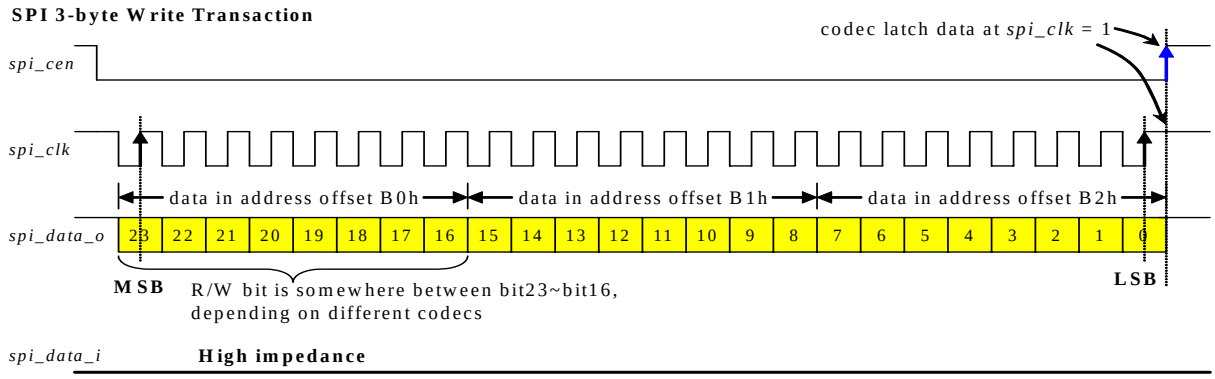


Fig. A. An SPI 3-byte write transaction with codec latching data at *spi_clk* high state.

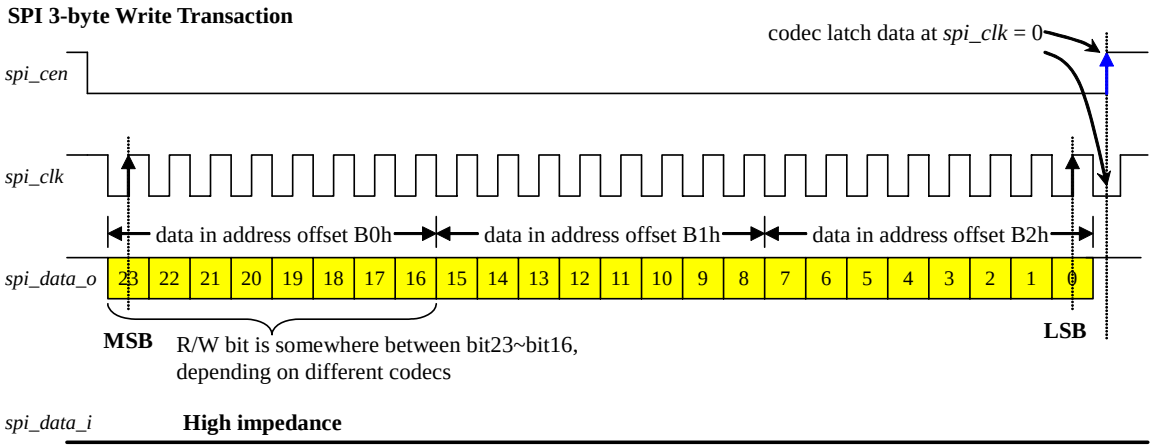


Fig. B. An SPI 3-byte write transaction with codec latching data at *spi_clk* low state.

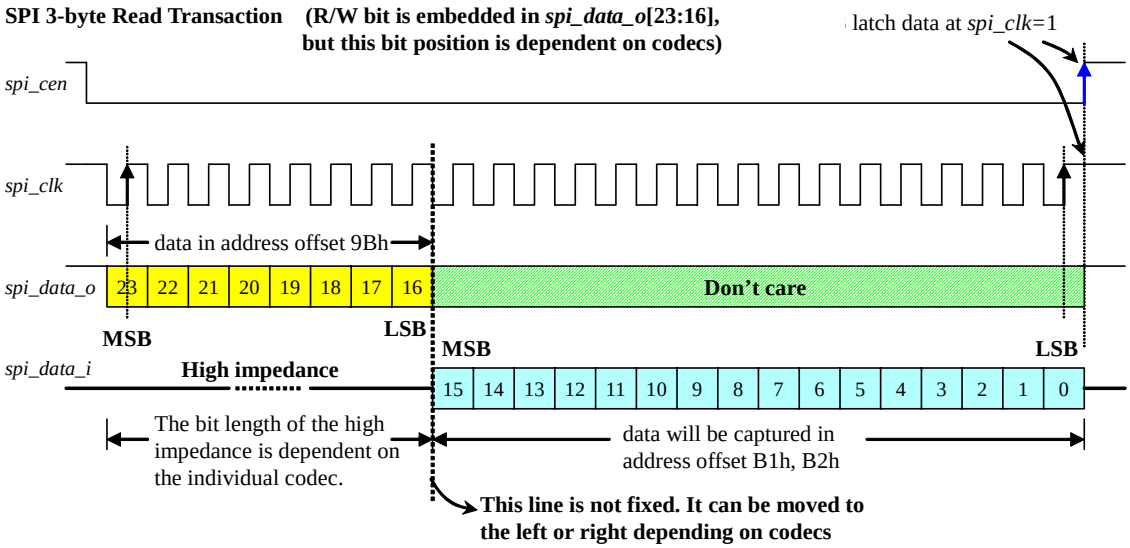


Fig. C. An SPI 3-byte read transaction with codec latching data at *spi_clk* high state.

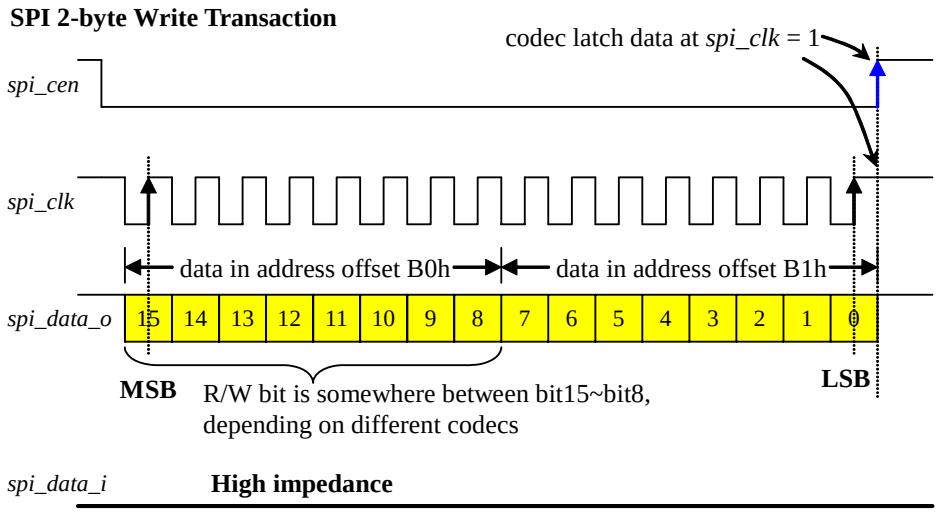


Fig. D. An SPI 2-byte write transaction with codec latching data at *spi_clk* high state.

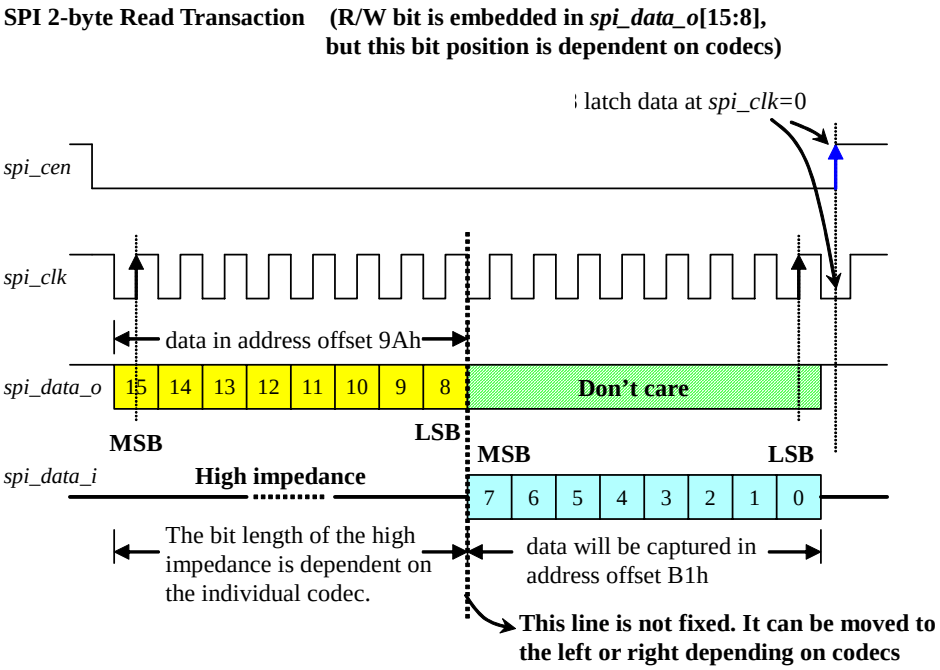


Fig. E. An SPI 2-byte read transaction with codecs latching data at *spi_clk* low state.

In order for our SPI interface to be capable of interfacing with all codecs, the content of the data registers (address offset 9Bh-99h, which includes address, r/w, and data bits) that are written to or read from the codec are not translated by the hardware SPI interface, but by the system driver. The meaning of the bits in this register should be interpreted according to the individual codec.

It is important to notice that the contents of this register, after a write transaction completes, have no meaning. However, after a read transaction completes, you should reference the codec's documentation to see how many bits in this register are valid. For example, if the codec is Analog Device AD1837, then SPI_Data_Reg[9:0] will be valid data.

As the highest SPI clock frequencies are different for many codecs, two control bits are used to adjust the spi_clk frequency to gain the maximum transfer speed. The CM6308 can control up to six codecs through the SPI interface, as shown in Fig. F below.

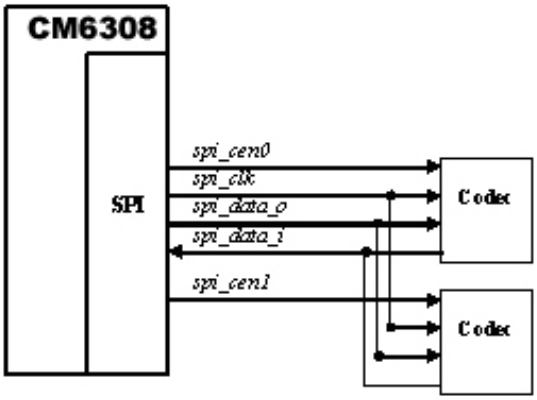
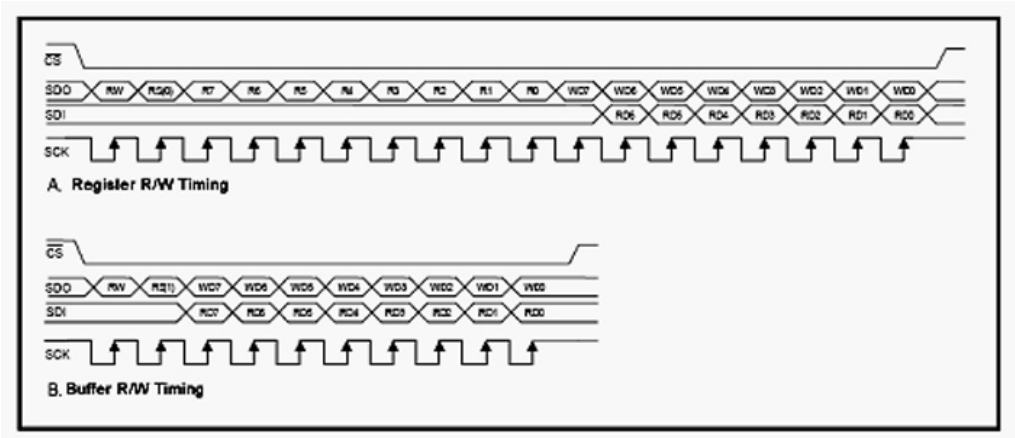


Fig. F. The SPI connection topology

7.2.2 2-bit leading mode

2-bit leading mode is designated for LCM controllers. Its waveform is almost the same as the general SPI except for two extra bits, RW and RS, in the beginning of each transaction. See the following figure.



7.2.3 The Serial Interface

The serial data is read from the serial data input pin on the rising edge of the serial clocks D7, D6 through D0, in this order. This data is converted to 8 bits of parallel data on the rising edge of the eighth serial clock cycle for the processing. The A0 input is used to determine whether or not the serial data input is displaying data or command data; when A0 = “H”, the data is display data, and when A0 = “L” then the data is command data. The A0 input is read and used for detection every 8th rising edge of the serial clock after the chip active. Figure 1 is a serial interface signal chart.

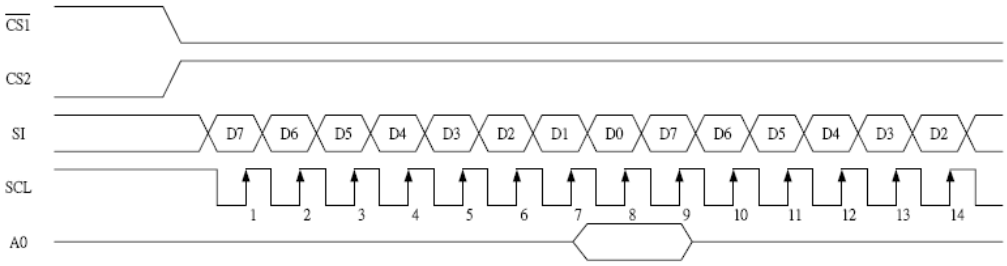
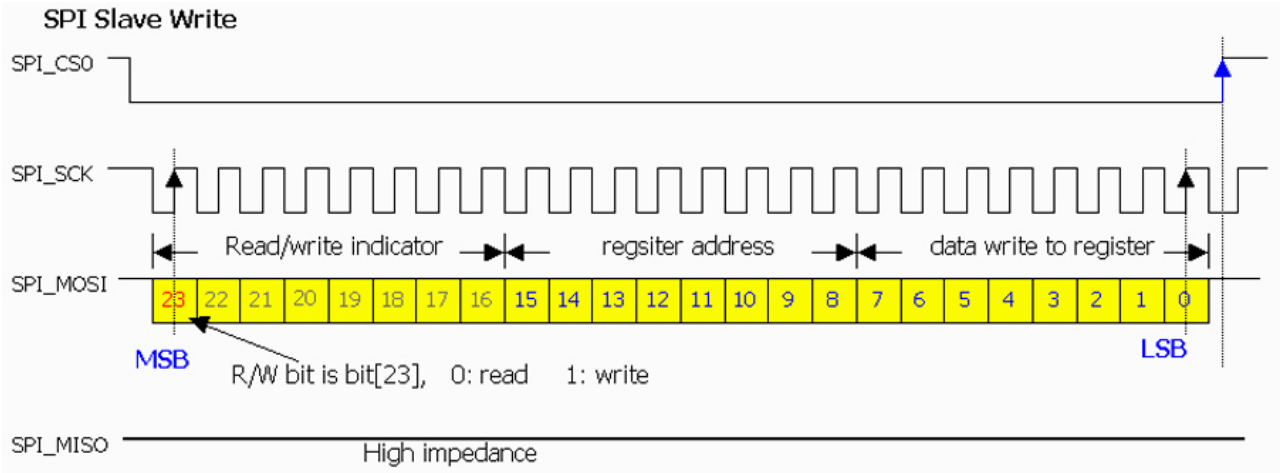
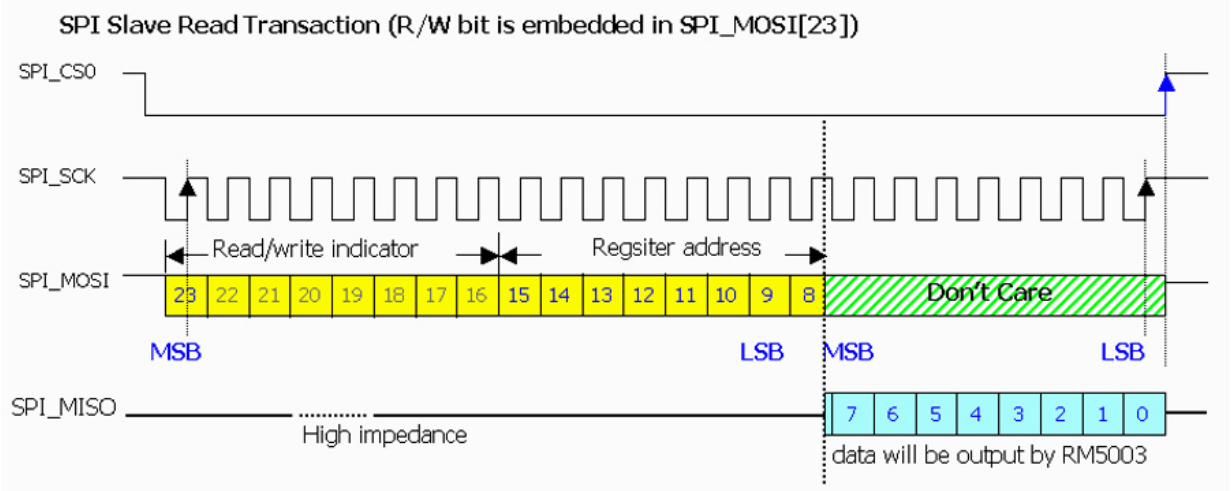


Figure 1

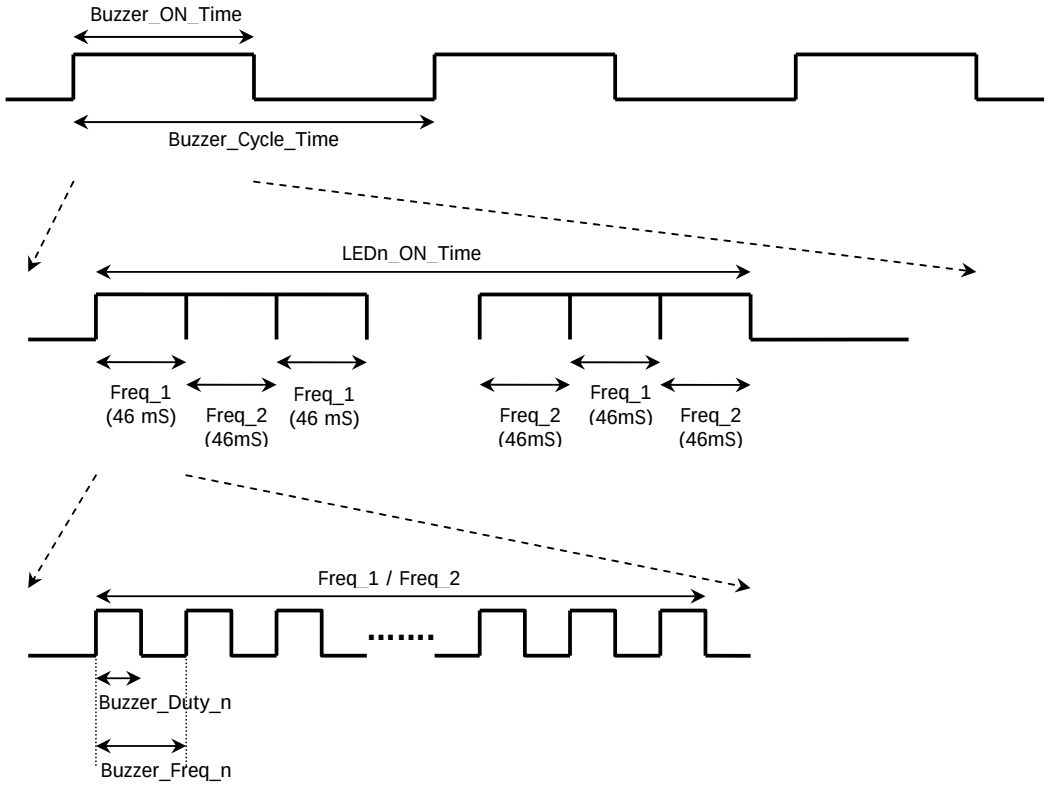
When the CM6308 acts as a SPI slave, the external MCU can read/write registers within the CM6308 through the SPI interface. Each transaction is 3-bytes long. The first byte is a read/write command indicator. Once the MSB of the first byte is low, it means a read transaction is occurring; otherwise it is a write transaction. The other bits of the first byte are meaningless. The second byte is the address of the desired register. The third byte, for a read transaction, is meaningless, and meanwhile the MISO would output the data of register. The third byte, for write transactions, is data.





7.3 Buzzer Behavior and Software Control

There are 2 main frequencies (default 3KHz & 300Hz) in the final tone, as shown below:

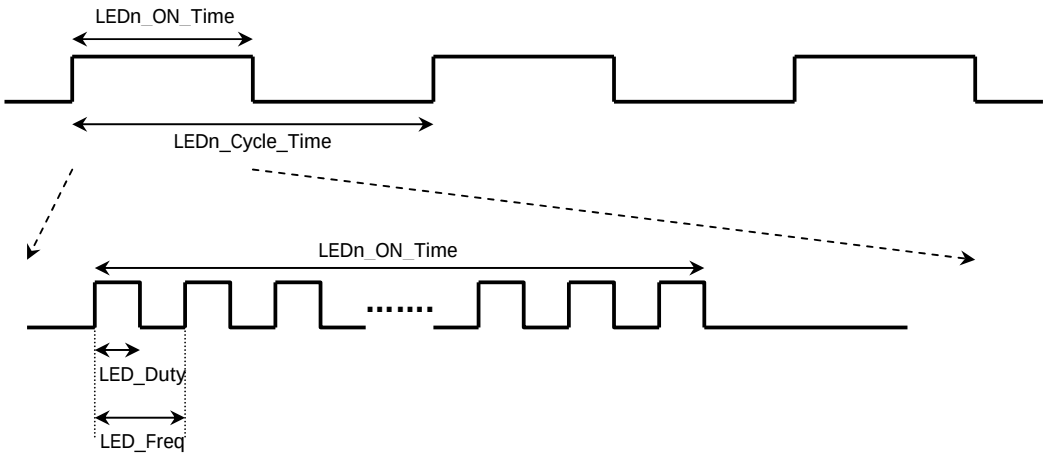


*Note: 1. Unit for Buzzer_Duty_n / Buzzer_Freq_n (Resolution) = 42.67 uS
2. Unit for Buzzer_ON_Time / Buzzer_Cycle_Time (Resolution) = 21.85 mS
3. Duration for Freq_1 & Freq_2 = 46 mS

7.4 LED Behavior and Software Control

LED1 (Config & Play/Rec)	3 times / sec
LED2 (Config & Play Mute)	Always On
LED3 (Config & Rec Mute)	1 time / sec

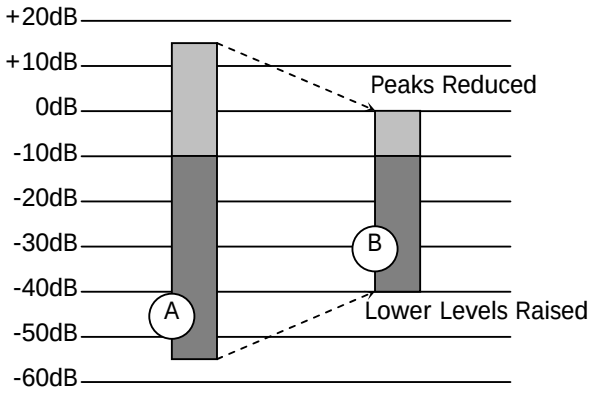
The LED Signal resembles a PWM waveform:



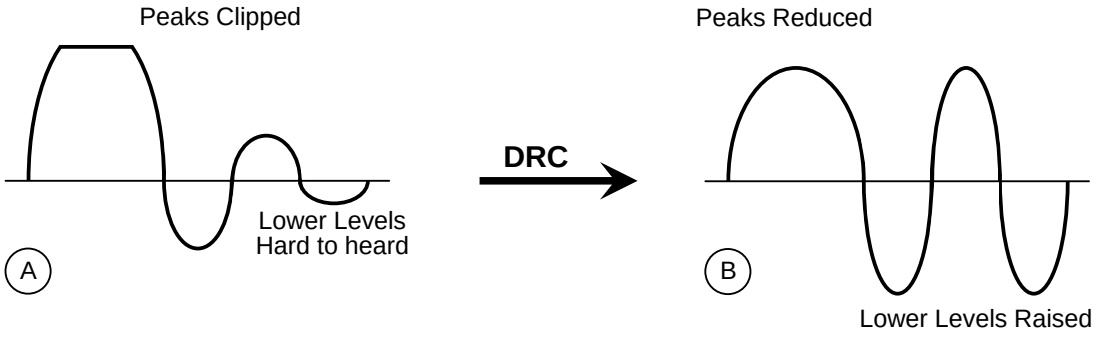
* Notes: 1. Unit for LED_Duty / LED_Freq (Resolution) = 42.67 uS
2. Unit for LEDn_ON_Time / LEDn_Cycle_Time (Resolution) = 21.85 mS

7.5 DRC (Dynamic Range Compression)

Dynamic Range is defined as the difference, in decibels (dB), between the loudest and quietest sounds in any particular piece of audio content. Classical music is a good example, with ranges from piano (soft) to forte to FFF (for extremely loud). Movies also typically have a wide dynamic range, which may cause you to have to turn the volume up and down as scenes change. For example, when watching a movie at home, you may be forced to turn up volume to hear the dialogue in a quiet scene, and then quickly turn it down again during a car chase scene that follows. In this way, there may be times in a home theater environment when it would be useful to be able to control the dynamic range.



With Dynamic Range Control enabled, the full dynamic range (A) of the program is reduced (B).



In CM6308, The maximum Increase Level is +12.5dB.

7.6 EEPROM Content Data Format

24c02 (256 x 8 bit)

[ADDR] [DATA]

0x00, Magic Word (“C”, 8’h43)

0x01, Magic Word (“M”, 8’h4D)

0x02, Total Data Length in EEPROM

0x03, EEPROM Content Setting

bit 0:	*Manufacture String Valid?*	*(0: No, 1: Yes)*
bit 1:	*Product String Valid?*	*(0: No, 1: Yes)*
bit 2:	*Serial Number Valid?*	*(0: No, 1: Yes)*
bit 3:	*Reserved*	*(Default 0)*
bit 4:	*Playback (DAC) Control Valid?*	*(0: No, 1: Yes)*
bit 5:	*Recording (ADC) Control Valid?*	*(0: No, 1: Yes)*
bit 6:	*Mixer (AA-Path) Control Valid?*	*(0: No, 1: Yes)*
bit 7:	*Enable Remote Wakeup?*	*(0: Disable, 1: Enable)*

0x04, Reserved (Default 8’h00)

0x05, Playback (DAC) Control

bit[5:0]:	*DAC (Unit f9) initial Volume*	
	(6’h3f ~ 6’h1a, -2.6 ~ -34.5dB/Mute, linear step)	
bit 6:	*Mute_f9 (DAC) initial Value*	*(0: Un-Mute, 1: Mute)*
bit 7:	*DRC initial Value*	*(0: Disable, 1: Enable)*

0x06, Recording (ADC) Control

bit[4:0]:	*ADC (Unit fa / fb) initial Volume*	
	(5’h1f ~ 5’h04, +33 ~ -6dB/Mute, -1.5dB/step)	
bit 5:	*Reserved*	*(Default 0)*
bit 6:	*Mute_fb (ADC Line) initial Value*	*(0: Un-Mute, 1: Mute)*
bit 7:	*Mute_fa (ADC Mic) initial Value*	*(0: Un-Mute, 1: Mute)*

[ADDR]	[DATA]
0x07,	Mixer (AA-Path) Control *bit[5:0]: AA-Path (Unit fd / fe) initial Volume* *(6'38 ~ 6'h10, +22.5 ~ -36dB/Mute, -1.5dB/step)* *bit 6: Mute_fe (AA Line) initial Value (0: Un-Mute, 1: Mute)* *bit 7: Mute_fd (AA Mic) initial Value (0: Un-Mute, 1: Mute)*
0x08,	VID (Low Byte)
0x09,	VID (High Byte)
0x0A,	PID (Low Byte)
0x0B,	PID (High Byte)
0x0C ~ 0x29	Manufacture String (30 bytes) *0x0c [String1]* *0x0d [String2]* *… …* *0x29 [String30]*
0x2A ~ 0x65	Product String (60 bytes) *0x2A [String1]* *0x2B [String2]* *… …* *0x65 [String60]*
0x66 ~ 0x75	String of Serial Number (16 bytes) *0x66 [String1]* *0x67 [String2]* *… …* *0x75 [String16]*
0x76 ~ 0xFF	Reserved (Default 8'h00)

8.Electrical Characteristics:

8.1 Absolute Maximum Rating

Symbol	Parameter	Value	Unit
Dvmin	Min Digital Supply Voltage	– 0.3	V
Dvmax	Max Digital Supply Voltage	+ 6	V
Avmin	Min Analog Supply Voltage	– 0.3	V
Avmax	Max Analog Supply Voltage	+ 6	V
Dvinout	Voltage on any Digital Input or Output Pin	–0.3 to +5.5	V
Avinout	Voltage on any Analog Input or Output Pin	–0.3 to +5.5	V
T_{stg}	Storage Temperature Range	-40 to +125	^{0}C
ESD (HBM)	ESD Human Body Mode	3500	V
ESD (MM)	ESD Machine Mode	200	V

8.2 Operation Conditions

Operation conditions				
	Min	Typ	Max	Unit
Analog Supply Voltage	4.75	5.0	5.25	V
Digital Supply Voltage	4.75	5.0	5.25	V
Operation Power Consumption, 4 Ohm Loading **(*Notes)**	-	300	330	mA
Operation Power Consumption, 10K Ohm Loading **(*Notes)**	-	110	120	mA
Standby Power Consumption	-	85	-	mA
Suspend Mode Power Consumption	-	380	-	uA
Operating ambient temperature	0	-	70	^{0}C

***Notes:** Test Environment Under 25^{o}C, 5.0V, 48K Sample Rate,
Max Output is Playing 1K Full Scale Sin Wave, Typical Output is Playing Music.

8.3 Electrical Parameters

	Min	Typ	Max	Unit
DAC (10K Ohm Loading)				
Resolution	-	16	-	Bits
THD + N (20 ~ 20KHz)	-85	-	-91	dB
Dynamic Range (20 ~ 20KHz)	-	95	-	dB
Cross Talk (20 ~ 20KHz)	-100	-	-112	dB
Frequency Response 48KHz	20	-	20K	Hz
Frequency Response 44.1KHz	20	-	20K	Hz
Output Voltage (rms)	-	1.27	-	Vrms
Inter Channel Phase Delay	0.03	-	0.09	Deg.
ADC				
Resolution	-	16	-	bit
THD + N (20 ~ 20KHz)	-79	-	-84	dB
Dynamic Range (20 ~ 20KHz)	-	88	-	dB
Frequency Response 48KHz	20	-	20K	Hz
Frequency Response 44.1KHz	20	-	20K	Hz
Input Voltage (rms)	-	1	-	Vrms

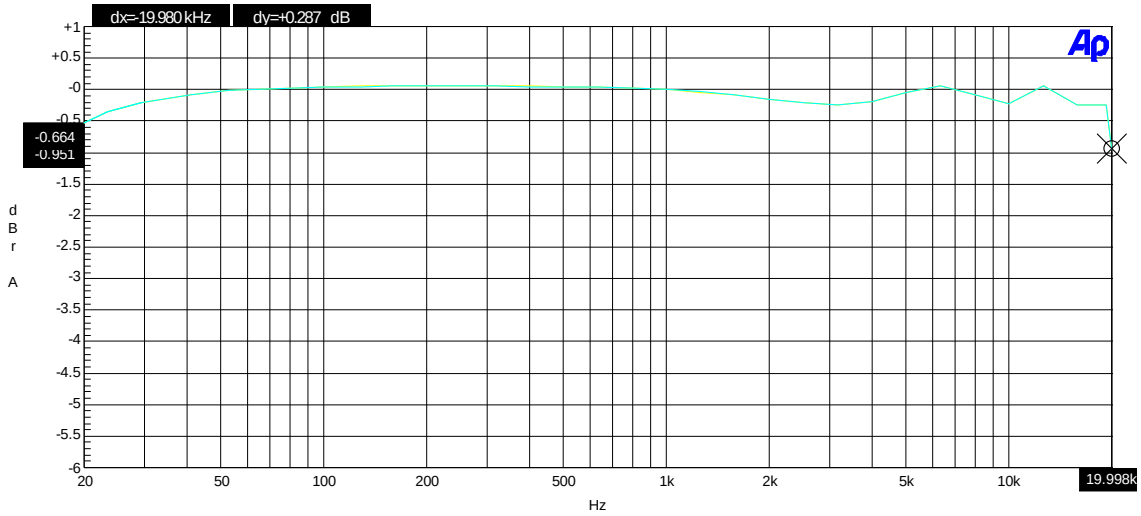
***Notes:** Test Environment Under 25^{o}C, 5.0V, 10KOhm Loading

9. FREQUENCY RESPONSE GRAPHS

9.1 Digital Playback for Line Output Frequency (10K Ohm Loading)

9.1.1 Frequency Response 48Ks/Sec (10K Ohm Loading)

Audio Precision 08/09/06 15:47:40

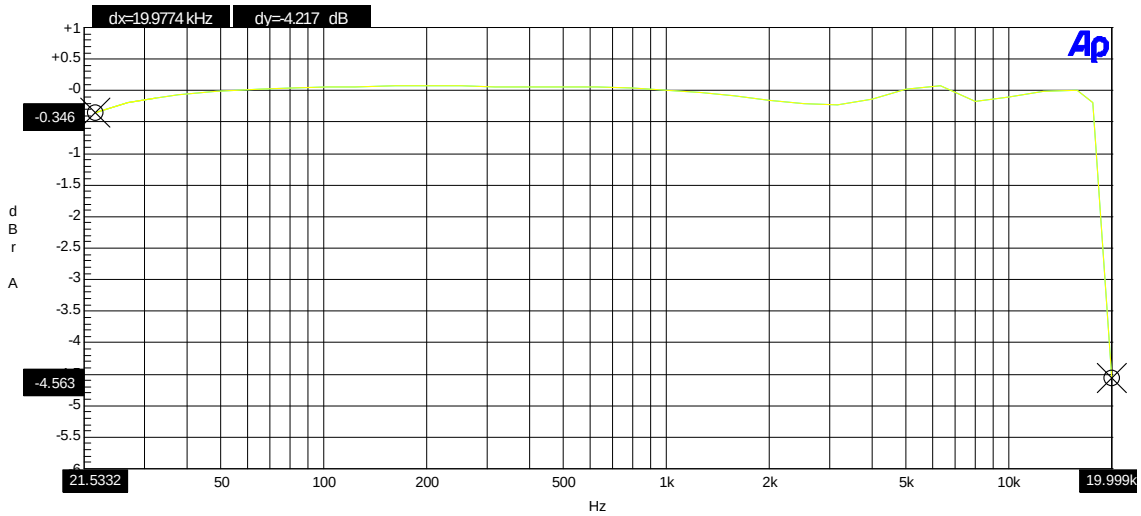


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Cyan	Solid	1	Fasttest.Ch.1 Ampl!Normalize	Left		*-0.951 dBr A	*-0.664 dBr A
1	2	Yellow	Solid	1	Fasttest.Ch.2 Ampl!Normalize	Left		-0.952 dBr A	-0.664 dBr A

Vista-Frequency Response-M48k.at27

9.1.2 Frequency Response 44.1Ks/Sec (10K Ohm Loading)

Audio Precision 08/09/06 16:20:55



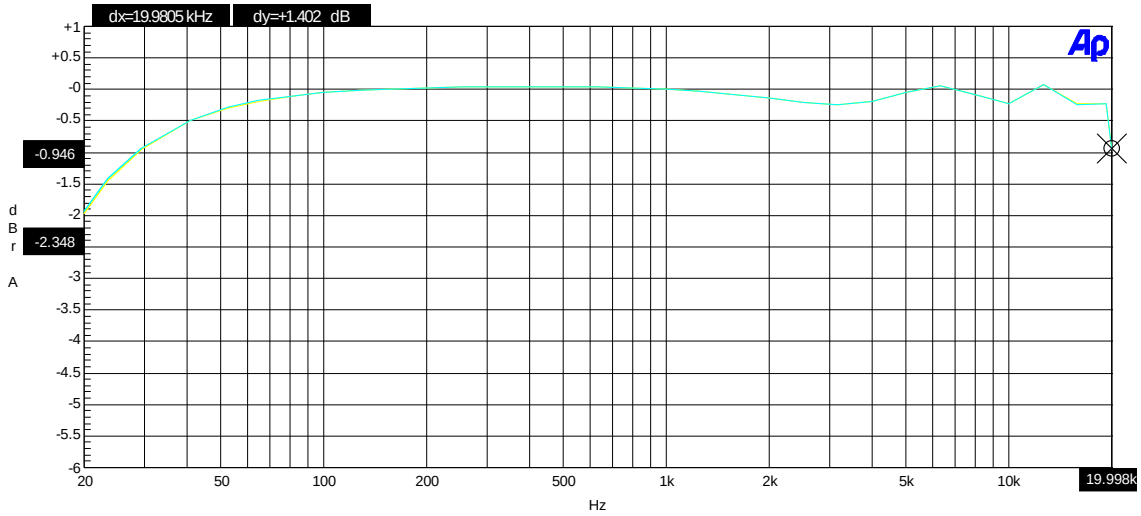
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Cyan	Solid	1	Fasttest.Ch.1 Ampl!Normalize	Left		*-0.346 dBr A	*-4.563 dBr A
1	2	Yellow	Solid	1	Fasttest.Ch.2 Ampl!Normalize	Left		-0.346 dBr A	-4.564 dBr A

Vista-Frequency Response-M44k.at27

9.2 Digital Playback for Line Output Frequency (32 Ohm Loading)

9.2.1 Frequency Response 48Ks/Sec (32 Ohm Loading)

Audio Precision 08/09/06 16:30:39

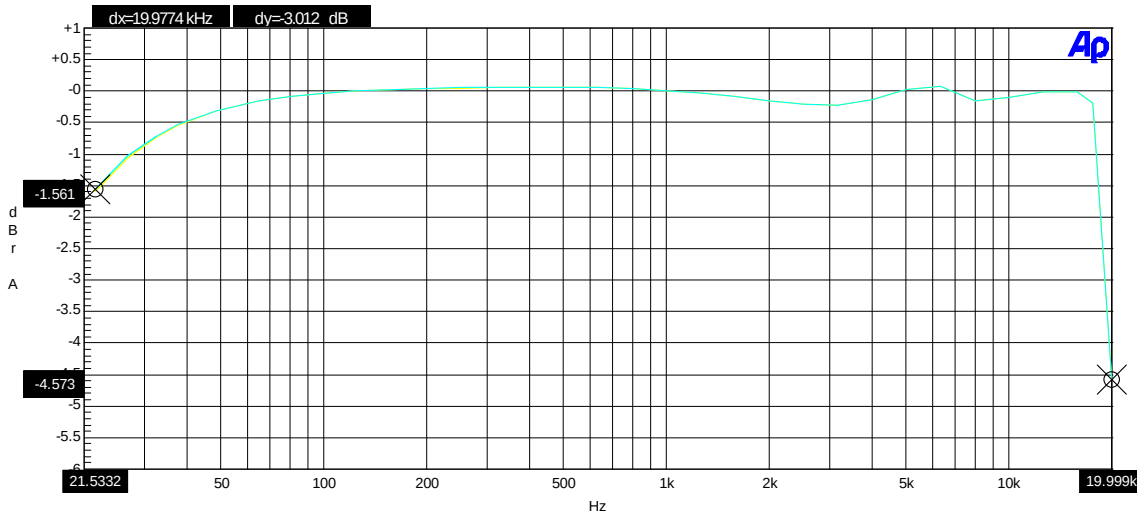


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Cyan	Solid	1	Fasttest.Ch.1 Ampl!Normalize	Left		*-2.348 dBr A	*-0.946 dBr A
1	2	Yellow	Solid	1	Fasttest.Ch.2 Ampl!Normalize	Left		-2.387 dBr A	-0.946 dBr A

Vista-Frequency Response-M48k.at27

9.2.2 Frequency Response 44.1Ks/Sec (32 Ohm Loading)

Audio Precision 08/09/06 16:39:28



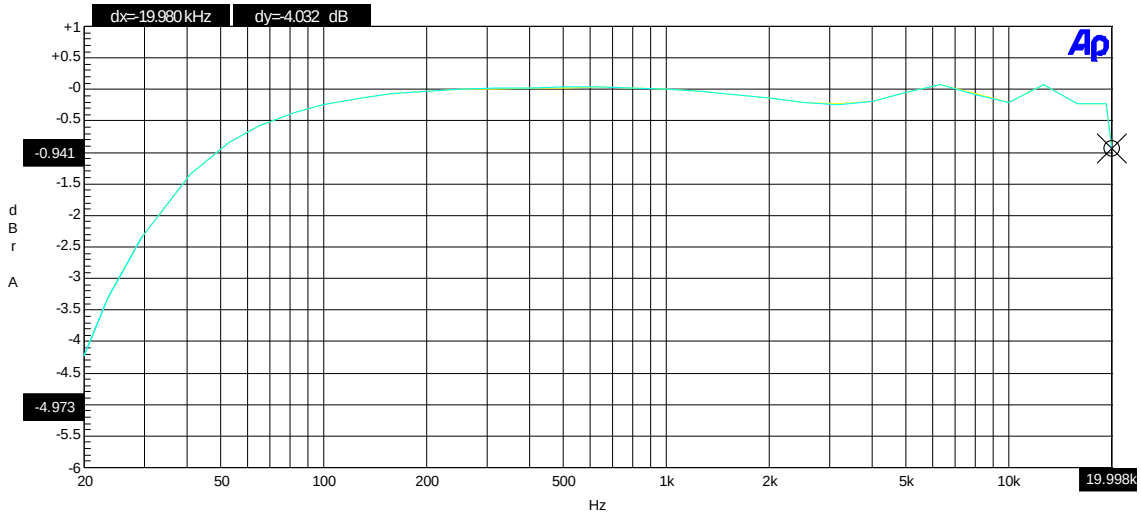
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Cyan	Solid	1	Fasttest.Ch.1 Ampl!Normalize	Left		*-1.561 dBr A	*-4.573 dBr A
1	2	Yellow	Solid	1	Fasttest.Ch.2 Ampl!Normalize	Left		-1.590 dBr A	-4.572 dBr A

Vista-Frequency Response-M44k.at27

9.3 Digital Playback for Line Output Frequency (16 Ohm Loading)

9.3.1 Frequency Response 48Ks/Sec (16 Ohm Loading)

Audio Precision 08/09/06 16:56:01

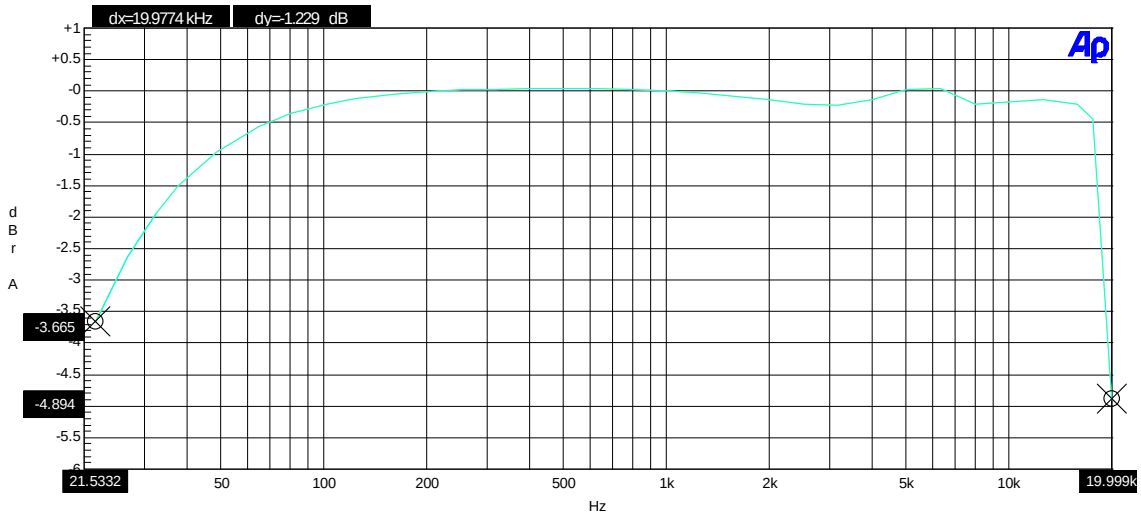


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Cyan	Solid	1	Fasttest.Ch.1 Ampl!Normalize	Left		*-0.941 dBr A	*-4.973 dBr A
1	2	Yellow	Solid	1	Fasttest.Ch.2 Ampl!Normalize	Left		-0.940 dBr A	-4.962 dBr A

Vista-Frequency Response-M48k.at27

9.3.2 Frequency Response 44.1Ks/Sec (16 Ohm Loading)

Audio Precision 08/09/06 17:03:08



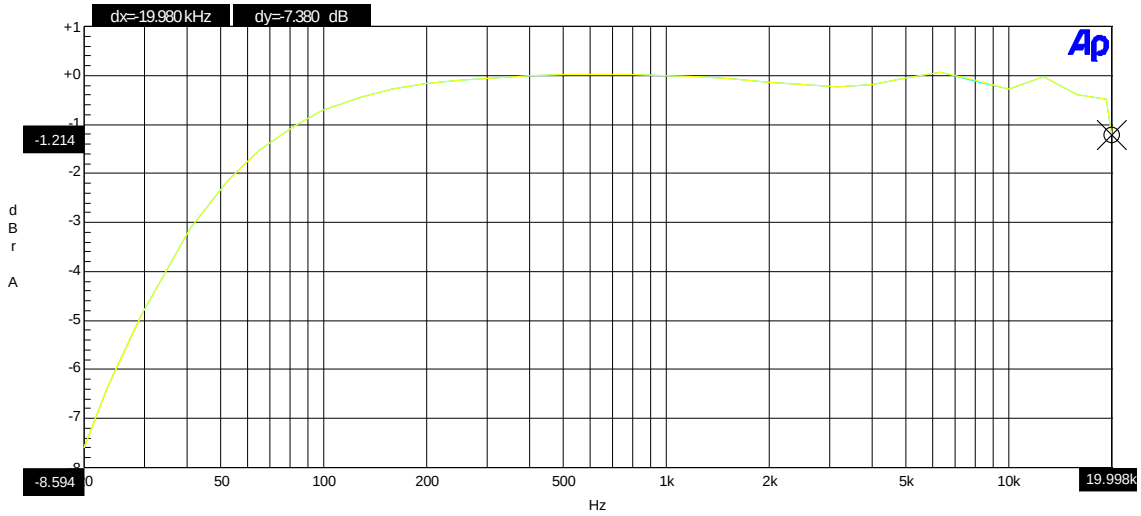
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Cyan	Solid	1	Fasttest.Ch.1 Ampl!Normalize	Left		*-3.665 dBr A	*-4.894 dBr A
1	2	Yellow	Solid	1	Fasttest.Ch.2 Ampl!Normalize	Left		-3.657 dBr A	-4.893 dBr A

Vista-Frequency Response-M44k.at27

9.4 Digital Playback for Line Output Frequency (8 Ohm Loading)

9.4.1 Frequency Response 48Ks/Sec (8 Ohm Loading)

Audio Precision 08/09/06 18:01:23

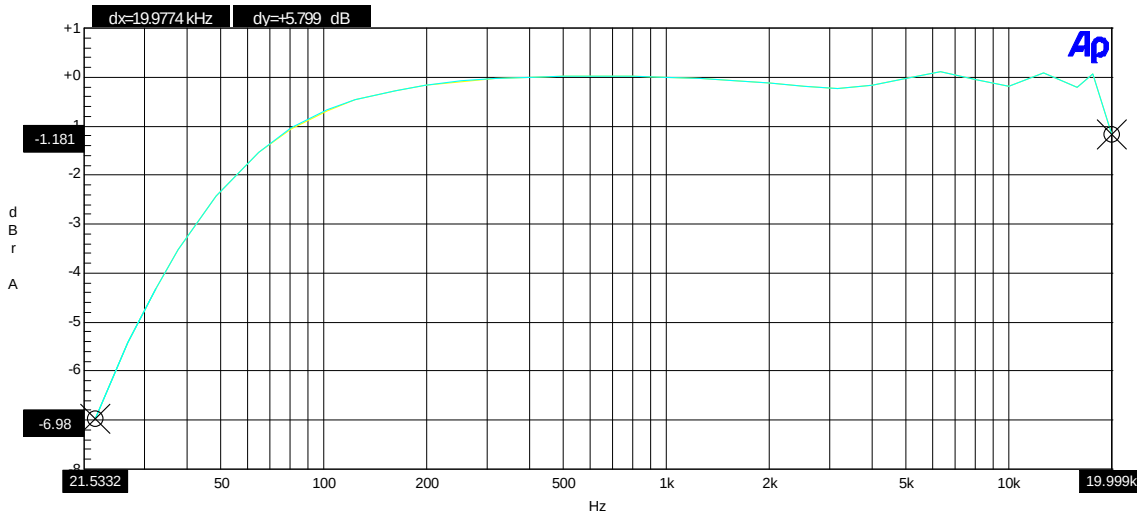


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Cyan	Solid	1	Fasttest.Ch.1 Ampl!Normalize	Left		-1.216 dBr A	-8.597 dBr A
1	2	Yellow	Solid	1	Fasttest.Ch.2 Ampl!Normalize	Left		*-1.214 dBr A	*-8.594 dBr A

Vista-Frequency Response-M48k.at27

9.4.2 Frequency Response 44.1Ks/Sec (8 Ohm Loading)

Audio Precision 08/09/06 18:00:37



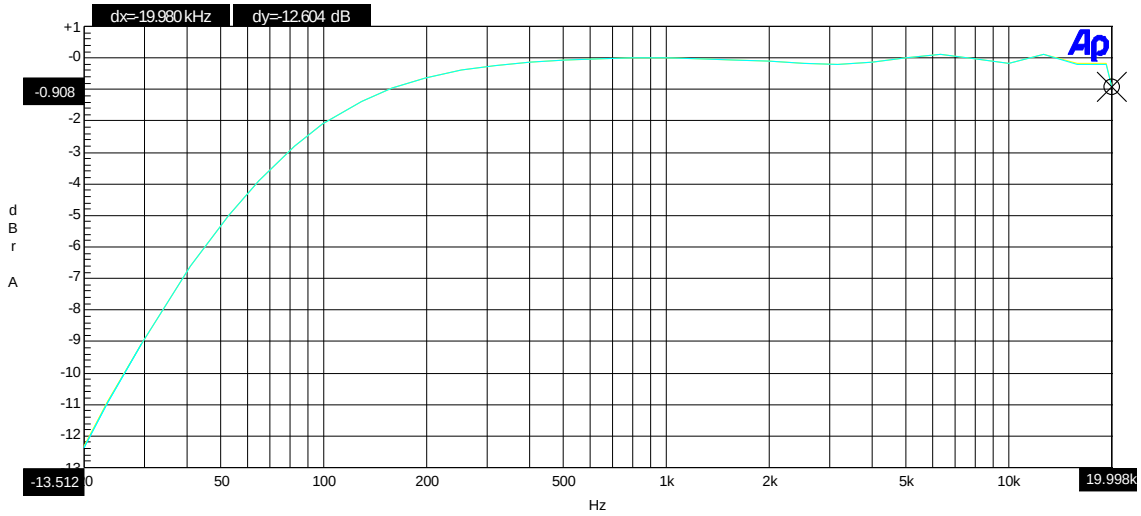
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Cyan	Solid	1	Fasttest.Ch.1 Ampl!Normalize	Left		*-6.980 dBr A	*-1.181 dBr A
1	2	Yellow	Solid	1	Fasttest.Ch.2 Ampl!Normalize	Left		-6.977 dBr A	-1.179 dBr A

Vista-Frequency Response-M44k.at27

9.5 Digital Playback for Line Output Frequency (4 Ohm Loading)

9.5.1 Frequency Response 48Ks/Sec (4 Ohm Loading)

Audio Precision 08/09/06 17:39:57

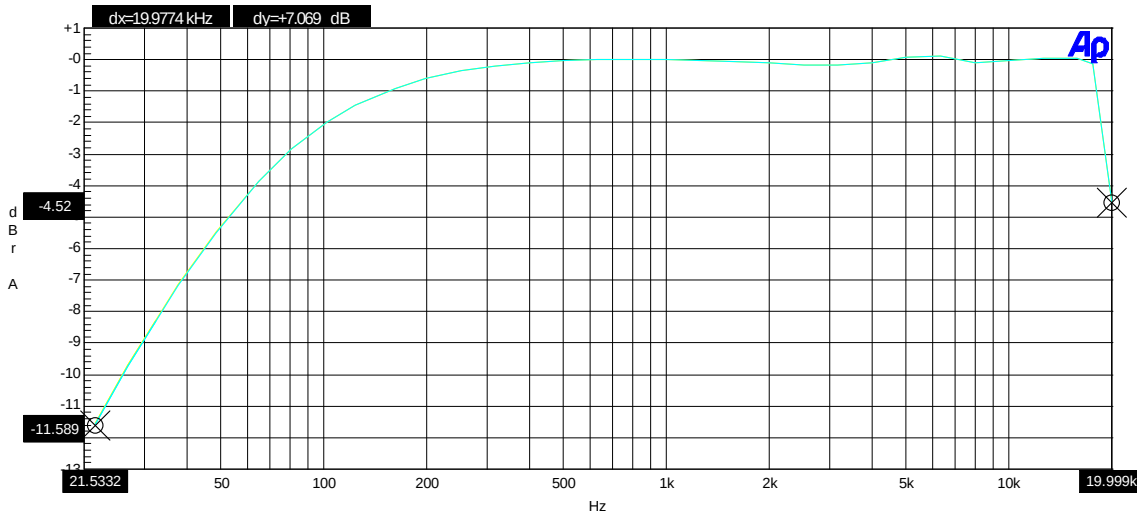


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Cyan	Solid	1	Fasttest.Ch.1 Ampl!Normalize	Left		*-0.908 dBr A	*-13.512 dBr A
1	2	Yellow	Solid	1	Fasttest.Ch.2 Ampl!Normalize	Left		-0.904 dBr A	-13.481 dBr A

Vista-Frequency Response-M48k.at27

9.5.2 Frequency Response 44.1Ks/Sec (4 Ohm Loading)

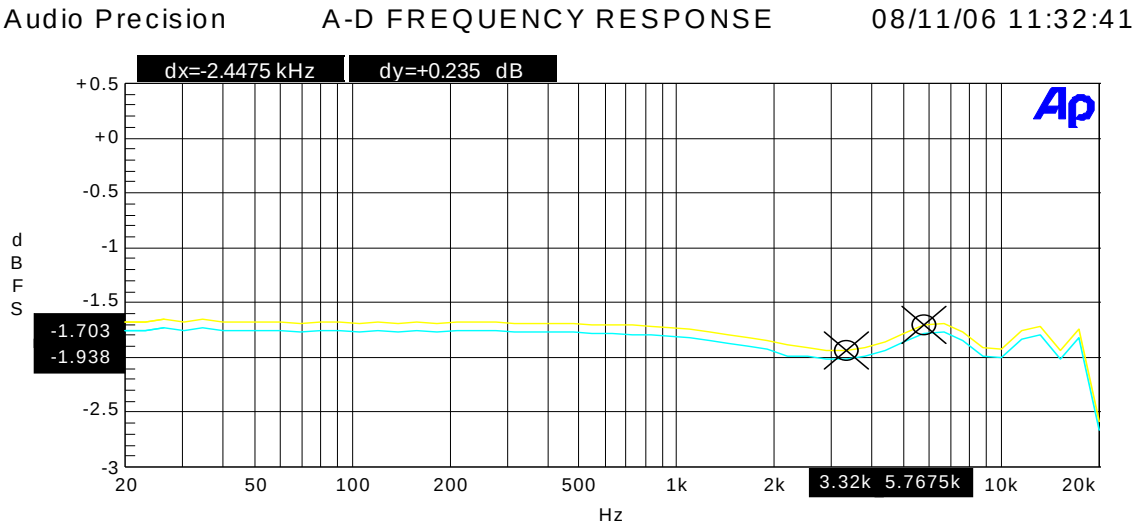
Audio Precision 08/09/06 17:52:58



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Cyan	Solid	1	Fasttest.Ch.1 Ampl!Normalize	Left		*-11.589 dBr A	*-4.520 dBr A
1	2	Yellow	Solid	1	Fasttest.Ch.2 Ampl!Normalize	Left		-11.559 dBr A	-4.516 dBr A

Vista-Frequency Response-M44k.at27

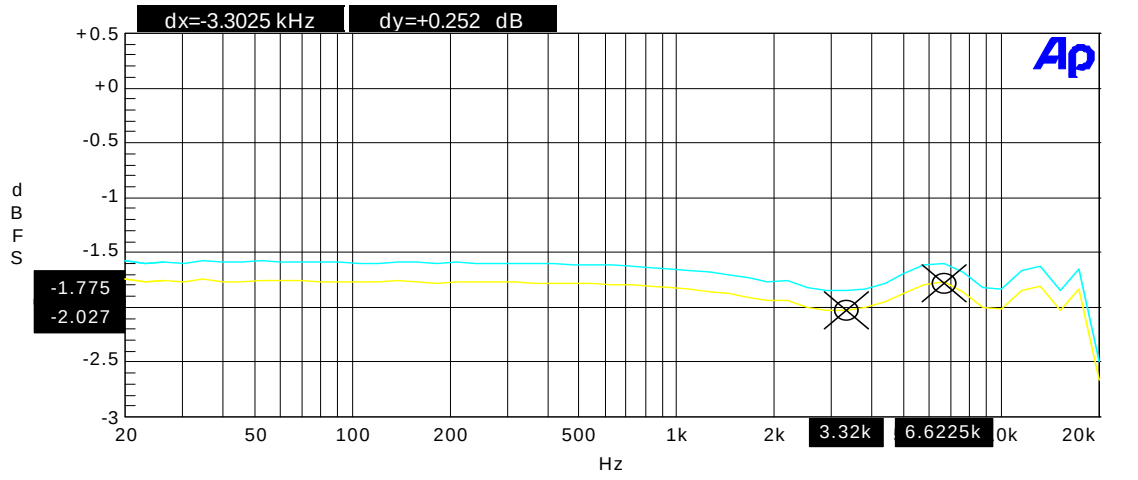
9.6 ADC (LINE IN) FREQUENCY RESPONSE



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1
1	1	Yellow	Solid	1	DSP Anlr.Level A	Left		*-1.703 dBFS
1	2	Cyan	Solid	1	DSP Anlr.Level B	Left		-1.782 dBFS

Vista-A-D Frequency Response.at2c

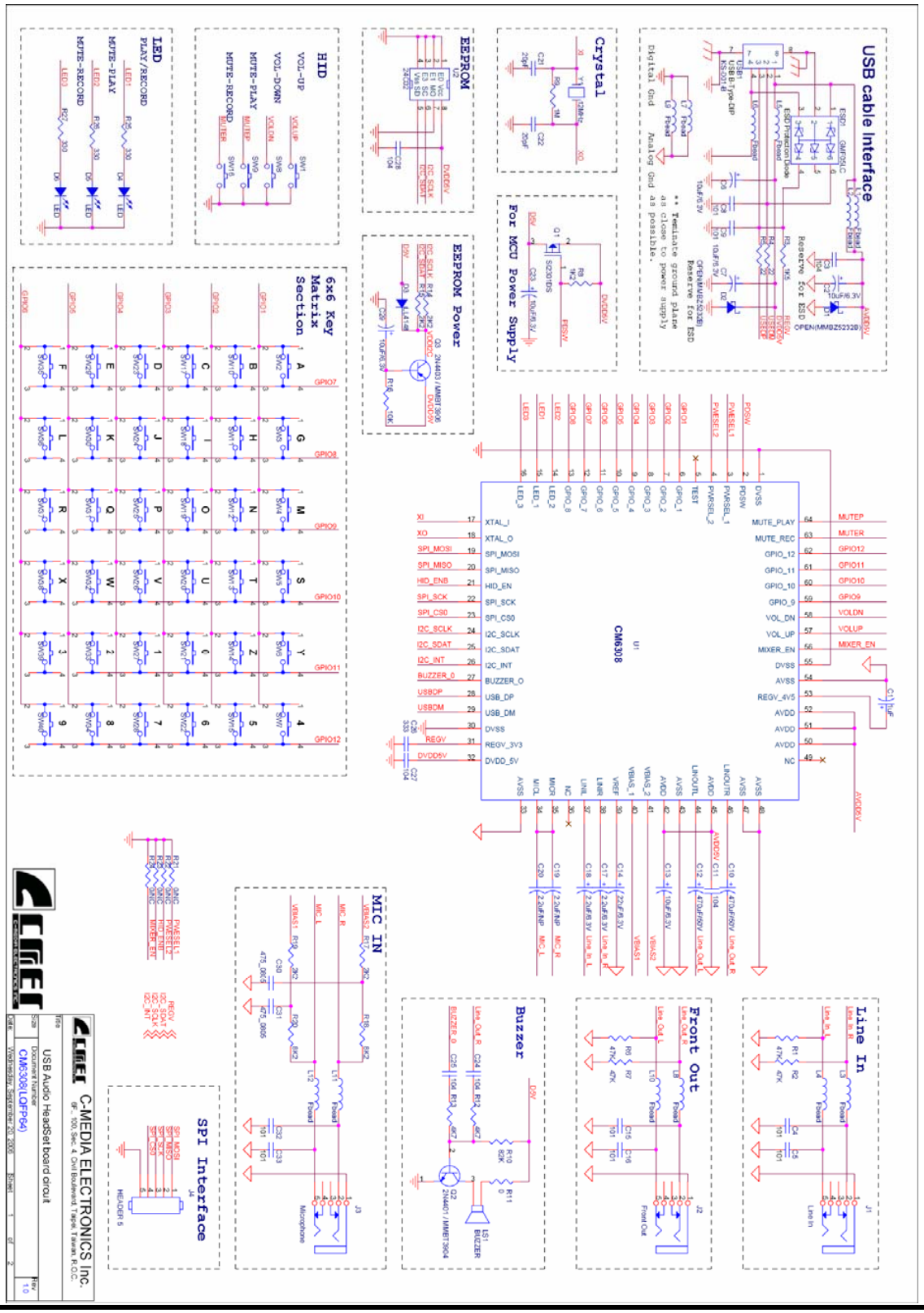
9.7 ADC (MIC IN) FREQUENCY RESPONSE

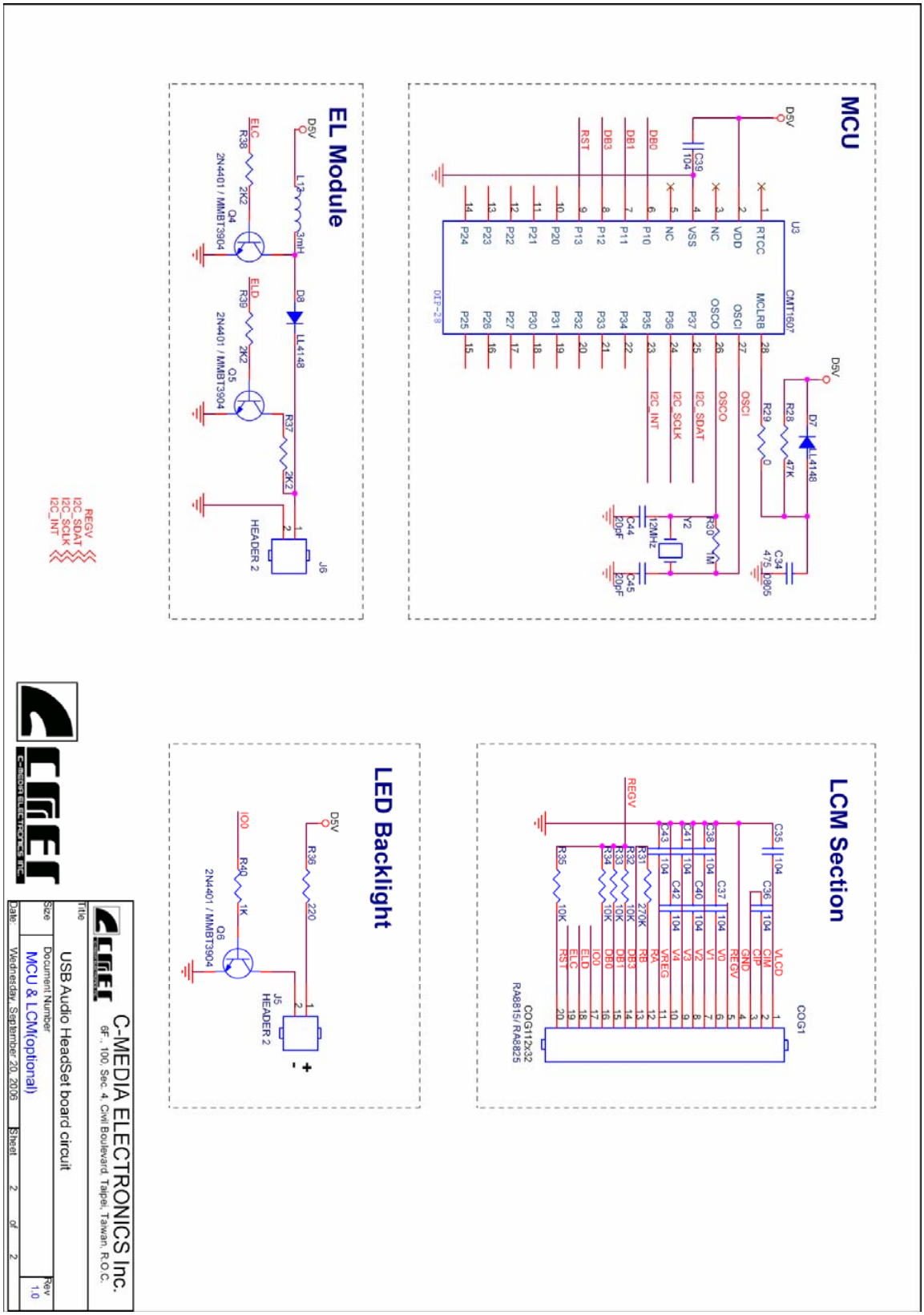


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1
1	1	Yellow	Solid	1	DSP Anlr.Level A	Left		*-1.775 dBFS
1	2	Cyan	Solid	1	DSP Anlr.Level B	Left		-1.600 dBFS

Vista-A-D Frequency Response.at2c

10. APPLICATION CIRCUIT REFERENCE





REFERENCE

USB-IF, USB Specification, Revision 1.1 and 2.0, and USB Audio Device Class Specification, Revision 1.0,.

— End of Specification —

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