SRAM

8K X 8 LOW POWER CMOS STATIC RAM

FEATURES

- High speed access time: 50/70/85/100ns
- Low power supply current :
  - Operating : 35mA(max)
  - Standby : 50uA
- Power supply : 5V (± 10%)
- Fully static operation – No clock or refreshing required
- All inputs and outputs directly LVTTL compatible
- Common I/O capability
- Data retention voltage : 1.5V (min)
- Available packages :
  28-pin DIP(600mil),SOJ, SOP,
  TSOP-I (8x13.4mm).
- Operating temperature : 0 ~ +70 °C

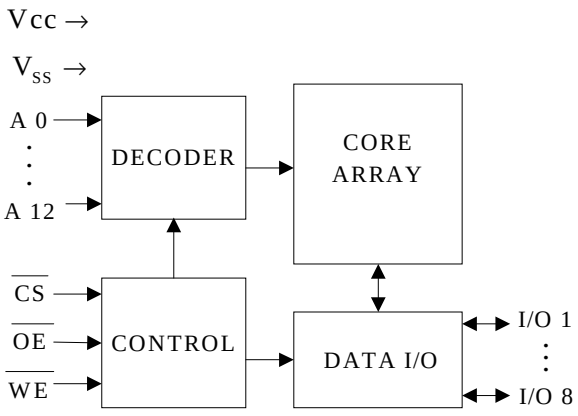
PART NUMBER EXAMPLES

PART NO.	PACKAGE CODE	ACCESS TIME
T15M64A-100N	N=DIP	100ns
T15M64A-100J	J=SOJ	
T15M64A-100D	D=SOP	
T15M64A-100P	P= TSOP-I	

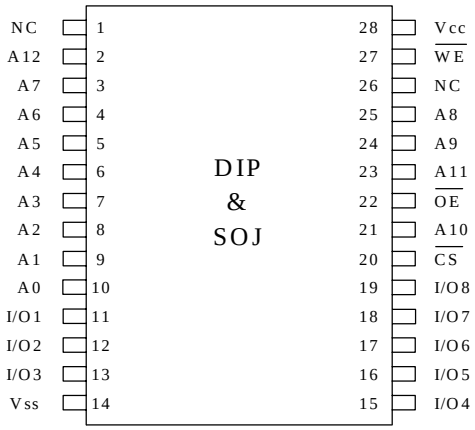
GENERAL DESCRIPTION

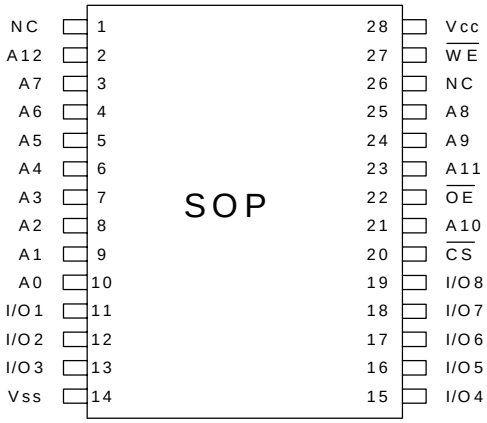
The T15M64A is a low power CMOS static RAM. organized as 8,192 x 8 bits that operates on a single 5-volt power supply. Low operating and standby current . Data retention is guaranteed at a power supply voltage as low as 1.5V. This device is packaged in a standard 28-pin DIP(600mil), SOJ, SOP, TSOP-I type.

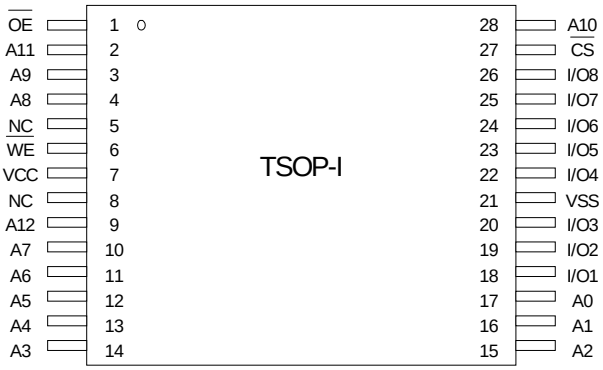
BLOCK DIAGRAM



PIN CONFIGURATION







PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A12	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
$\overline{CS}$	Chip Select Inputs
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc	Power Supply
Vss	Ground

DC CHARACTERISTICS ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply Voltage to Vss Potential	-0.5 to + 7V	V
Inputs to Vss Potential	-0.5 to Vcc +0.5	V
Power Dissipation	0.7	W
Storage Temperature	-60 to +150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYM	MIN	TYP	MAX	UNIT
Supply Voltage	Vcc	4.5	5	5.5	V
Input Voltage, low	V_{IL}	-0.3	-	0.8	V
Input Voltage, high	V_{IH}	2.2	-	Vcc+0.3	V
Ambient Temperature	T_A	0	-	+70	°C

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O1- I/O8	Power
H	X	X	Not Selected	High-Z	Standby
L	H	H	Output Disable	High-Z	Active
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active

OPERATING CHARACTERISTICS

(Vcc = 5V / ± 10%, Vss = 0V, Ta = 0 ~ +70 °C)

PARAMETER	SYM.	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input Leakage Current	I_{LI}	Vin=Vss to Vcc		-	-	1	uA
Output Leakage Current	I_{LO}	$V_{I/O}$=Vss to Vcc , $\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}		-	-	1	uA
Output Low Voltage	V_{OL}	I_{OL} = + 2.1mA		-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = - 1.0mA		2.4	-	-	V
Operating Power Supply Current	Icc	$\overline{CS}$ = V_{IL}, I/O=0mA Cycle = MIN. Duty = 100%	-50	-	-	35	mA
			-70	-	-	30	mA
			-85	-	-	25	mA
			-100	-	-	20	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, Cycle=min, Duty=100%		-	-	0.3	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC}-0.2V		-	-	50	uA

CAPACITANCE

(Vcc = 5V / ± 10%, Ta = 25°C, f = 1 MHz)

PARAMETER	SYMBOL	CONDITION	MAX.	UNIT
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pF
Input/ Output Capacitance	$C_{I/O}$	V_{OUT}= 0V	8	pF

Note: These parameters are sampled but not 100% tested.

AC TEST CONDITIONS

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3 ns
Input and Output Timing Reference Level	1.5V
Output Load	See Fig. 1,2

AC TEST LOADS AND WAVEFORM

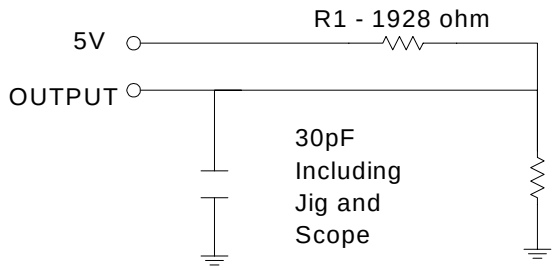
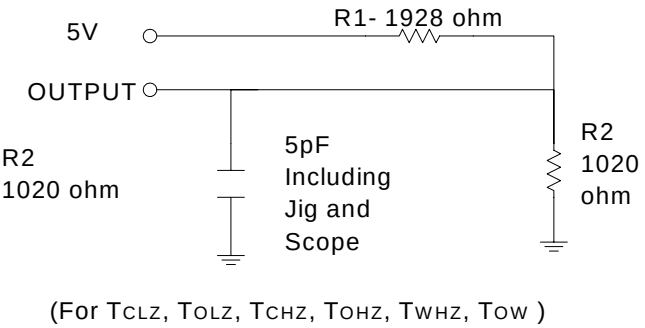


Fig 1



(For TCLZ, TOLZ, TCHZ, TOHZ, TWHZ, TOW)

Fig 2

AC CHARACTERISTICS

(V_{CC}= 5V / ± 10%, Vss = 0V, Ta =0 ~ +70 °C)

(1) READ CYCLE

PARAMETER	SYM.	-50ns		-70ns		-85ns		-100ns		UNIT
		MIN	MAX	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	tRC	50	-	70	-	85	-	100	-	ns
Address Access Time	tAA	-	50	-	70	-	85	-	100	ns
Chip Select Access Time	tACS	-	50	-	70	-	85	-	100	ns
Output Enable to Output Valid	tAOE	-	25	-	35	-	40	-	50	ns
Chip Selection to Output in Low Z	tCLZ*	7	-	10	-	10	-	10	-	ns
Output Enable to Output in Low Z	tOLZ*	5	-	5	-	5	-	5	-	ns
Chip Deselection to Output in High Z	tCHZ*	-	20	-	25	-	30	-	30	ns
Output Disable to Output in High Z	tOHZ*	-	20	-	25	-	30	-	30	ns
Output Hold from Address Change	tOH	10	-	10	-	10	-	10	-	ns

* These parameters is measured with 5pF test load.

(2)WRITE CYCLE

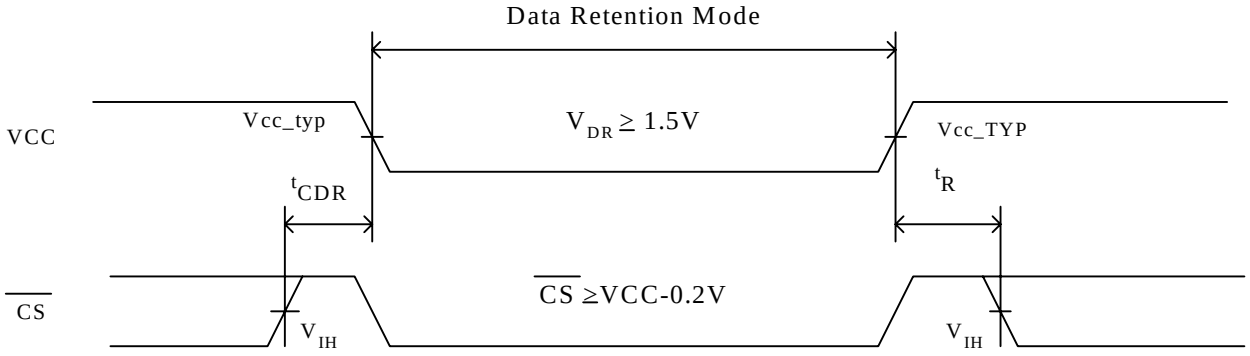
PARAMETER	SYM.	-50ns		-70ns		-85ns		-100ns		UNIT
		MIN	MAX	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	tWC	50	-	70	-	85	-	100	-	ns
Chip Selection to End of Write	tCW	40	-	60	-	70	-	80	-	ns
Address Valid to End of Write	tAW	40	-	60	-	70	-	80	-	ns
Address Setup Time	tAS	0	-	0	-	0	-	0	-	ns
Write Pulse Width	tWP	30	-	50	-	60	-	70	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	0	-	ns
Data Valid to End of Write	tDW	25	-	30	-	35	-	40	-	ns
Data Hold from End of Write	tDH	0	-	0	-	0	-	0	-	ns
Write to Output in High Z	tWHZ*	-	20	-	25	-	30	-	30	ns
Output Active from End of Write	tOW	5	-	5	-	5	-	5	-	ns

* These parameters is measured with 30pF test load.

DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	max	unit
Vcc for data retention	V_{DR}	$\overline{CS} \geq V_{CC}$-0.2V	1.5	-	-	V
Data retention current	I_{DR}	V_{CC}=5.0, $\overline{CS} \geq V_{CC}$-0.2V	-		50	uA
Data retention set-up time	t_{CDR}	See data retention waveform	0	-	-	ms
Recovery time	t_R		5	-	-	

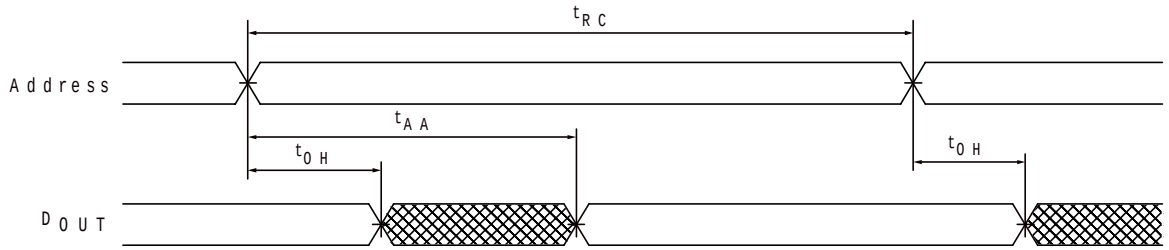
DATA RETENTION WAVE FORM



TIMING WAVEFORMS

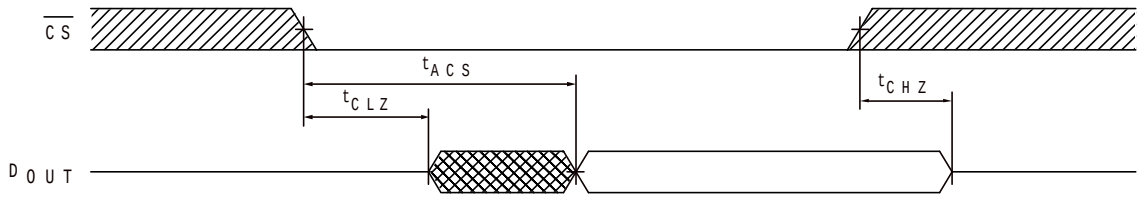
READ CYCLE 1

(Address Controlled)



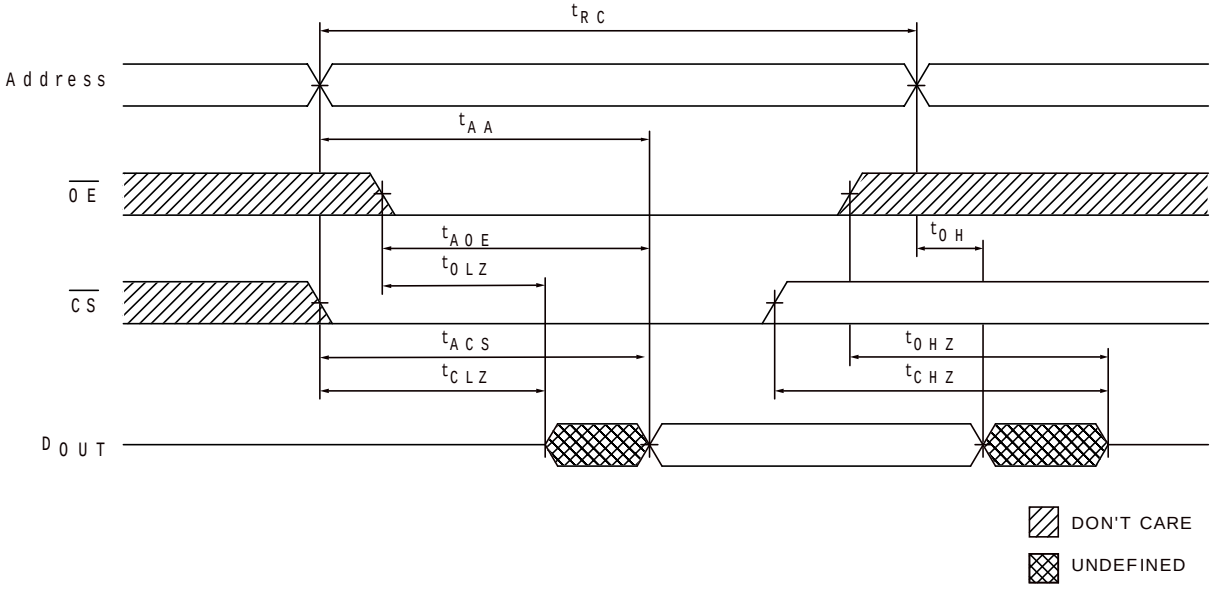
READ CYCLE 2

(Chip Select Controlled)

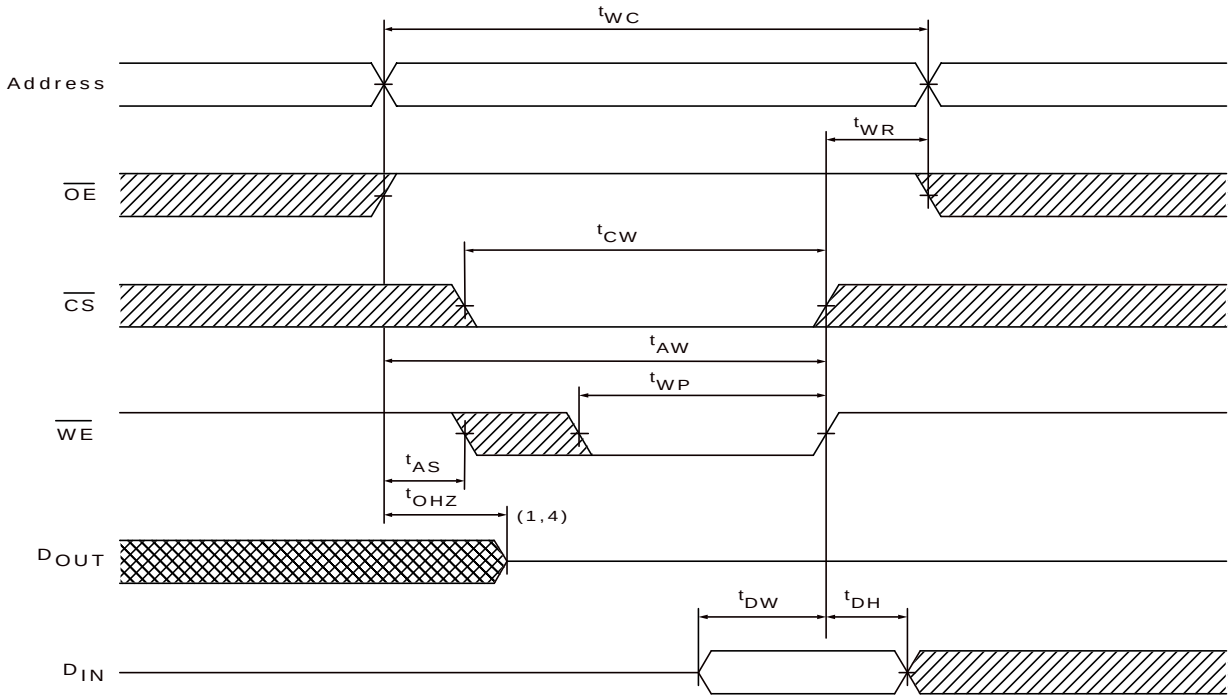


READ CYCLE 3

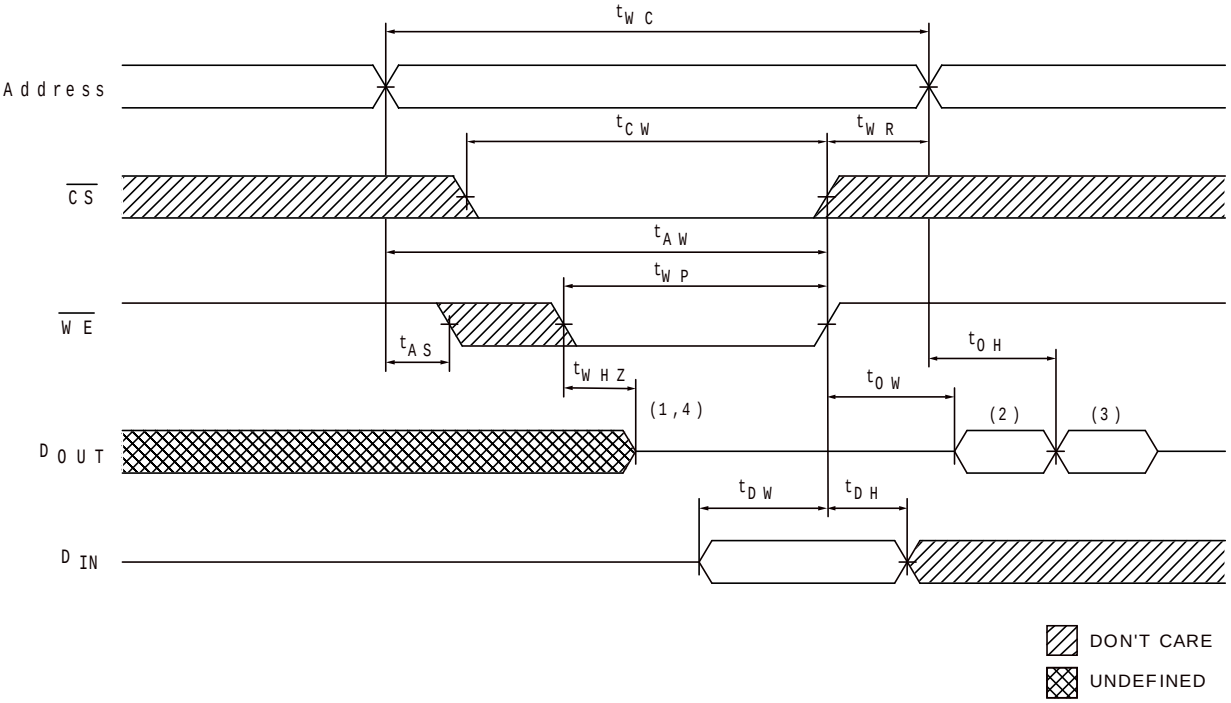
(Output Enable Controlled)



WRITE CYCLE 1 ($\overline{OE}$ CLOCK)



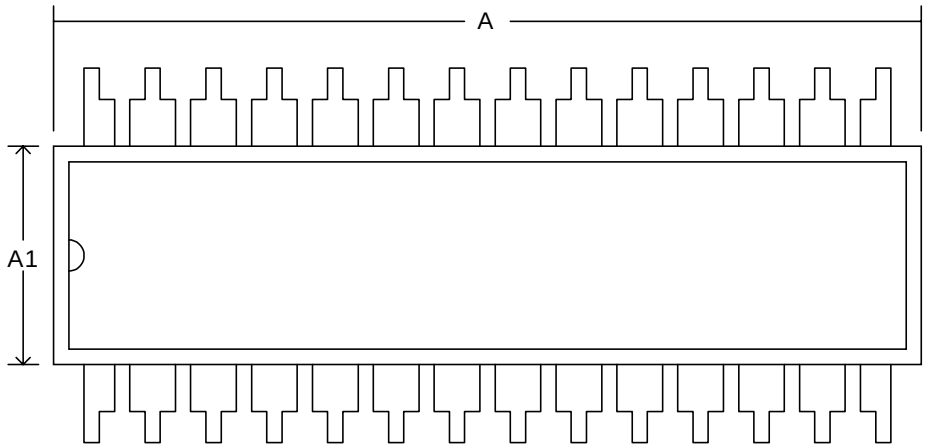
WRITE CYCLE 2 ($\overline{OE}$ = V_{IL} Fixed)

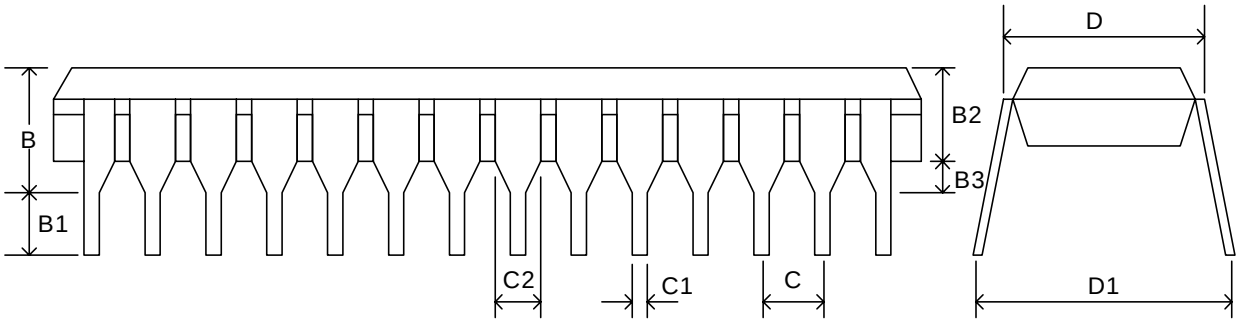


Notes: 1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.

2. The data output from D_{OUT} are the same as the data written to D_{IN} during the write cycle.
3. D_{OUT} provides the read data for the next address.
4. Transition is measured ± 500 mV from steady state with C_L = 5pF. This parameter is guaranteed but not 100% tested.
5. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

PACKAGE DIMENSIONS
28-LEAD DIP SRAM (600 mil)

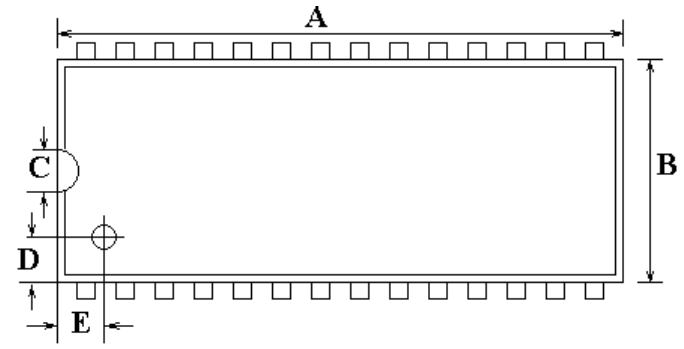


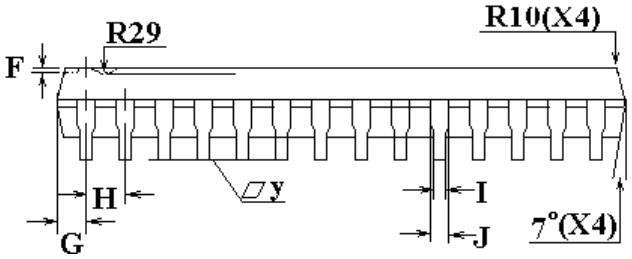


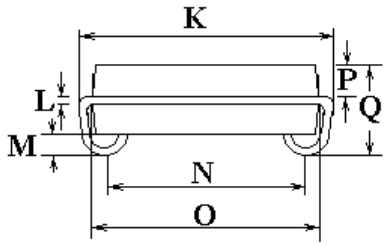
Symbol	Dimension in inches			Dimension in mm		
	min.	typ.	max	min.	typ.	max.
A	1.440	1.450	1.460	36.58	36.83	37.08
A1	0.546	0.550	0.554	13.87	13.97	14.07
B	-	0.210	-	-	5.33	-
B1	0.100	-	-	2.54	-	-
B2	0.140	0.150	0.160	3.56	3.81	4.06
B3	0.015	-	-	0.38	-	-
C	-	0.100	-	-	2.54	-
C1	0.016	0.018	0.020	0.41	0.46	0.51
C2	-	0.060	-	-	1.52	-
D	0.600	0.612	0.624	15.24	15.54	15.85
D1	0.630	0.650	0.670	16.0	16.51	17.0

PACKAGE DIMENSIONS

28-LEAD SOJ SRAM (300 mil)

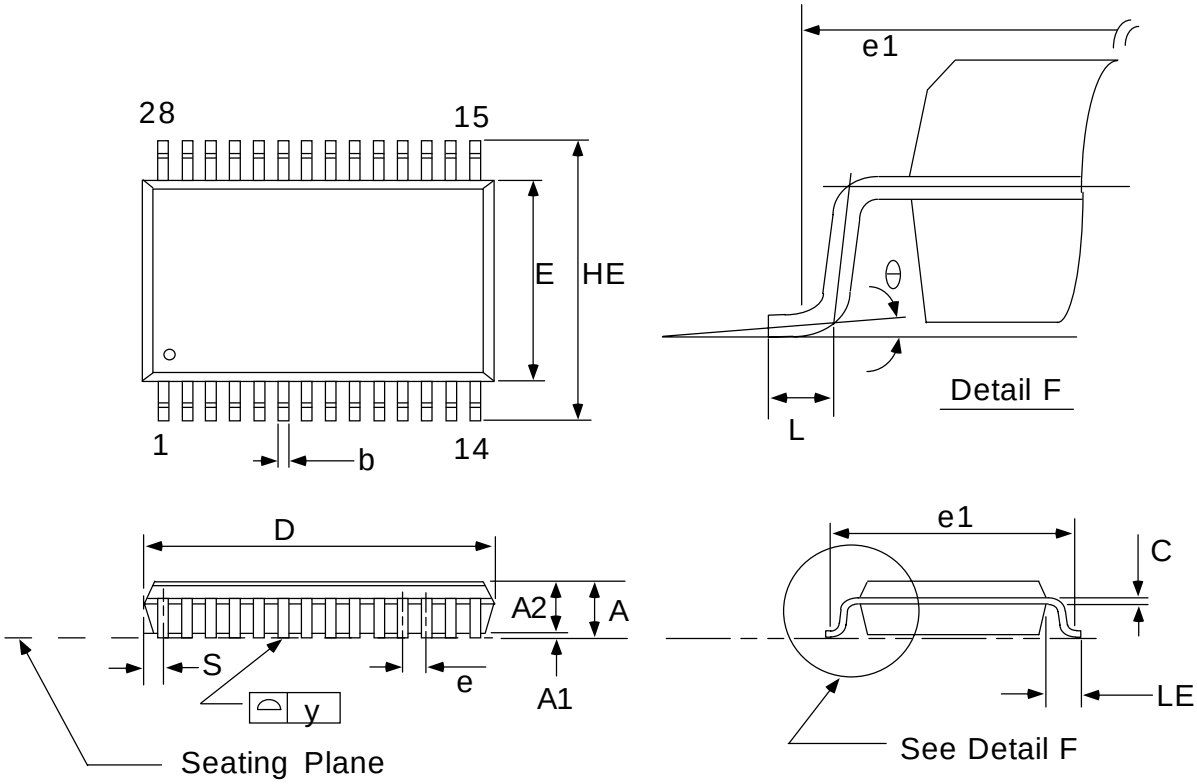






SYMBOL	DIMENSIONS IN INCHES	DIMENSIONS IN MM
A	0.710±0.002	18.03±0.05
B	0.300±0.005	7.62±0.13
C	0.060±0.002	1.52±0.05
D	0.050±0.001	1.27±0.03
E	0.063±0.001	1.63±0.03
F	0.015±0.002	0.38±0.05
G	0.030±0.002	0.76±0.05
H	0.050±0.002	1.27±0.05
I	0.018±0.002	0.46±0.05
J	0.028±0.002	0.71±0.05
K	0.337±0.002	8.56±0.05
L	0.010±0.001	0.25±0.03
M	0.026±0.002	0.66±0.05
N	0.268±0.003	6.81±0.08
O	0.300±0.002	7.62±0.05
P	0.053±0.001	1.35±0.03
Q	0.140±0.004	3.56±0.10
y	0.004(MAX)	0.10(MAX)

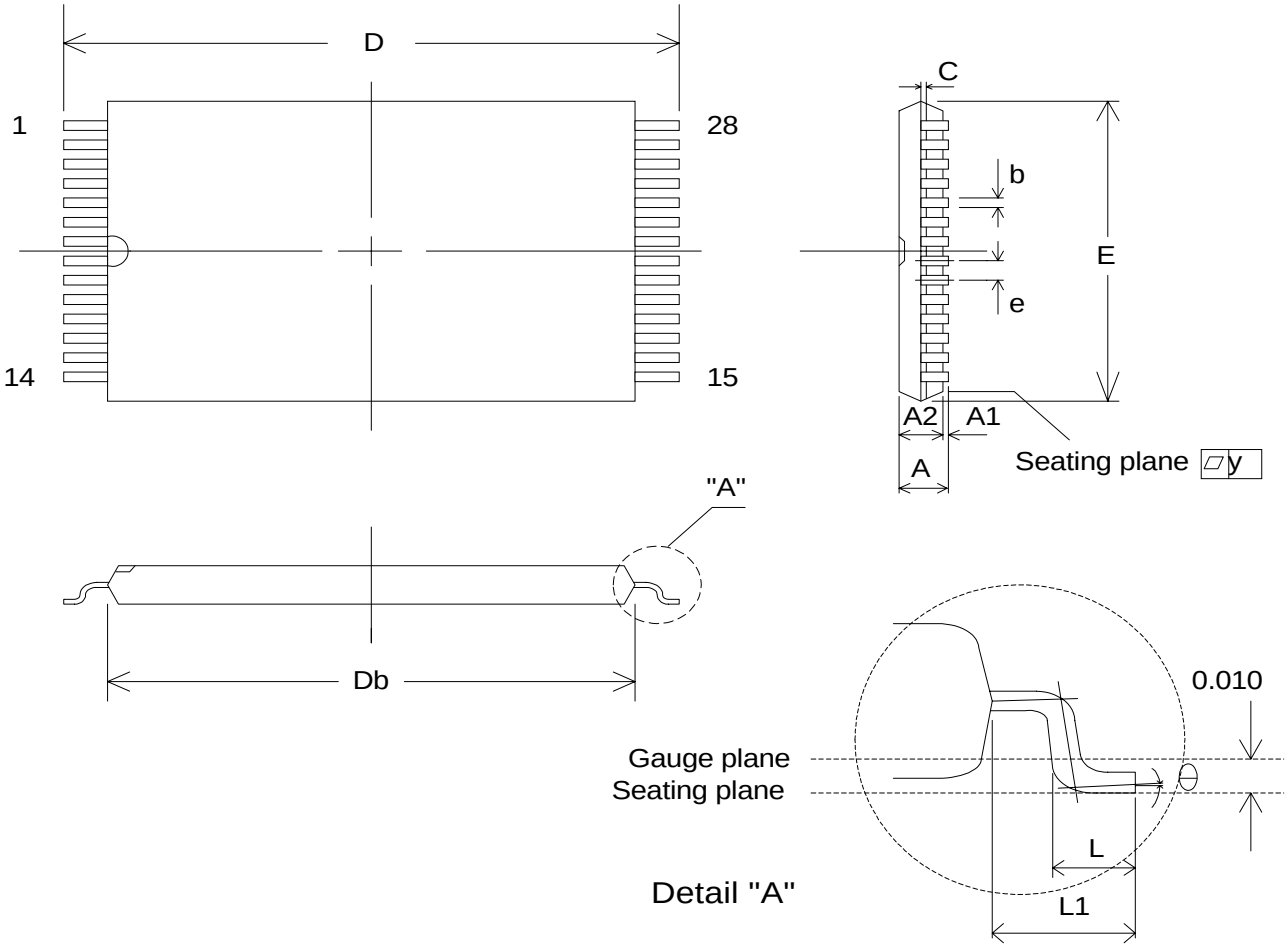
PACKAGE DIMENSIONS
28-LEAD SOP



Symbol	Dimension in inches			Dimension in mm		
	min.	typ.	max	min.	typ.	max.
A	-	-	0.112	-	-	2.845
A1	0.004	-	-	0.102	-	-
A2	0.093	0.098	0.103	2.362	2.489	2.616
b	0.014	0.016	0.020	0.335	0.406	0.508
C	0.008	0.010	0.014	0.203	0.254	0.356
D	-	0.713	0.733	-	18.110	18.618
E	0.326	0.331	0.336	8.280	8.407	8.534
e	0.044	0.050	0.056	1.118	1.270	1.422
HE	0.453	0.465	0.477	11.506	11.811	12.116
L	0.028	0.036	0.044	0.711	0.914	1.117
LE	0.059	0.067	0.075	1.499	1.702	1.905
S	-	39	-	-	1.0	-
y	-	-	0.004	-	-	0.102
θ	0°	-	10°	0°	-	10°

Notes :
1. Dimensions D max. & S include mold flash or tie bar burrs.
2. Dimension b does not include dambar protrusion / intrusion.
3. Dimensions D & E include mold mismatch and determined at the mold parting line.
4. controlling dimension : inches
5. general appearance spec should be based on final visual inspection spec.

PACKAGE DIMENSIONS
28-LEAD TSOP-I (8X13.4mm)



SYMBOL	DIMENSIONS IN INCHES	DIMENSIONS IN MM
A	0.047(max.)	1.20(max.)
A1	0.004±0.002	0.10±0.05
A2	0.039±0.002	1.00±0.05
b	0.008(typ.)	0.20(typ.)
c	0.006(typ.)	0.15(typ.)
Db	0.465±0.004	11.80±0.10
E	0.315±0.004	8.00±0.10
e	0.022(typ.)	0.55(typ.)
D	0.528±0.008	13.40±0.20
L	0.020±0.004	0.50±0.10
L1	0.0315±0.004	0.80±0.10
y	0.004(max.)	0.10(max.)
θ	0°~5°	0°~5°