STGIPN3H60

SLLIMM™-nano (small low-loss intelligent molded module) IPM, 3 A - 600 V 3-phase IGBT inverter bridge

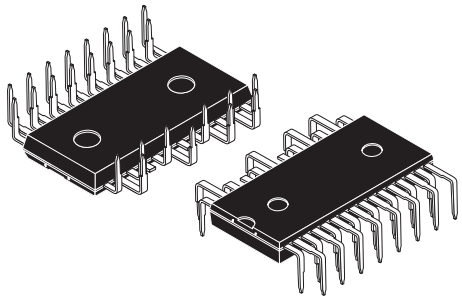
Preliminary data

Features

- IPM 3 A, 600 V, 3-phase IGBT inverter bridge including control ICs for gate driving and freewheeling diodes
- Optimized for low electromagnetic interference
- $V_{CE(sat)}$ negative temperature coefficient
- 3.3 V, 5 V, 15 V CMOS/TTL inputs comparators with hysteresis and pull down/pull up resistors
- Undervoltage lockout
- Internal bootstrap diode
- Interlocking function
- Shutdown function
- Comparator for fault protection against overtemperature and overcurrent
- Op amp for advanced current sensing
- Optimized pinout for easy board layout

Applications

- 3-phase inverters for motor drives
- Dish washers, refrigerator compressors, heating systems, air-conditioning fans, draining and recirculation pumps



NDIP-26L

Description

This intelligent power module implements a compact, high performance AC motor drive in a simple, rugged design. It is composed of six IGBTs with freewheeling diodes and three half-bridge HVICs for gate driving, providing low electromagnetic interference (EMI) characteristics with optimized switching speed. The package is optimized for thermal performance and compactness in built-in motor applications, or other low power applications where assembly space is limited. This IPM includes an operational amplifier, completely uncommitted, and a comparator that can be used to design a fast and efficient protection circuit. SLLIMM™ is a trademark of STMicroelectronics.

Table 1. Device summary

Order code	Marking	Package	Packaging
STGIPN3H60	GIPN3H60	NDIP-26L	Tube

Contents

1 Internal schematic diagram and pin configuration

Figure 1. Internal schematic diagram

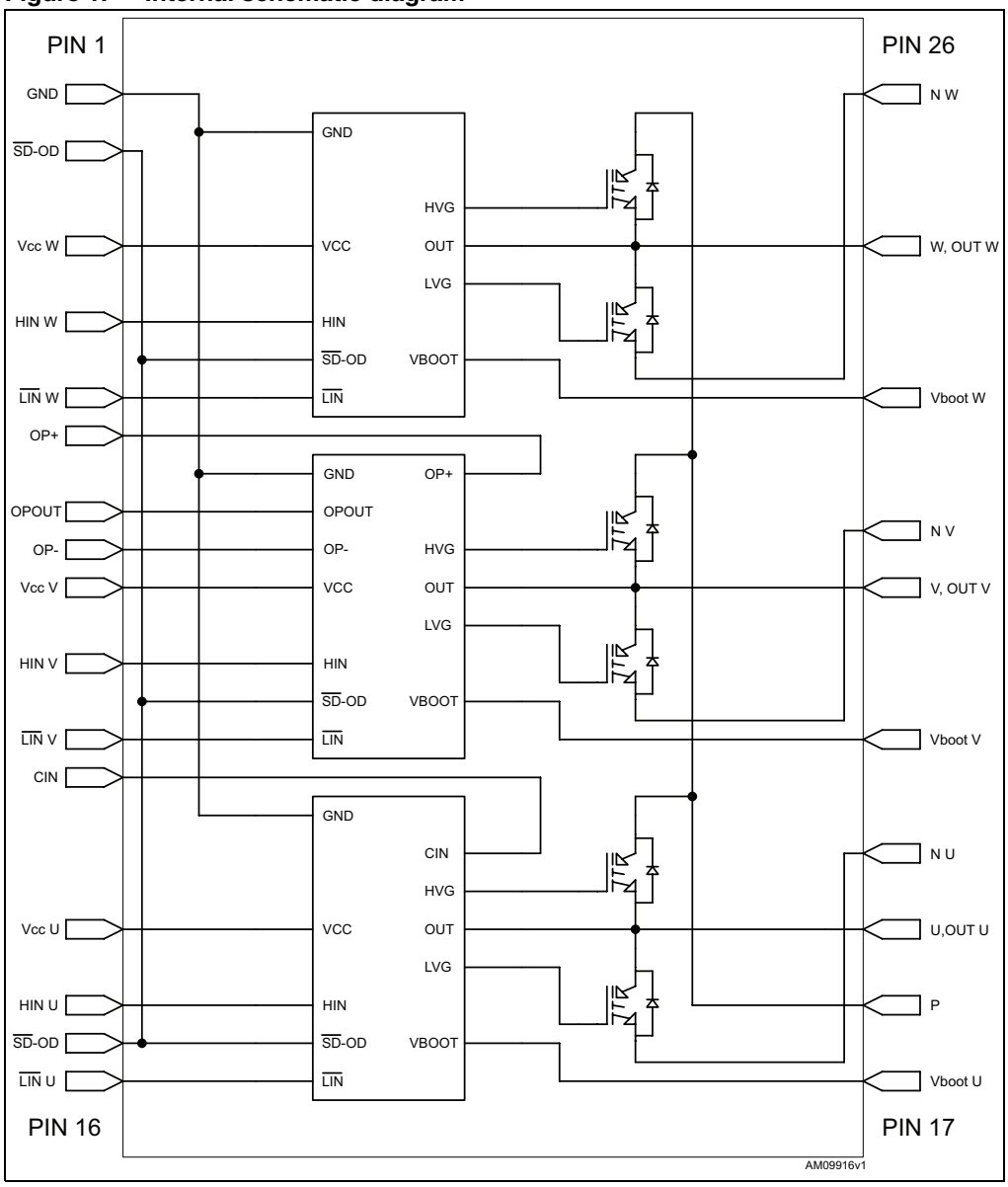
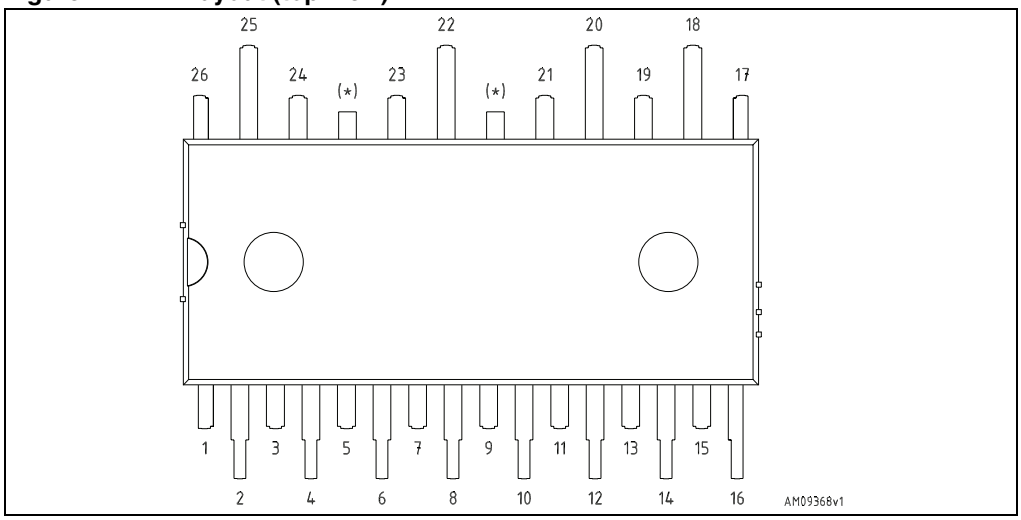


Table 2. Pin description

Pin	Symbol	Description
1	GND	Ground
2	$\overline{SD}$ / OD	Shut down logic input (active low) / open drain (comparator output)
3	V_{CC} W	Low voltage power supply W phase
4	HIN W	High side logic input for W phase
5	$\overline{LIN}$ W	Low side logic input for W phase
6	OP+	Op amp non inverting input
7	OP_{OUT}	Op amp output
8	OP-	Op amp inverting input
9	V_{CC} V	Low voltage power supply V phase
10	HIN V	High side logic input for V phase
11	$\overline{LIN}$ V	Low side logic input for V phase
12	CIN	Comparator input
13	V_{CC} U	Low voltage power supply for U phase
14	HIN U	High side logic input for U phase
15	$\overline{SD}$ / OD	Shut down logic input (active low) / open drain (comparator output)
16	$\overline{LIN}$ U	Low side logic input for U phase
17	V_{BOOT} U	Bootstrap voltage for U phase
18	P	Positive DC input
19	U, OUT_U	U phase output
20	N_U	Negative DC input for U phase
21	V_{BOOT} V	Bootstrap voltage for V phase
22	V, OUT_V	V phase output
23	N_V	Negative DC input for V phase
24	V_{BOOT} W	Bootstrap voltage for W phase
25	W, OUT_W	W phase output
26	N_W	Negative DC input for W phase

Figure 2. Pin layout (top view)



(*) Dummy pin internally connected to P (positive DC input).

2 Electrical ratings

2.1 Absolute maximum ratings

Table 3. Inverter part

Symbol	Parameter	Value	Unit
V_{CES}	Each IGBT collector emitter voltage (V_{IN} (1) = 0)	600	V
± I_C (2)	Each IGBT continuous collector current at T_C = 25°C	3	A
± I_{CP} (3)	Each IGBT pulsed collector current	TBD	A
P_{TOT}	Each IGBT total dissipation at T_C = 25°C	TBD	W

1. Applied between HIN_i, $\overline{LIN_i}$ and GND for i = U, V, W
2. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{j(max)} - T_C}{R_{thj-c} \times V_{CE(sat)(max)}(T_{j(max)}, I_C(T_C))}$$

3. Pulse width limited by max junction temperature

Table 4. Control part

Symbol	Parameter	Value	Unit
V_{OUT}	Output voltage applied between OUT_U, OUT_V, OUT_W - GND (V_{CC} = 15 V)	V_{boot} - 21 to V_{boot} + 0.3	V
V_{CC}	Low voltage power supply	-0.3 to +21	V
V_{CIN}	Comparator input voltage	-0.3 to V_{CC} +0.3	V
V_{boot}	Bootstrap voltage applied between $V_{boot\ i}$ - OUT_i for i = U, V, W	-0.3 to 620	V
V_{IN}	Logic input voltage applied between HIN, $\overline{LIN}$ and GND	-0.3 to 15	V
$V_{\overline{SD}/OD}$	Open drain voltage	-0.3 to 15	V

Table 5. Total system

Symbol	Parameter	Value	Unit
V_{ISO}	Isolation withstand voltage applied between each pin and heatsink plate (AC voltage, t = 60 sec.)	1000	V
T_j (1)	Operating junction temperature	-40 to 150	°C
T_C	Module case operation temperature	-40 to 125	°C

1. The maximum junction temperature rating of the power chips integrated within the NDIP module is 150°C (@$T_C \leq$ 100°C). To ensure safe operation of the NDIP module, the average junction temperature should be limited to $T_{j(avg)} \leq$ 125°C (@$T_C \leq$ 100°C).

2.2 Thermal data

Table 6. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	50	°C/W

3 Electrical characteristics

T_J = 25 °C unless otherwise specified.

Table 7. Inverter part

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{CC} = V_{boot}$ = 15 V, V_{IN}(1)= 0 - 5 V, I_C = 1 A	-	2.15	2.6	V
		$V_{CC} = V_{boot}$ = 15 V, V_{IN}(1)= 0 - 5 V, I_C = 1 A, T_J = 125 °C	-	1.65		
I_{CES}	Collector-cut off current (V_{IN}(1)= 0 “logic state”)	V_{CE} = 600 V, $V_{CC} = V_{Boot}$ = 15 V	-		250	µA
V_F	Diode forward voltage	V_{IN}(1) = 0 “logic state”, I_C = 1 A	-		1.7	V
Inductive load switching time and energy						
t_{on}	Turn-on time	V_{DD} = 300 V, $V_{CC} = V_{boot}$ = 15 V, V_{IN}(1) = 0 - 5 V, I_C = 1 A (see *Figure 4*)	-	275		ns
$t_{c(on)}$	Crossover time (on)		-	90		
t_{off}	Turn-off time		-	890		
$t_{c(off)}$	Crossover time (off)		-	125		
t_{rr}	Reverse recovery time		-	50		
E_{on}	Turn-on switching losses		-	18		µJ
E_{off}	Turn-off switching losses		-	13		

1. Applied between HIN_i, $\overline{LIN_i}$ and GND for i = U, V, W ($\overline{LIN}$ inputs are active-low).

Note: t_{ON} and t_{OFF} include the propagation delay time of the internal drive. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the internally given gate driving condition.

Figure 3. Switching time test circuit

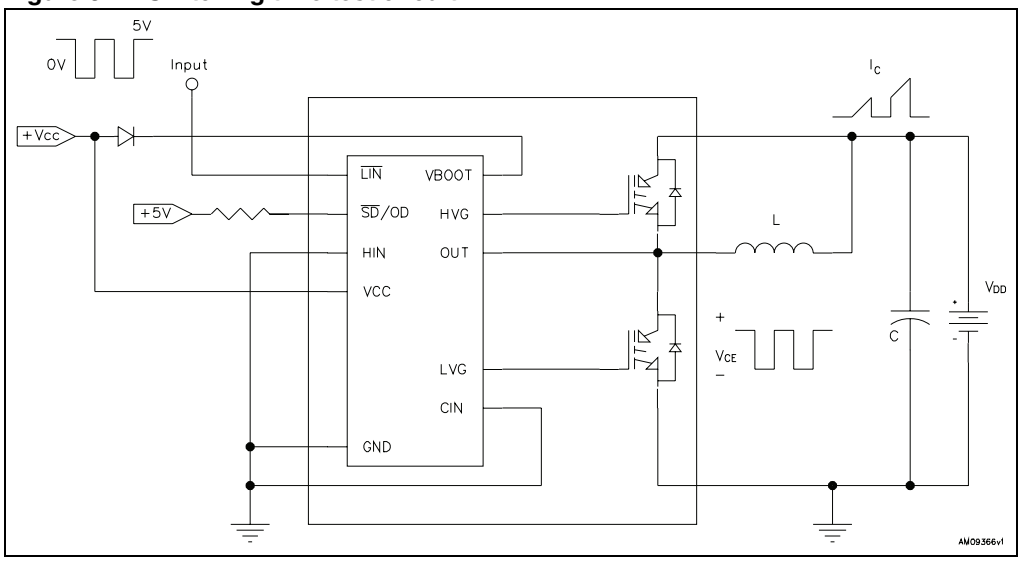
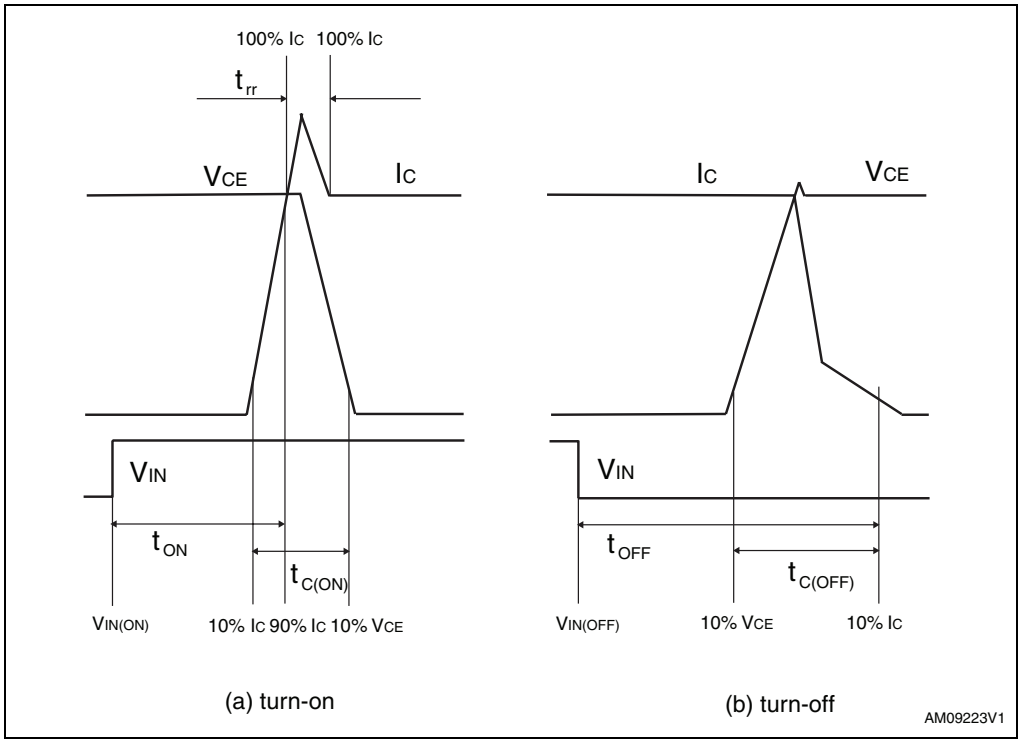


Figure 4. Switching time definition



Note: Figure 4 "Switching time definition" refers to HIN inputs (active high). For $\overline{LIN}$ inputs (active low), VIN polarity must be inverted for turn-on and turn-off.

3.1 Control part

Table 8. Low voltage power supply (V_{CC} = 15 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC_hys}	V_{CC} UV hysteresis		1.2	1.5	1.8	V
V_{CC_thON}	V_{CC} UV turn ON threshold		11.5	12	12.5	V
V_{CC_thOFF}	V_{CC} UV turn OFF threshold		10	10.5	11	V
I_{qccu}	Undervoltage quiescent supply current	V_{CC} = 10 V $\overline{SD}$/OD = 5 V; $\overline{LIN}$ = 5 V; HIN = 0, CIN = 0			150	µA
I_{qcc}	Quiescent current	V_{cc} = 15 V $\overline{SD}$/OD = 5 V; $\overline{LIN}$ = 5 V HIN = 0, CIN = 0			1	mA
V_{ref}	Internal comparator (CIN) reference voltage		0.5	0.54	0.58	V

Table 9. Bootstrapped voltage (V_{CC} = 15 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{BS_hys}	V_{BS} UV hysteresis		1.2	1.5	1.8	V
V_{BS_thON}	V_{BS} UV turn ON threshold		10.6	11.5	12.4	V
V_{BS_thOFF}	V_{BS} UV turn OFF threshold		9.1	10	10.9	V
I_{QBSU}	Undervoltage V_{BS} quiescent current	V_{BS} = 10 V $\overline{SD}$/OD = 5 V; $\overline{LIN}$ and HIN = 5 V; CIN = 0		70	110	µA
I_{QBS}	V_{BS} quiescent current	V_{BS} = 15 V $\overline{SD}$/OD = 5 V; $\overline{LIN}$ and HIN = 5 V; CIN = 0		150	210	µA
$R_{DS(on)}$	Bootstrap driver on resistance	LVG ON		120		Ω

Table 10. Logic inputs (V_{CC} = 15 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{il}	Low logic level voltage				0.8	V
V_{ih}	High logic level voltage		2.25			V
I_{HINh}	HIN logic “1” input bias current	HIN = 15 V	110	175	260	µA

Table 10. Logic inputs (V_{CC} = 15 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{HINl}	HIN logic “0” input bias current	HIN = 0 V			1	µA
I_{LINl}	$\overline{LIN}$ logic “1” input bias current	$\overline{LIN}$ = 0 V	3	6	20	µA
I_{LINh}	$\overline{LIN}$ logic “0” input bias current	$\overline{LIN}$ = 15 V			1	µA
I_{SDh}	$\overline{SD}$ logic “0” input bias current	$\overline{SD}$ = 15 V	30	120	300	µA
I_{SDl}	$\overline{SD}$ logic “1” input bias current	$\overline{SD}$ = 0 V			3	µA
Dt	Dead time	see *Figure 5*		180		ns

Table 11. OPAMP characteristics (V_{CC} = 15 V)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage	V_{ic} = 0 V, V_o = 7.5 V			6	mV
I_{io}	Input offset current	V_{ic} = 0 V, V_o = 7.5 V		4	40	nA
I_{ib}	Input bias current (1)			100	200	nA
V_{icm}	Input common mode voltage range		0			V
V_{OL}	Low level output voltage	R_L = 10 kΩ to V_{CC}		75	150	mV
V_{OH}	High level output voltage	R_L = 10 kΩ to GND	14	14.7		V
I_o	Output short circuit current	Source, V_{id} = +1; V_o = 0 V	16	30		mA
		Sink, V_{id} = -1; V_o = V_{CC}	50	80		mA
SR	Slew rate	V_i = 1 - 4 V; C_L = 100 pF; unity gain	2.5	3.8		V/µs
GBWP	Gain bandwidth product	V_o = 7.5 V	8	12		MHz
A_{vd}	Large signal voltage gain	R_L = 2 kΩ	70	85		dB
SVR	Supply voltage rejection ratio	vs. V_{CC}	60	75		dB
CMRR	Common mode rejection ratio		55	70		dB

1. The direction of input current is out of the IC.

Table 12. Sense comparator characteristics (V_{CC} = 15 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{ib}	Input bias current	V_{CP+} = 1 V	-		3	µA
V_{ol}	Open drain low level output voltage	I_{od} = - 3 mA	-		0.5	V
t_{d_comp}	Comparator delay	$\overline{SD}$/OD pulled to 5 V through 100 kΩ resistor	-	90	130	ns
SR	Slew rate	C_L = 180 pF; R_{pu} = 5 kΩ	-	60		V/µsec
t_{sd}	Shutdown to high / low side driver propagation delay	V_{OUT} = 0, V_{boot} = V_{CC}, V_{IN} = 0 to 3.3 V	50	125	200	ns
t_{isd}	Comparator triggering to high / low side driver turn-off propagation delay	Measured applying a voltage step from 0 V to 3.3 V to pin CIN_i	50	200	250	

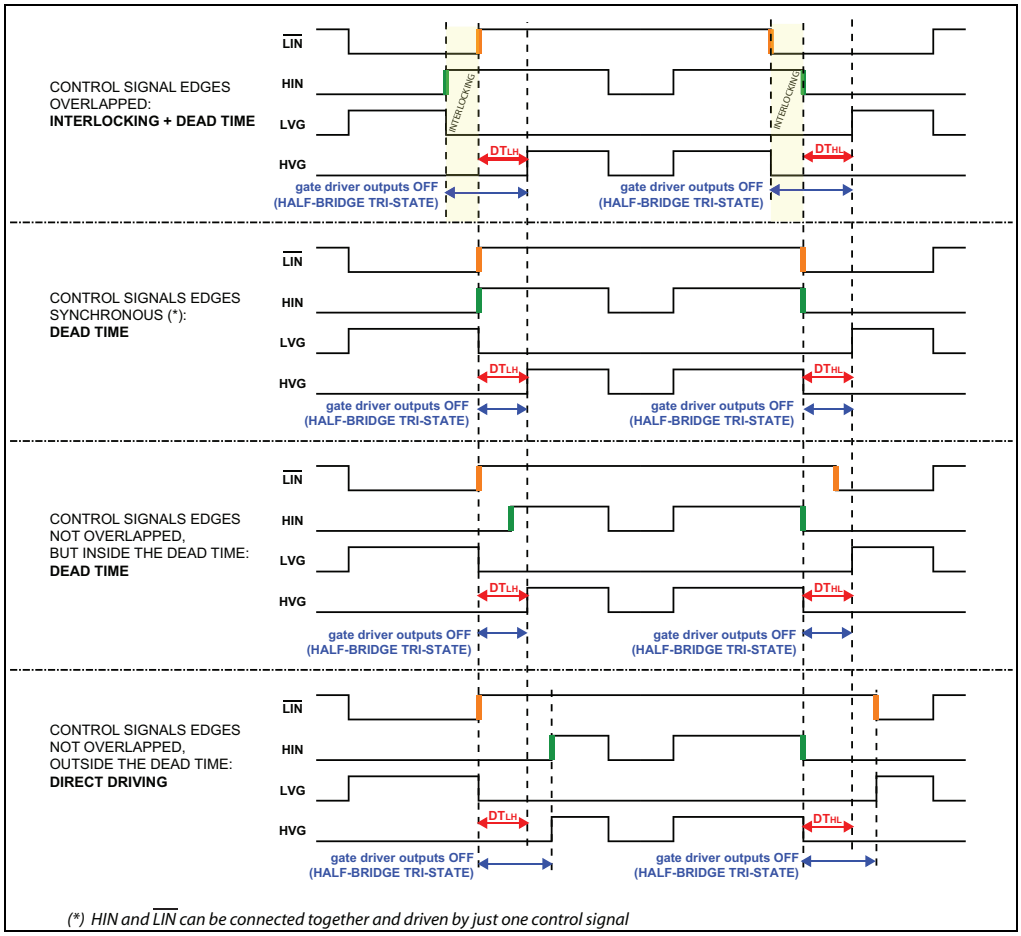
Table 13. Truth table

Condition	Logic input (V_I)			Output	
	$\overline{SD}$/OD	$\overline{LIN}$	HIN	LVG	HVG
Shutdown enable half-bridge tri-state	L	X	X	L	L
Interlocking half-bridge tri-state	H	L	H	L	L
0 “logic state” half-bridge tri-state	H	H	L	L	L
1 “logic state” low side direct driving	H	L	L	H	L
1 “logic state” high side direct driving	H	H	H	L	H

Note: X: don’t care

3.2 Waveform definitions

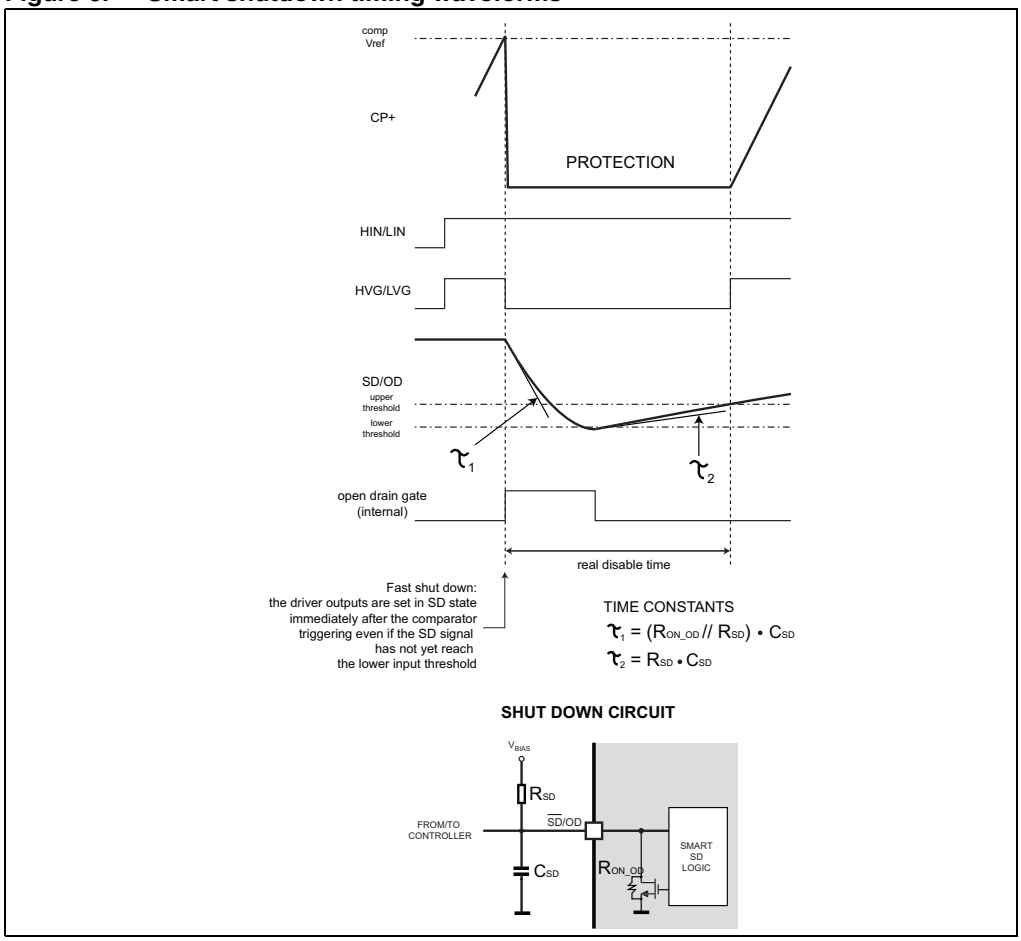
Figure 5. Dead time and interlocking waveform definitions



4 Smart shutdown function

The STGIPN3H60 integrates a comparator for fault sensing purposes. The comparator non-inverting input (CIN) can be connected to an external shunt resistor in order to implement a simple overcurrent protection function. When the comparator triggers, the device is set in shutdown state and both its outputs are set to low-level leading the half bridge in 3-state. In the common overcurrent protection architectures the comparator output is usually connected to the shutdown input through a RC network, in order to provide a mono-stable circuit, which implements a protection time that follows the fault condition. Our smart shutdown architecture allows to immediately turn-off the output gate driver in case of overcurrent, the fault signal has a preferential path which directly switches off the outputs. The time delay between the fault and the outputs turn-off is no more dependent on the RC values of the external network connected to the shutdown pin. At the same time the internal logic turns on the open-drain output and holds it on until the shutdown voltage goes below the logic input lower threshold. Finally the smart shutdown function provides the possibility to increase the real disable time without increasing the constant time of the external RC network.

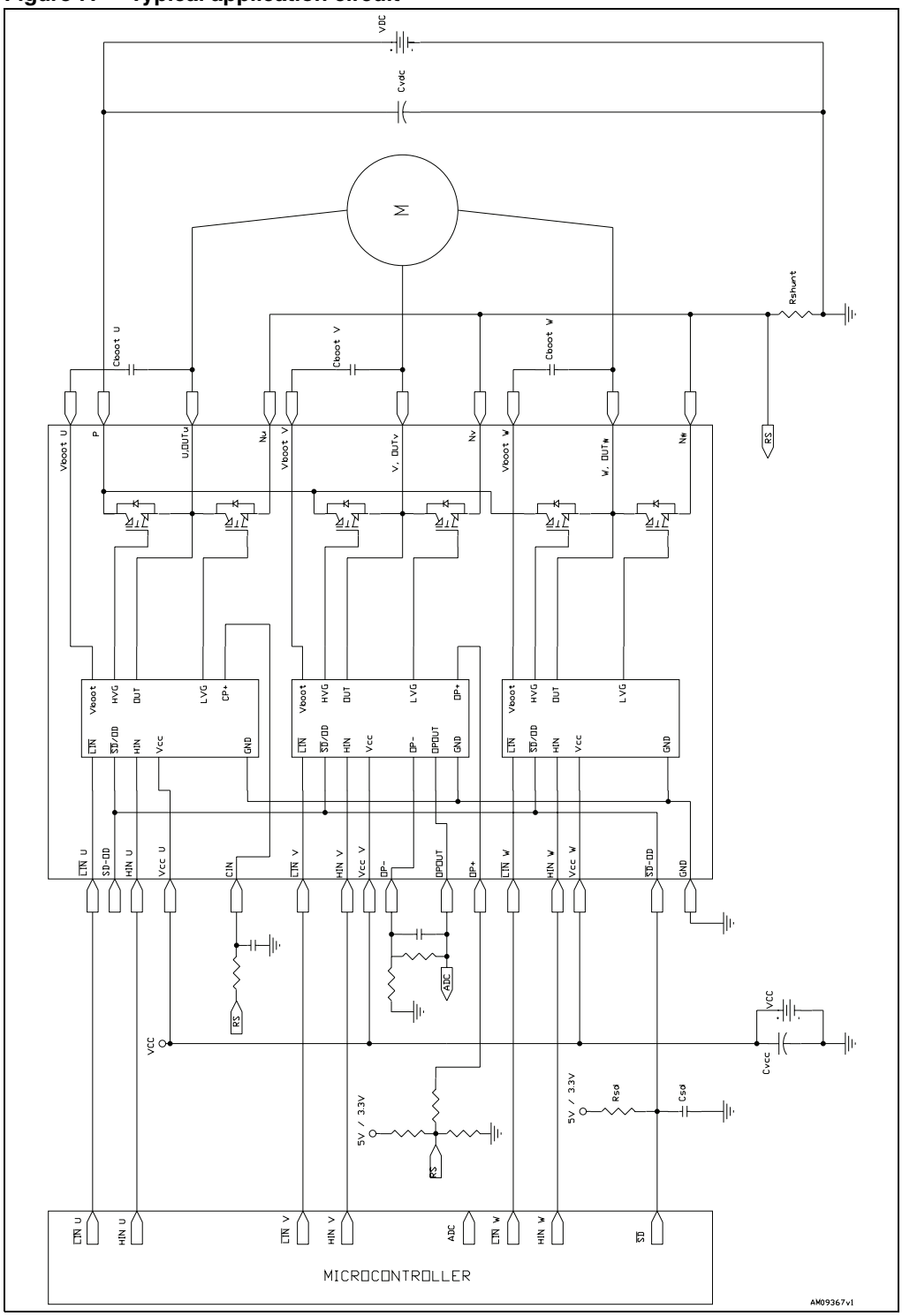
Figure 6. Smart shutdown timing waveforms



Please refer to *Table 12* for internal propagation delay time details.

5 Application information

Figure 7. Typical application circuit



5.1 Recommendations

- Input signal HIN is active high logic. An 85 kΩ (typ.) pull-down resistor is built-in for each high side input. If an external RC filter is used for noise immunity, attention should be given to the variation of the input signal level.
- Input signal $\overline{\text{LIN}}$ is active low logic. A 720 kΩ (typ.) pull-up resistor, connected to an internal 5 V regulator through a diode, is built-in for each low side input.
- To prevent input signal oscillation, the wiring of each input should be as short as possible.
- By integrating an application-specific type HVIC inside the module, direct coupling to the MCU terminals without an opto-coupler is possible.
- Each capacitor should be located as close as possible to the pins of the IPM.
- Low inductance shunt resistors should be used for phase leg current sensing.
- Electrolytic bus capacitors should be mounted as close to the module bus terminals as possible. Additional high frequency ceramic capacitors mounted close to the module pins will further improve performance.
- The $\overline{\text{SD}}$/OD signal should be pulled up to 5 V / 3.3 V with an external resistor (see *Section 4: Smart shutdown function* for detailed info).

6 Package mechanical data

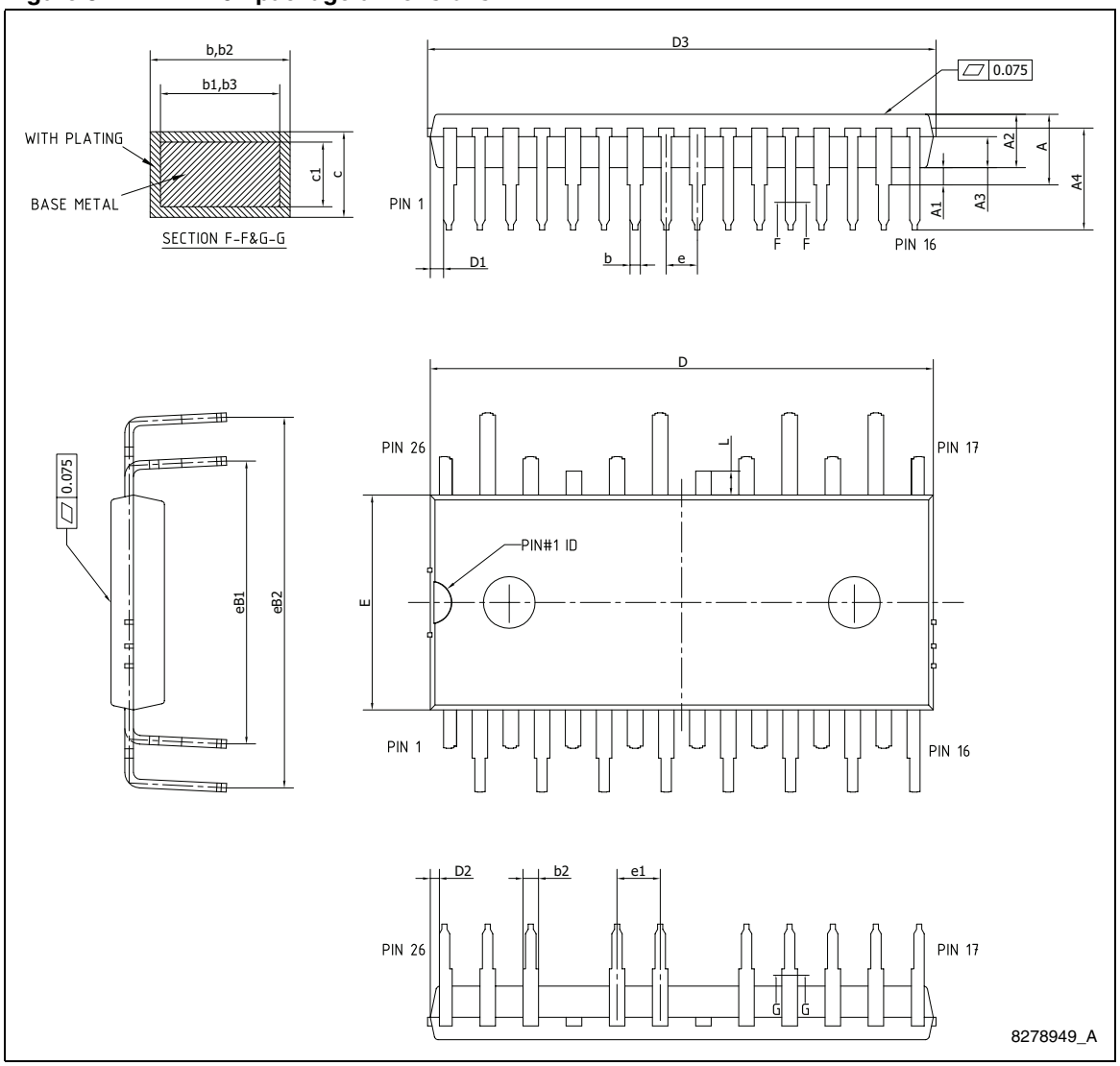
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Please refer to dedicated technical note TN0107 for mounting instructions.

Table 14. NDIP-26L mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A			4.40
A1	0.80	1.00	1.20
A2	3.00	3.10	3.20
A3	1.70	1.80	1.90
A4	5.70	5.90	6.10
b	0.53		0.72
b1	0.52	0.60	0.68
b2	0.83		1.02
b3	0.82	0.90	0.98
c	0.46		0.59
c1	0.45	0.50	0.55
D	29.05	29.15	29.25
D1	0.50		
D2	0.35		
D3			29.55
E	12.35	12.45	12.55
e	1.70	1.80	1.90
e1	2.40	2.50	2.60
eB1	16.10	16.40	16.70
eB2	21.18	21.48	21.78
L	1.24	1.39	1.54

Figure 8. NDIP-26L package dimensions



7 Revision history

Table 15. Document revision history

Date	Revision	Changes
23-Jun-2011	1	Initial release.

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