PIC24F16KA102 Family Silicon Errata and Data Sheet Clarification

The PIC24F16KA102 family devices that you have received conform functionally to the current Device Data Sheet (DS39927**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC24F16KA102 family silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A5**).

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device* and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the Output window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC24F16KA102 family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)
		A5
PIC24F08KA101	0B08h	05h
PIC24F08KA102	0B0Ah	
PIC24F16KA101	0B01h	
PIC24F16KA102	0B03h	

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses in program memory. They are shown in hexadecimal in the format, "DEVID DEVREV".

2: Refer to the *"PIC24FXXKAXXX Flash Programming Specification"* (DS39919) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)
				A5
CTMU	—	1.	Module operates in Sleep modes.	X
Resets	BOR	2.	Inadvertent Reset when disabling/enabling BOR.	X
Core	ICSP™	3.	Unable to use PGC/PGD pair under certain conditions.	X
Core	Deep Sleep	4.	Failure to avoid Deep Sleep entry.	X
Memory	Code Protection	5.	No direct jump to Boot Sector from Reset Vector.	X
Comparator	—	6.	Change in maximum VIOFF.	X
SPI	Enhanced Buffer mode	7.	Errors when polling SPITBF flag.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A5**).

1. Module: CTMU

The CTMU and its current source may continue to operate in Sleep mode. This results in current consumption in excess of the specifications for Sleep.

Work around

Clear the CTMU Enable bit (CTMUCON<15>) prior to entering Sleep mode.

Affected Silicon Revisions

A5							
X							

2. Module: Resets (BOR)

A device Reset may occur if the BOR is disabled and immediately re-enabled in software (RCON<14> is cleared, and then immediately set).

Work around

It is recommended that several NOP instructions be added to a BOR disable/enable sequence. Alternatively, place several instructions or a short routine between the instructions to disable and enable the BOR.

Affected Silicon Revisions

A5							
X							

3. Module: Core (ICSP™)

Under certain circumstances, a PGC/PGD pin pair may not function to enter ICSP Programming mode. This has been observed only when both the following conditions are met:

- Pin RA5 is configured as $\overline{\text{MCLR}}$ (FPOR<5> = 1), and
- The pins of the PGEC/PGED pair were configured as digital outputs (corresponding TRIS bit cleared) in software.

In these circumstances, the pins do not switch to a high-impedance state upon entry into Programming mode, but remain configured as outputs.

Work around

Choose a PGC/PGD pair with pins that are always configured as inputs (TRIS bits are set).

Affected Silicon Revisions

A5							
X							

4. Module: Core (Deep Sleep)

Deep Sleep wake-up sources may be ignored if they occur just prior to entry into Deep Sleep mode. As a result, the device may enter Deep Sleep mode when it should not.

Work around

If possible, configure external Deep Sleep wake-up sources to repeat themselves once. If the device does enter Deep Sleep, the second occurrence of the wake-up source will wake the device.

Alternatively, synchronize the entry into Deep Sleep with external wake-up sources, where possible.

Affected Silicon Revisions

A5							
X							

5. Module: Memory (Code Protection)

When any boot segment is enabled in program memory (FBS<3:1> ≠ 111), it is not possible to jump directly from the Reset vector to any address in the boot segment.

Work around

Point the Reset vector to an address in the general segment. From there, it is possible to jump into the boot segment.

Affected Silicon Revisions

A5							
X							

6. Module: Comparator

The maximum value for the input offset voltage (specification D300, VIOFF), shown in Table 29-13 of the Device Data Sheet, has changed for this silicon revision. The new value is shown in Table 3 (changes in **bold**).

Work around

None.

Affected Silicon Revisions

A5							
X							

7. Module: SPI (Enhanced Buffer Mode)

In Enhanced Buffer mode (SPI1CON2<0> = 1), polling the SPI Transmit Buffer Full bit, SPITBF (SPI1STAT<1>), may produce erroneous results. This occurs only under two circumstances:

- In Master mode, when the SPI divide clock is 4 or greater.
- In Slave mode, when the SPI sample clock is slower than 1/4 of the CPU instruction time (TCY).

For Master mode, this includes all combinations of the primary prescale bits (SPI11CON1<1:0>) and secondary prescale bits (SPI1CON1<4:2>) that, when combined, create an SPI sample clock divisor with a value of four or greater.

Work around

Instead of polling the SPITBF bit to test for an empty buffer (SPI1STAT<1> = 0), implement a SPI receive interrupt handler in software and add to the SPI transmit buffer in this routine.

Alternatively, poll the SPI Receive Full bit, SPIRBF (SPI1STAT<0>), or the Shift Register Empty bit, SRMPT (SPI1STAT<7>), to determine when to service the SPI transmit and transmit buffers.

Affected Silicon Revisions

A5							
X							

TABLE 3: COMPARATOR DC SPECIFICATIONS (PARTIAL)

Param No.	Symbol	Characteristics	Min	Typ	Max	Units	Comments
	VIOFF	Input Offset Voltage	—	20	**60**	mV	

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the Device Data Sheet (DS39927**B**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Memory

In Table 4-4, the CN9IE, CN9PUE and CN9PDE bits (CNEN1<9>, CNPU1<9> and CNPD1<9>, respectively) are not implemented on 20-pin devices. These bits are to be marked with the existing footnote 1 (“These bits are not implemented in 20-pin devices”).

2. Module: Electrical Specifications (AC Specifications)

In Table 29-25, the maximum Differential Nonlinearity specification for the A/D module (parameter AD22b) has changed. The new value is shown below (changes in bold).

TABLE 29-25: ADC MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	Symbol	Characteristic	Min.	Typ	Max.	Units	Conditions
ADC Accuracy							
AD22b	DNL	Differential Nonlinearity	—	±1	**-1, +1.5**	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V

Note 1: The ADC conversion result never decreases with an increase in the input voltage and has no missing codes.

2: Measurements taken with external VREF+ and VREF- used as the ADC voltage reference.

3. Module: Electrical Specifications (DC Specifications)

In Table 29-6, the values for parameters 20d and 20e (IDD for Deep Sleep) have changed. The corrected values are shown below (changes in bold).

TABLE 29-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Parameter No.	Typical(1)	Max	Units	Conditions		
IDD Current						
DC20	195	330	µA	-40°C	1.8V	0.5 MIPS, FOSC = 1 MHz
DS20a		330		+25°C		
DC20b		330		+60°C		
DC20c		330		+85°C		
DC20d	365	**590**	µA	-40°C	3.3V	
DC20e		**590**		+25°C		
DC20f		645		+60°C		
DC20g		720		+85°C		

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Operating Parameters:
- EC mode with clock input driven with a square wave rail-to-rail
- I/O configured as outputs driven low
- $\overline{MCLR}$ – VDD
- WDT FSCM disabled
- SRAM, program and data memory active
- All PMD bits set except for modules being measured

4. Module: Electrical Specifications (DC Specifications)

In Table 29-8, the typical values for the Watchdog Timer Current at 1.8V and all temperatures (parameters D61 through D61C) are changed to 0.55 µA.

5. Module: Electrical Specifications (DC Specifications)

In Table 29-8, footnote 2 includes the text: "All I/Os are configured as inputs and pulled high….". This is changed to read as, "All I/Os are configured as outputs and set low….".

6. Module: Electrical Specifications (DC Specifications)

The minimum and maximum values for the BOR trip points in Table 29-5 have changed. The corrected values are shown below (changes in bold).

TABLE 29-5: BOR TRIP POINTS

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial								
Param No.	Sym	Characteristic		Min	Typ	Max	Units	Conditions
DC19		BOR Voltage on VDD Transition	BOR = 00	**1.55**	2	**2.00**	V	Valid for LPBOR and DSBOR
			BOR = 01	2.92	3	**3.25**	V	
			BOR = 10	2.63	2.7	**2.92**	V	
			BOR = 11	1.75	1.82	**2.01**	V	

7. Module: A/D

In Register 22-3, the values shown for AD1CON3<5:0> (ADCS<5:0>) are incorrect. The corrected values are shown below (changes in bold).

REGISTER 22-3: AD1CON3: A/D CONTROL REGISTER 3

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADRC	—	—	SAMC4	SAMC3	SAMC2	SAMC1	SAMC0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 5-0 ADCS<5:0>: A/D Conversion Clock Select bits

11111 = 63 • TCY
11110 = 62 • TCY
.
.
.
00001 = TCY
00000 = TCY/2

8. Module: Comparators

The descriptions given for the CMIDL bit (CMSTAT<15>) are incorrect. The correct descriptions are shown below (changes in bold).

REGISTER 22-4: CMSTAT: COMPARATOR MODULE STATUS REGISTER

R/W-0	U-0	U-0	U-0	U-0	U-0	R-0, HSC	R-0, HSC
CMIDL	—	—	—	—	—	C2EVT	C1EVT
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R-0, HSC	R-0, HSC
—	—	—	—	—	—	C2OUT	C1OUT
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **CMIDL: Stop in Idle Mode bit**

1 = When device enters Idle mode, the module does not generate interrupts; module is still enabled

0 = Continue normal module operation in Idle mode

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (6/2009)

Initial release of this document; issued for revision A5. Includes silicon issues 1 (CTMU), 2 (Resets – BOR), 3 (Core – ICSP), 4 (Core – Deep Sleep), 5 (Memory – Code Protection), 6 (Comparator) and 7 (SPI – Enhanced Buffer Mode). Includes data sheet clarifications 1 (Memory), 2 (Electrical Specifications – AC Specifications), 3-6 (Electrical Specifications – DC Specifications), 7 (A/D) and 8 (Comparators).

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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