



PIC18F87J93 Family Data Sheet

**64/80-Pin, High-Performance Microcontrollers
with LCD Driver, 12-Bit A/D
and nanoWatt Technology**

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64/80-Pin, High-Performance Microcontrollers with LCD Driver, 12-Bit A/D and nanoWatt Technology

LCD Driver and Keypad Interface

Features:

- Direct LCD Panel Drive Capability:
 - Can drive LCD panel while in Sleep mode
- Up to 48 Segments and 192 Pixels, Software Selectable
- Programmable LCD Timing module:
 - Multiple LCD timing sources available
 - Up to four commons: static, 1/2, 1/3 or 1/4 multiplex
 - Static, 1/2 or 1/3 bias configuration
- On-Chip LCD Boost Voltage Regulator for Contrast Control
- Charge Time Measurement Unit (CTMU) for Capacitive Touch Sensing
- ADC for Resistive Touch Sensing

Low-Power Features:

- Power-Managed modes:
 - Run: CPU On, Peripherals On
 - Idle: CPU Off, Peripherals On
 - Sleep: CPU Off, Peripherals Off
- Two-Speed Oscillator Start-up

Flexible Oscillator Structure:

- Two Crystal modes, 4-25 MHz
- Two External Clock modes, up to 48 MHz
- 4x Phase Lock Loop (PLL)
- Internal Oscillator Block with PLL:
 - Eight user-selectable frequencies from 31.25 kHz to 8 MHz
- Secondary Oscillator using Timer1 at 32 kHz
- Fail-Safe Clock Monitor (FSCM):
 - Allows for safe shutdown if peripheral clock fails

Peripheral Highlights:

- High-Current Sink/Source 25 mA/25 mA (PORTB and PORTC)
- Up to Four External Interrupts
- Four 8-Bit/16-Bit Timer/Counter modules
- Two Capture/Compare/PWM (CCP) modules
- Master Synchronous Serial Port (MSSP) module with Two Modes of Operation:
 - 3-Wire/4-Wire SPI (supports all four SPI modes)
 - I²C™ Master and Slave mode
- One Addressable USART module
- One Enhanced Addressable USART module:
 - LIN/J2602 support
 - Auto-wake-up on Start bit and Break character
 - Auto-Baud Detect (ABD)
- 12-Bit, up to 12-Channel A/D Converter:
 - Auto-acquisition
 - Conversion available during Sleep
- Two Analog Comparators
- Programmable Reference Voltage for Comparators
- Hardware Real-Time Clock and Calendar (RTCC) with Clock, Calendar and Alarm Functions
- Charge Time Measurement Unit (CTMU):
 - Capacitance measurement
 - Time measurement with 1 ns typical resolution

Note: This document is supplemented by the "PIC18F87J90 Family Data Sheet" (DS39933). See **Section 1.0 "Device Overview"**.

Device	Flash Program Memory (Bytes)	SRAM Data Memory (Bytes)	I/O	LCD (Pixels)	Timers 8/16-Bit	CCP	MSSP		EUSART AUSART	12-Bit A/D (Channels)	Comparators	BOR/LVD	RTCC	CTMU
							SPI	Master I ² C™						
PIC18F66J93	64K	3,923	51	132	1/3	2	Yes	Yes	1/1	12	2	Yes	Yes	Yes
PIC18F67J93	128K	3,923	51	132	1/3	2	Yes	Yes	1/1	12	2	Yes	Yes	Yes
PIC18F86J93	64K	3,923	67	192	1/3	2	Yes	Yes	1/1	12	2	Yes	Yes	Yes
PIC18F87J93	128K	3,923	67	192	1/3	2	Yes	Yes	1/1	12	2	Yes	Yes	Yes

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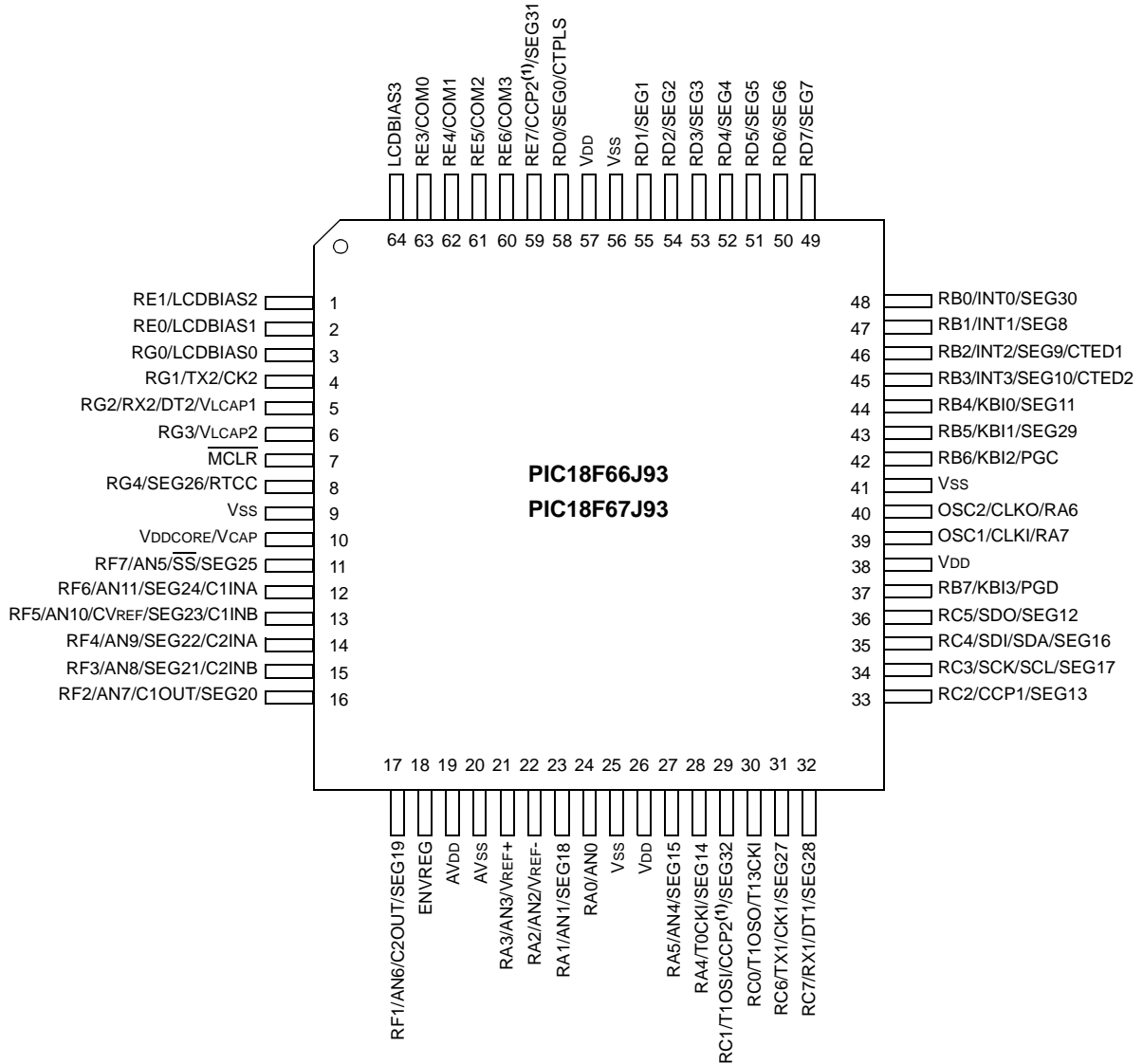
Special Microcontroller Features:

- 10,000 Erase/Write Cycle Flash Program Memory, Typical
- Flash Retention 20 Years, Minimum
- Self-Programmable under Software Control
- Flash Program Memory has Word Write Capability for Data EEPROM Emulators
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
 - Programmable period from 4 ms to 131s
- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug via Two Pins
- Operating Voltage Range: 2.0V to 3.6V
- 5.5V Tolerant Input (digital pins only)
- Selectable Open-Drain Configuration for Serial Communication and CCP Pins for Driving Outputs up to 5V
- On-Chip 2.5V Regulator

PIC18F87J93 FAMILY

Pin Diagrams – PIC18F6XJ93

64-Pin TQFP

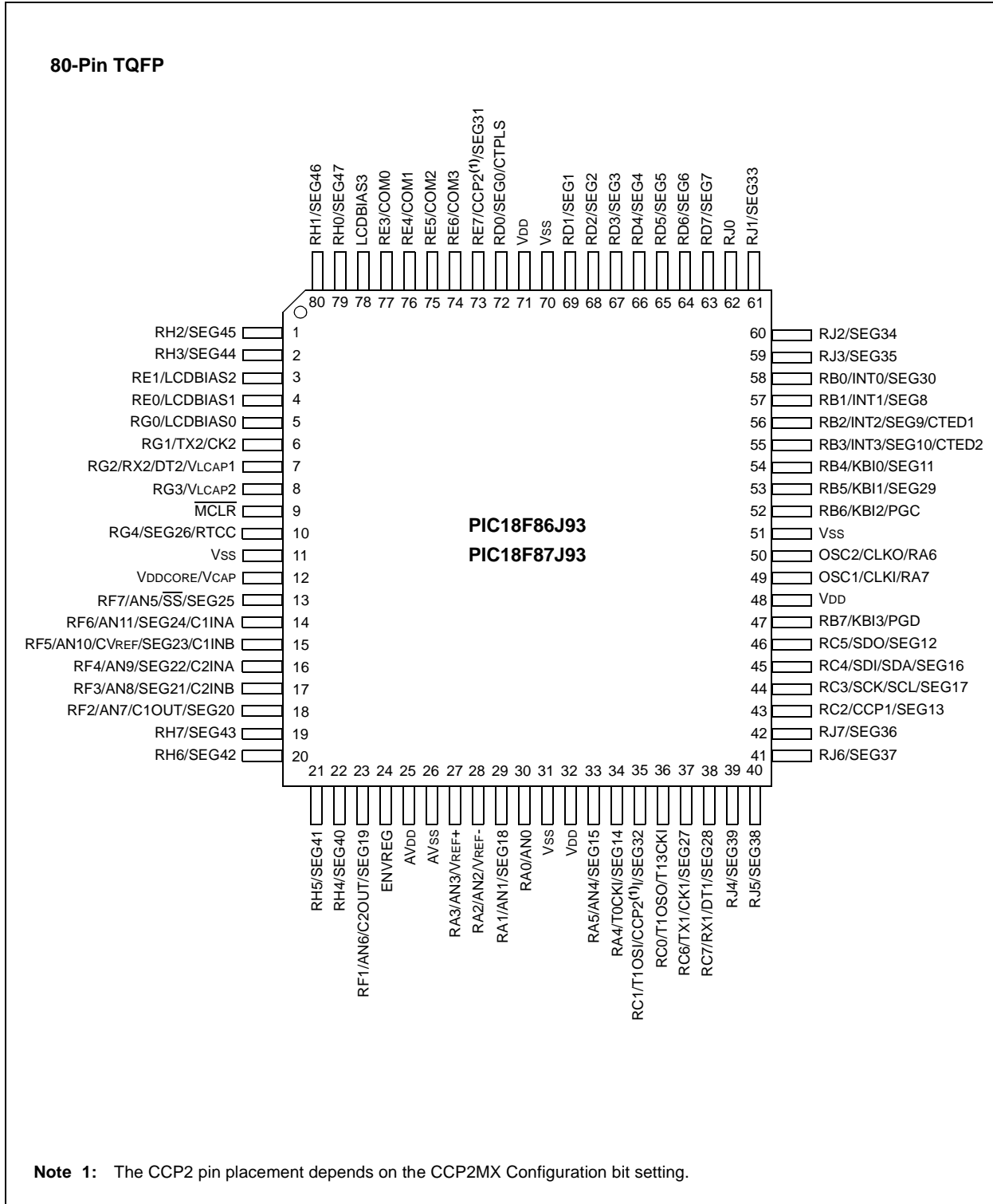


Note 1: The CCP2 pin placement depends on the CCP2MX Configuration bit setting.

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Pin Diagrams – PIC18F8XJ93



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1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC18F66J93
- PIC18F67J93
- PIC18F86J93
- PIC18F87J93

Note: This data sheet documents only the devices' features and specifications that are in addition to the features and specifications of the PIC18F87J90 family devices. For information on the features and specifications shared by the PIC18F87J93 family and PIC18F87J90 family devices, see the "PIC18F87J90 Family Data Sheet" (DS39933).

The PIC18F87J93 family of devices offers the advantages of all PIC18 microcontrollers – high computational performance, a rich feature set and economical price – with the addition of a versatile, on-chip LCD driver. These features make the PIC18F87J93 family a logical choice for many high-performance applications where price is a primary consideration.

1.1 Special Features

- **12-Bit A/D Converter:** The PIC18F87J93 family implements a 12-bit A/D converter. A/D converters in both families incorporate programmable acquisition time. This allows for a channel to be selected and a conversion to be initiated, without waiting for a sampling period and thus, reducing code overhead.
- **Data RAM:** The PIC18F87J93 family devices have 3,923 bytes of RAM.

1.2 Details on Individual Family Members

Devices in the PIC18F87J93 family are available in 64-pin and 80-pin packages. Block diagrams for the two groups are shown in Figure 1-1 and Figure 1-2.

The devices are differentiated from each other in the following ways:

- Flash Program Memory (64 Kbytes for PIC18FX6J93 devices and 128 Kbytes for PIC18FX7J93).
- LCD Pixels:
 - 64-pin devices – 132 pixels (33 SEGs x 4 COMs)
 - 80-pin devices – 192 pixels (48 SEGs x 4 COMs)
- I/O Ports (seven bidirectional ports on PIC18F6XJ93 devices and nine bidirectional ports on PIC18F8XJ93 devices).

All other features for devices in this family are identical and are summarized in Table 1-1 and Table 1-2.

The devices' block diagrams are given in Figure 1-1 and Figure 1-2.

The pinouts for all devices are listed in Table 1-3 and Table 1-4.

PIC18F87J93 FAMILY

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TABLE 1-1: DEVICE FEATURES FOR THE PIC18F6XJ93 (64-PIN DEVICES)

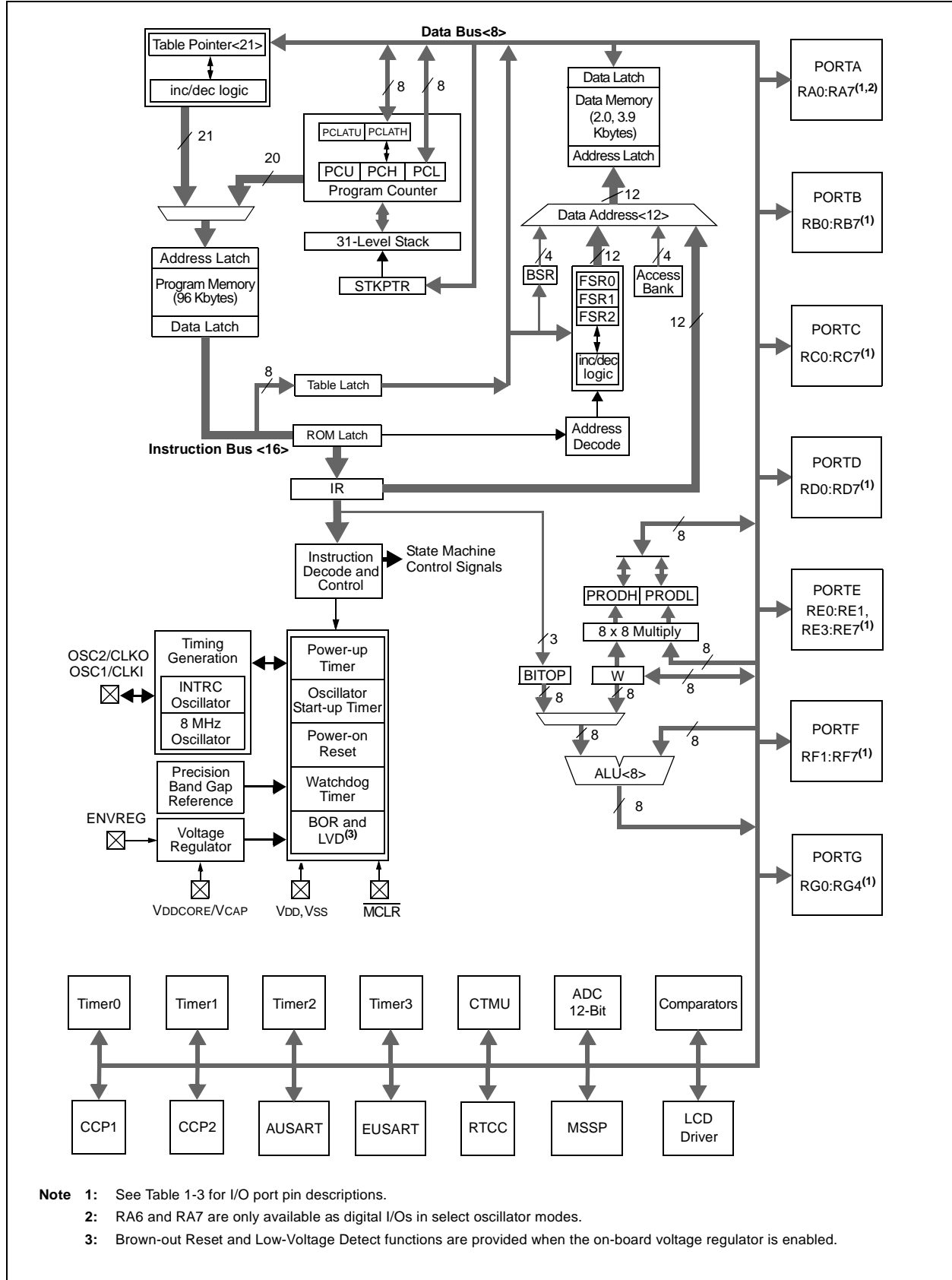
Features	PIC18F66J93	PIC18F67J93
Operating Frequency	DC – 48 MHz	
Program Memory (Bytes)	64K	128K
Program Memory (Instructions)	32,768	65,536
Data Memory (Bytes)	3,923	3,923
Interrupt Sources	29	
I/O Ports	Ports A, B, C, D, E, F, G	
LCD Driver (available pixels to drive)	132 (33 SEGs x 4 COMs)	
Timers	4	
Comparators	2	
CTMU	Yes	
RTCC	Yes	
Capture/Compare/PWM Modules	2	
Serial Communications	MSSP, Addressable USART, Enhanced USART	
12-Bit Analog-to-Digital Module	12 Input Channels	
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow, MCLR, WDT (PWRT, OST)	
Instruction Set	75 Instructions, 83 with Extended Instruction Set Enabled	
Packages	64-Pin TQFP	

TABLE 1-2: DEVICE FEATURES FOR THE PIC18F8XJ93 (80-PIN DEVICES)

Features	PIC18F86J93	PIC18F87J93
Operating Frequency	DC – 48 MHz	
Program Memory (Bytes)	64K	128K
Program Memory (Instructions)	32,768	65,536
Data Memory (Bytes)	3,923	3,923
Interrupt Sources	29	
I/O Ports	Ports A, B, C, D, E, F, G, H, J	
LCD Driver (available pixels to drive)	192 (48 SEGs x 4 COMs)	
Timers	4	
Comparators	2	
CTMU	Yes	
RTCC	Yes	
Capture/Compare/PWM Modules	2	
Serial Communications	MSSP, Addressable USART, Enhanced USART	
12-Bit Analog-to-Digital Module	12 Input Channels	
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow, MCLR, WDT (PWRT, OST)	
Instruction Set	75 Instructions, 83 with Extended Instruction Set Enabled	
Packages	80-Pin TQFP	

PIC18F87J93 FAMILY

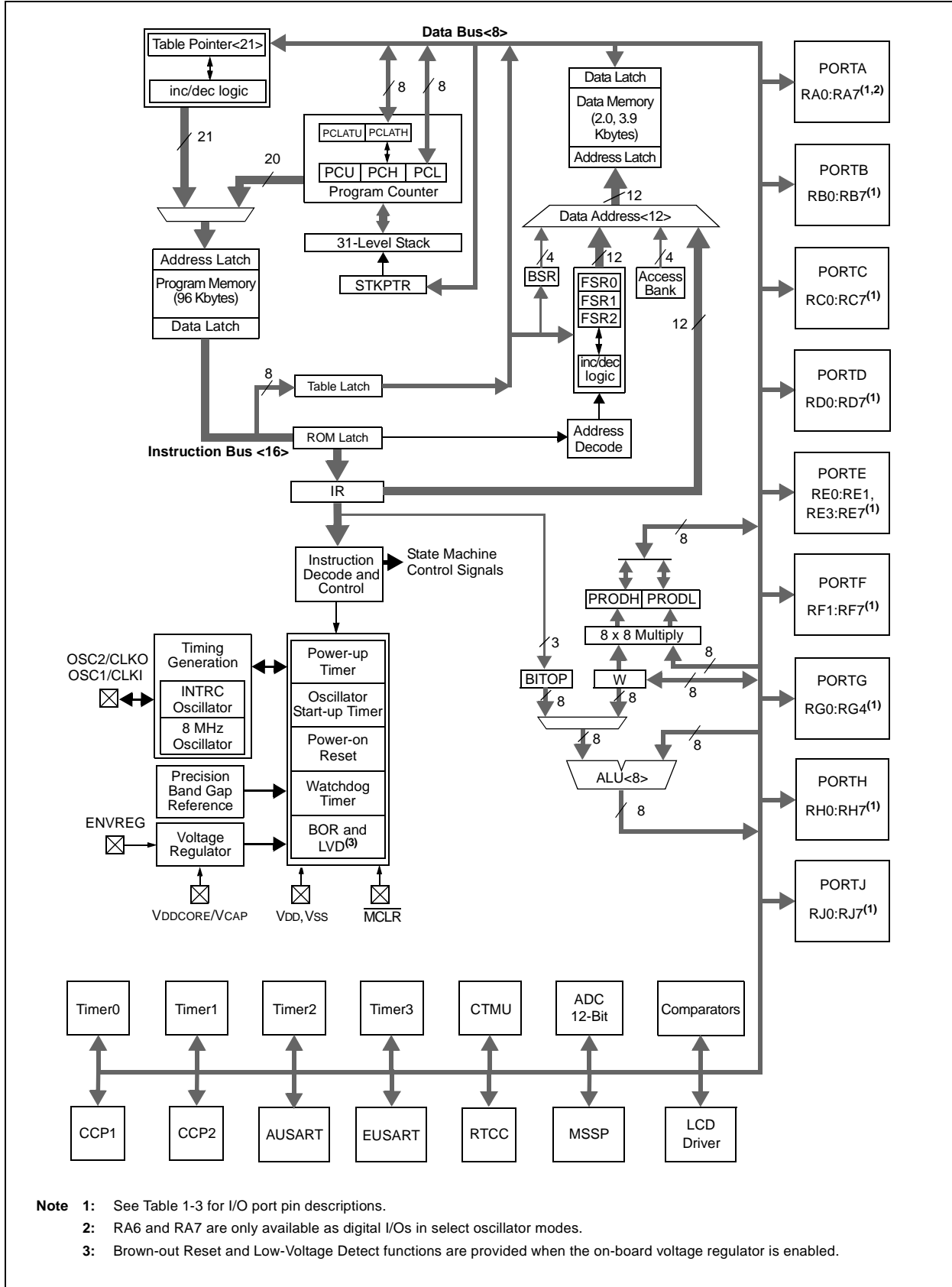
FIGURE 1-1: PIC18F6XJ93 (64-PIN) BLOCK DIAGRAM



- Note 1:** See Table 1-3 for I/O port pin descriptions.
Note 2: RA6 and RA7 are only available as digital I/Os in select oscillator modes.
Note 3: Brown-out Reset and Low-Voltage Detect functions are provided when the on-board voltage regulator is enabled.

PIC18F87J93 FAMILY

FIGURE 1-2: PIC18F8XJ93 (80-PIN) BLOCK DIAGRAM



PIC18F87J93 FAMILY

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TABLE 1-3: PIC18F6XJ93 (64-PIN DEVICE) PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
				PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/INT0/SEG30 RB0 INT0 SEG30	48	I/O I O	TTL ST Analog	Digital I/O. External Interrupt 0. SEG30 output for LCD.
RB1/INT1/SEG8 RB1 INT1 SEG8	47	I/O I O	TTL ST Analog	Digital I/O. External Interrupt 1. SEG8 output for LCD.
RB2/INT2/SEG9/CTED1 RB2 INT2 SEG9 CTED1	46	I/O I O I	TTL ST Analog ST	Digital I/O. External Interrupt 2. SEG9 output for LCD. CTMU Edge 1 input.
RB3/INT3/SEG10/CTED2 RB3 INT3 SEG10 CTED2	45	I/O I O I	TTL ST Analog ST	Digital I/O. External Interrupt 3. SEG10 output for LCD. CTMU Edge 2 input.
RB4/KBI0/SEG11 RB4 KBI0 SEG11	44	I/O I O	TTL TTL Analog	Digital I/O. Interrupt-on-change pin. SEG11 output for LCD.
RB5/KBI1/SEG29 RB5 KBI1 SEG29	43	I/O I O	TTL TTL Analog	Digital I/O. Interrupt-on-change pin. SEG29 output for LCD.
RB6/KBI2/PGC RB6 KBI2 PGC	42	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP™ programming clock pin.
RB7/KBI3/PGD RB7 KBI3 PGD	37	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP programming data pin.

Legend: TTL = TTL compatible input
 ST = Schmitt Trigger input with CMOS levels
 I = Input
 P = Power
 CMOS = CMOS compatible input or output
 Analog = Analog input
 O = Output
 OD = Open-Drain (no P diode to VDD)

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.
Note 2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

PIC18F87J93 FAMILY

TABLE 1-3: PIC18F6XJ93 (64-PIN DEVICE) PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RD0/SEG0/CTPLS	58	I/O	ST	PORTD is a bidirectional I/O port. Digital I/O. SEG0 output for LCD. CTMU pulse generator output.
RD0		O	Analog	
SEG0 CTPLS		O	—	
RD1/SEG1	55	I/O	ST	Digital I/O. SEG1 output for LCD.
RD1 SEG1		O	Analog	
RD2/SEG2	54	I/O	ST	Digital I/O. SEG2 output for LCD.
RD2 SEG2		O	Analog	
RD3/SEG3	53	I/O	ST	Digital I/O. SEG3 output for LCD.
RD3 SEG3		O	Analog	
RD4/SEG4	52	I/O	ST	Digital I/O. SEG4 output for LCD.
RD4 SEG4		O	Analog	
RD5/SEG5	51	I/O	ST	Digital I/O. SEG5 output for LCD.
RD5 SEG5		O	Analog	
RD6/SEG6	50	I/O	ST	Digital I/O. SEG6 output for LCD.
RD6 SEG6		O	Analog	
RD7/SEG7	49	I/O	ST	Digital I/O. SEG7 output for LCD.
RD7 SEG7		O	Analog	

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
 ST = Schmitt Trigger input with CMOS levels Analog = Analog input
 I = Input O = Output
 P = Power OD = Open-Drain (no P diode to VDD)

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

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TABLE 1-3: PIC18F6XJ93 (64-PIN DEVICE) PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RE0/LCDBIAS1 RE0 LCDBIAS1	2	I/O I	ST Analog	<p>PORTE is a bidirectional I/O port.</p> <p>Digital I/O. BIAS1 input for LCD.</p>
RE1/LCDBIAS2 RE1 LCDBIAS2	1	I/O I	ST Analog	<p>Digital I/O. BIAS2 input for LCD.</p>
LCDBIAS3	64	I	Analog	BIAS3 input for LCD.
RE3/COM0 RE3 COM0	63	I/O O	ST Analog	<p>Digital I/O. COM0 output for LCD.</p>
RE4/COM1 RE4 COM1	62	I/O O	ST Analog	<p>Digital I/O. COM1 output for LCD.</p>
RE5/COM2 RE5 COM2	61	I/O O	ST Analog	<p>Digital I/O. COM2 output for LCD.</p>
RE6/COM3 RE6 COM3	60	I/O O	ST Analog	<p>Digital I/O. COM3 output for LCD.</p>
RE7/CCP2/SEG31 RE7 CCP2 ⁽²⁾ SEG31	59	I/O I/O O	ST ST Analog	<p>Digital I/O. Capture 2 input/Compare 2 output/PWM2 output. SEG31 output for LCD.</p>

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
 ST = Schmitt Trigger input with CMOS levels Analog = Analog input
 I = Input O = Output
 P = Power OD = Open-Drain (no P diode to VDD)

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

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TABLE 1-3: PIC18F6XJ93 (64-PIN DEVICE) PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RF1/AN6/C2OUT/SEG19	17	I/O	ST	PORTF is a bidirectional I/O port. Digital I/O. Analog Input 6. Comparator 2 output. SEG19 output for LCD.
RF1		I	Analog	
AN6		O	—	
C2OUT		O	Analog	
RF2/AN7/C1OUT/SEG20	16	I/O	ST	Digital I/O. Analog Input 7. Comparator 1 output. SEG20 output for LCD.
RF2		I	Analog	
AN7		O	—	
C1OUT		O	Analog	
RF3/AN8/SEG21/C2INB	15	I/O	ST	Digital I/O. Analog Input 8. SEG21 output for LCD. Comparator 2 input B.
RF3		I	Analog	
AN8		O	Analog	
SEG21		I	Analog	
RF4/AN9/SEG22/C2INA	14	I/O	ST	Digital I/O. Analog Input 9. SEG22 output for LCD Comparator 2 input A.
RF4		I	Analog	
AN9		O	Analog	
SEG22		I	Analog	
RF5/AN10/CVREF/SEG23/C1INB	13	I/O	ST	Digital I/O. Analog Input 10. Comparator reference voltage output. SEG23 output for LCD. Comparator 1 input B.
RF5		I	Analog	
AN10		O	Analog	
CVREF		O	Analog	
SEG23		I	Analog	
C1INB				
RF6/AN11/SEG24/C1INA	12	I/O	ST	Digital I/O. Analog Input 11. SEG24 output for LCD Comparator 1 input A.
RF6		I	Analog	
AN11		O	Analog	
SEG24		I	Analog	
RF7/AN5/SS/SEG25	11	I/O	ST	Digital I/O. Analog Input 5. SPI slave select input. SEG25 output for LCD.
RF7		O	Analog	
AN5		I	TTL	
SS		O	Analog	
SEG25				

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
 ST = Schmitt Trigger input with CMOS levels Analog = Analog input
 I = Input O = Output
 P = Power OD = Open-Drain (no P diode to VDD)

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

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TABLE 1-3: PIC18F6XJ93 (64-PIN DEVICE) PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RG0/LCDBIAS0 RG0 LCDBIAS0	3	I/O I	ST Analog	PORTG is a bidirectional I/O port. Digital I/O. BIAS0 input for LCD.
RG1/TX2/CK2 RG1 TX2 CK2	4	I/O O I/O	ST — ST	Digital I/O. AUSART asynchronous transmit. AUSART synchronous clock (see related RX2/DT2).
RG2/RX2/DT2/VLCAP1 RG2 RX2 DT2 VLCAP1	5	I/O I I/O I	ST ST ST Analog	Digital I/O. AUSART asynchronous receive. AUSART synchronous data (see related TX2/CK2). LCD charge pump capacitor input.
RG3/VLCAP2 RG3 VLCAP2	6	I/O I	ST Analog	Digital I/O. LCD charge pump capacitor input.
RG4/SEG26/RTCC RG4 SEG26 RTCC	8	I/O O O	ST Analog —	Digital I/O. SEG26 output for LCD. RTCC output
VSS	9, 25, 41, 56	P	—	Ground reference for logic and I/O pins.
VDD	26, 38, 57	P	—	Positive supply for logic and I/O pins.
AVSS	20	P	—	Ground reference for analog modules.
AVDD	19	P	—	Positive supply for analog modules.
ENVREG	18	I	ST	Enable for on-chip voltage regulator.
VDDCORE/VCAP VDDCORE VCAP	10	P P	— —	Core logic power or external filter capacitor connection. Positive supply for microcontroller core logic (regulator disabled). External filter capacitor connection (regulator enabled).

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
 ST = Schmitt Trigger input with CMOS levels Analog = Analog input
 I = Input O = Output
 P = Power OD = Open-Drain (no P diode to VDD)

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.
Note 2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

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TABLE 1-4: PIC18F8XJ93 (80-PIN DEVICE) PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
MCLR	9	I	ST	Master Clear (input) or programming voltage (input). This pin is an active-low Reset to the device.
OSC1/CLKI/RA7 OSC1 CLKI RA7	49	I I I/O	CMOS CMOS TTL	Oscillator crystal or external clock input. Oscillator crystal input. External clock source input. Always associated with pin function OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.) General purpose I/O pin.
OSC2/CLKO/RA6 OSC2 CLKO RA6	50	O O I/O	— — TTL	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In EC modes, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate. General purpose I/O pin.
RA0/AN0 RA0 AN0	30	I/O I	TTL Analog	PORTA is a bidirectional I/O port. Digital I/O. Analog Input 0.
RA1/AN1/SEG18 RA1 AN1 SEG18	29	I/O I O	TTL Analog Analog	Digital I/O. Analog Input 1. SEG18 output for LCD.
RA2/AN2/VREF- RA2 AN2 VREF-	28	I/O I I	TTL Analog Analog	Digital I/O. Analog Input 2. A/D reference voltage (low) input.
RA3/AN3/VREF+ RA3 AN3 VREF+	27	I/O I I	TTL Analog Analog	Digital I/O. Analog Input 3. A/D reference voltage (high) input.
RA4/T0CKI/SEG14 RA4 T0CKI SEG14	34	I/O I O	ST ST Analog	Digital I/O. Timer0 external clock input. SEG14 output for LCD.
RA5/AN4/SEG15 RA5 AN4 SEG15	33	I/O I O	TTL Analog Analog	Digital I/O. Analog Input 4. SEG15 output for LCD.
RA6				See the OSC2/CLKO/RA6 pin.
RA7				See the OSC1/CLKI/RA7 pin.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power OD = Open-Drain (no P diode to VDD)

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.
Note 2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

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TABLE 1-4: PIC18F8XJ93 (80-PIN DEVICE) PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.				
RB0/INT0/SEG30 RB0 INT0 SEG30	58	I/O I O	TTL ST Analog	Digital I/O. External Interrupt 0. SEG30 output for LCD.
RB1/INT1/SEG8 RB1 INT1 SEG8	57	I/O I O	TTL ST Analog	Digital I/O. External Interrupt 1. SEG8 output for LCD.
RB2/INT2/SEG9/CTED1 RB2 INT2 SEG9 CTED1	56	I/O I O I	TTL ST Analog ST	Digital I/O. External Interrupt 2. SEG9 output for LCD. CTMU Edge 1 input.
RB3/INT3/SEG10/ CTED2 RB3 INT3 SEG10 CTED2	55	I/O I O I	TTL ST Analog ST	Digital I/O. External Interrupt 3. SEG10 output for LCD. CTMU Edge 2 input.
RB4/KBI0/SEG11 RB4 KBI0 SEG11	54	I/O I O	TTL TTL Analog	Digital I/O. Interrupt-on-change pin. SEG11 output for LCD.
RB5/KBI1/SEG29 RB5 KBI1 SEG29	53	I/O I O	TTL TTL Analog	Digital I/O. Interrupt-on-change pin. SEG29 output for LCD.
RB6/KBI2/PGC RB6 KBI2 PGC	52	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP™ programming clock pin.
RB7/KBI3/PGD RB7 KBI3 PGD	47	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP programming data pin.

Legend: TTL = TTL compatible input
 ST = Schmitt Trigger input with CMOS levels
 I = Input
 P = Power
 CMOS = CMOS compatible input or output
 Analog = Analog input
 O = Output
 OD = Open-Drain (no P diode to VDD)

- Note 1:** Default assignment for CCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

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TABLE 1-4: PIC18F8XJ93 (80-PIN DEVICE) PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RC0/T1OSO/T13CKI	36			PORTC is a bidirectional I/O port.
RC0		I/O	ST	Digital I/O.
T1OSO		O	—	Timer1 oscillator output.
T13CKI		I	ST	Timer1/Timer3 external clock input.
RC1/T1OSI/CCP2/SEG32	35			
RC1		I/O	ST	Digital I/O.
T1OSI		I	CMOS	Timer1 oscillator input.
CCP2 ⁽¹⁾ SEG32		I/O O	ST Analog	Capture 2 input/Compare 2 output/PWM2 output. SEG32 output for LCD.
RC2/CCP1/SEG13	43			
RC2		I/O	ST	Digital I/O.
CCP1 SEG13		I/O O	ST Analog	Capture 1 input/Compare 1 output/PWM1 output. SEG13 output for LCD.
RC3/SCK/SCL/SEG17	44			
RC3		I/O	ST	Digital I/O.
SCK		I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL SEG17		I/O O	ST Analog	Synchronous serial clock input/output for I ² C™ mode. SEG17 output for LCD.
RC4/SDI/SDA/SEG16	45			
RC4		I/O	ST	Digital I/O.
SDI		I	ST	SPI data in.
SDA SEG16		I/O O	ST Analog	I ² C data I/O. SEG16 output for LCD.
RC5/SDO/SEG12	46			
RC5		I/O	ST	Digital I/O.
SDO SEG12		O O	— Analog	SPI data out. SEG12 output for LCD.
RC6/TX1/CK1/SEG27	37			
RC6		I/O	ST	Digital I/O.
TX1		O	—	EUSART asynchronous transmit.
CK1 SEG27		I/O O	ST Analog	EUSART synchronous clock (see related RX1/DT1). SEG27 output for LCD.
RC7/RX1/DT1/SEG28	38			
RC7		I/O	ST	Digital I/O.
RX1		I	ST	EUSART asynchronous receive.
DT1 SEG28		I/O O	ST Analog	EUSART synchronous data (see related TX1/CK1). SEG28 output for LCD.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power OD = Open-Drain (no P diode to VDD)

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

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TABLE 1-4: PIC18F8XJ93 (80-PIN DEVICE) PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RD0/SEG0/CTPLS	72	I/O	ST	PORTD is a bidirectional I/O port. Digital I/O. SEG0 output for LCD. CTMU pulse generator output.
RD0		O	Analog	
SEG0		O	ST	
CTPLS		O	ST	
RD1/SEG1	69	I/O	ST	Digital I/O. SEG1 output for LCD.
RD1		O	Analog	
RD2/SEG2	68	I/O	ST	Digital I/O. SEG2 output for LCD.
RD2		O	Analog	
RD3/SEG3	67	I/O	ST	Digital I/O. SEG3 output for LCD.
RD3		O	Analog	
RD4/SEG4	66	I/O	ST	Digital I/O. SEG4 output for LCD.
RD4		O	Analog	
RD5/SEG5	65	I/O	ST	Digital I/O. SEG5 output for LCD.
RD5		O	Analog	
RD6/SEG6	64	I/O	ST	Digital I/O. SEG6 output for LCD.
RD6		O	Analog	
RD7/SEG7	63	I/O	ST	Digital I/O. SEG7 output for LCD.
RD7		O	Analog	
SEG7		O	Analog	

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
 ST = Schmitt Trigger input with CMOS levels Analog = Analog input
 I = Input O = Output
 P = Power OD = Open-Drain (no P diode to VDD)

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

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TABLE 1-4: PIC18F8XJ93 (80-PIN DEVICE) PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RE0/LCDBIAS1 RE0 LCDBIAS1	4	I/O I	ST Analog	PORTE is a bidirectional I/O port. Digital I/O. BIAS1 input for LCD.
RE1/LCDBIAS2 RE1 LCDBIAS2	3	I/O I	ST Analog	Digital I/O. BIAS2 input for LCD.
LCDBIAS3	78	I	Analog	BIAS3 input for LCD.
RE3/COM0 RE3 COM0	77	I/O O	ST Analog	Digital I/O. COM0 output for LCD.
RE4/COM1 RE4 COM1	76	I/O O	ST Analog	Digital I/O. COM1 output for LCD.
RE5/COM2 RE5 COM2	75	I/O O	ST Analog	Digital I/O. COM2 output for LCD.
RE6/COM3 RE6 COM3	74	I/O O	ST Analog	Digital I/O. COM3 output for LCD.
RE7/CCP2/SEG31 RE7 CCP2 ⁽²⁾ SEG31	73	I/O I/O O	ST ST Analog	Digital I/O. Capture 2 input/Compare 2 output/PWM2 output. SEG31 output for LCD.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
 ST = Schmitt Trigger input with CMOS levels Analog = Analog input
 I = Input O = Output
 P = Power OD = Open-Drain (no P diode to VDD)

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.
Note 2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

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TABLE 1-4: PIC18F8XJ93 (80-PIN DEVICE) PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RF1/AN6/C2OUT/SEG19	23			PORTF is a bidirectional I/O port.
RF1		I/O	ST	Digital I/O.
AN6		I	Analog	Analog Input 6.
C2OUT		O	—	Comparator 2 output.
SEG19		O	Analog	SEG19 output for LCD.
RF2/AN7/C1OUT/SEG20	18			
RF2		I/O	ST	Digital I/O.
AN7		I	Analog	Analog Input 7.
C1OUT		O	—	Comparator 1 output.
SEG20		O	Analog	SEG20 output for LCD.
RF3/AN8/SEG21/C2INB	17			
RF3		I/O	ST	Digital I/O.
AN8		I	Analog	Analog Input 8.
SEG21		O	Analog	SEG21 output for LCD.
C2INB		I	Analog	Comparator 2 input B.
RF4/AN9/SEG22/C2INA	16			
RF4		I/O	ST	Digital I/O.
AN9		I	Analog	Analog Input 9.
SEG22		O	Analog	SEG22 output for LCD.
C2INA		I	Analog	Comparator 2 input A.
RF5/AN10/CVREF/SEG23/C1INB	15			
RF5		I/O	ST	Digital I/O.
AN10		I	Analog	Analog Input 10.
CVREF		O	Analog	Comparator reference voltage output.
SEG23		O	Analog	SEG23 output for LCD.
C1INB		I	Analog	Comparator 1 input B.
RF6/AN11/SEG24/C1INA	14			
RF6		I/O	ST	Digital I/O.
AN11		I	Analog	Analog Input 11.
SEG24		O	Analog	SEG24 output for LCD.
C1INA		I	Analog	Comparator 1 input A.
RF7/AN5/SS/SEG25	13			
RF7		I/O	ST	Digital I/O.
AN5		O	Analog	Analog Input 5.
SS		I	TTL	SPI slave select input.
SEG25		O	Analog	SEG25 output for LCD.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
 ST = Schmitt Trigger input with CMOS levels Analog = Analog input
 I = Input O = Output
 P = Power OD = Open-Drain (no P diode to VDD)

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

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TABLE 1-4: PIC18F8XJ93 (80-PIN DEVICE) PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RG0/LCDBIAS0 RG0 LCDBIAS0	5	I/O I	ST Analog	PORTG is a bidirectional I/O port. Digital I/O. BIAS0 input for LCD.
RG1/TX2/CK2 RG1 TX2 CK2	6	I/O O I/O	ST — ST	Digital I/O. AUSART asynchronous transmit. AUSART synchronous clock (see related RX2/DT2).
RG2/RX2/DT2/VLCAP1 RG2 RX2 DT2 VLCAP1	7	I/O I I/O I	ST ST ST Analog	Digital I/O. AUSART asynchronous receive. AUSART synchronous data (see related TX2/CK2). LCD charge pump capacitor input.
RG3/VLCAP2 RG3 VLCAP2	8	I/O I	ST Analog	Digital I/O. LCD charge pump capacitor input.
RG4/SEG26/RTCC RG4 SEG26 RTCC	10	I/O O O	ST Analog —	Digital I/O. SEG26 output for LCD. RTCC output.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power OD = Open-Drain (no P diode to VDD)

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

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TABLE 1-4: PIC18F8XJ93 (80-PIN DEVICE) PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RH0/SEG47 RH0 SEG47	79	I/O O	ST Analog	PORTH is a bidirectional I/O port. Digital I/O. SEG47 output for LCD.
RH1/SEG46 RH1 SEG46	80	I/O O	ST Analog	Digital I/O. SEG46 output for LCD.
RH2/SEG45 RH2 SEG45	1	I/O O	ST Analog	Digital I/O. SEG45 output for LCD.
RH3/SEG44 RH3 SEG44	2	I/O O	ST Analog	Digital I/O. SEG44 output for LCD.
RH4/SEG40 RH4 SEG40	22	I/O O	ST Analog	Digital I/O. SEG40 output for LCD.
RH5/SEG41 RH5 SEG41	21	I/O O	ST Analog	Digital I/O. SEG41 output for LCD.
RH6/SEG42 RH6 SEG42	20	I/O O	ST Analog	Digital I/O. SEG42 output for LCD.
RH7/SEG43 RH7 SEG43	19	I/O O	ST Analog	Digital I/O. SEG43 output for LCD.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power OD = Open-Drain (no P diode to VDD)

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

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TABLE 1-4: PIC18F8XJ93 (80-PIN DEVICE) PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RJ0	62	I/O	ST	PORTJ is a bidirectional I/O port. Digital I/O.
RJ1/SEG33	61	I/O	ST	Digital I/O.
RJ1		O	Analog	SEG33 output for LCD.
RJ2/SEG34	60	I/O	ST	Digital I/O.
RJ2		O	Analog	SEG34 output for LCD.
RJ3/SEG35	59	I/O	ST	Digital I/O.
RJ3		O	Analog	SEG35 output for LCD.
RJ4/SEG39	39	I/O	ST	Digital I/O.
RJ4		O	Analog	SEG39 output for LCD.
RJ5/SEG38	40	I/O	ST	Digital I/O.
RJ5		O	Analog	SEG38 output for LCD.
RJ6/SEG37	41	I/O	ST	Digital I/O.
RJ6		O	Analog	SEG37 output for LCD.
RJ7/SEG36	42	I/O	ST	Digital I/O.
RJ7		O	Analog	SEG36 output for LCD.
VSS	11, 31, 51, 70	P	—	Ground reference for logic and I/O pins.
VDD	32, 48, 71	P	—	Positive supply for logic and I/O pins.
AVSS	26	P	—	Ground reference for analog modules.
AVDD	25	P	—	Positive supply for analog modules.
ENVREG	24	I	ST	Enable for on-chip voltage regulator.
VDDCORE/VCAP	12	P	—	Core logic power or external filter capacitor connection.
VDDCORE		P	—	Positive supply for microcontroller core logic (regulator disabled).
VCAP		P	—	External filter capacitor connection (regulator enabled).

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power OD = Open-Drain (no P diode to VDD)

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

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2.0 12-BIT ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The Analog-to-Digital (A/D) converter module has 12 inputs for all PIC18F87J93 family devices. This module allows conversion of an analog input signal to a corresponding 12-bit digital number.

The module has these registers:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)
- A/D Control Register 2 (ADCON2)

The ADCON0 register, shown in Register 2-1, controls the operation of the A/D module. The ADCON1 register, shown in Register 2-2, configures the functions of the port pins. The ADCON2 register, shown in Register 2-3, configures the A/D clock source, programmed acquisition time and justification.

REGISTER 2-1: ADCON0: A/D CONTROL REGISTER 0

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCAL	—	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON
bit 7						bit 0	

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared

x = Bit is unknown

- bit 7 **ADCAL:** A/D Calibration bit
1 = Calibration is performed on next A/D conversion
0 = Normal A/D converter operation (no calibration is performed)
- bit 6 **Unimplemented:** Read as '0'
- bit 5-2 **CHS<3:0>:** Analog Channel Select bits
0000 = Channel 00 (AN0)
0001 = Channel 01 (AN1)
0010 = Channel 02 (AN2)
0011 = Channel 03 (AN3)
0100 = Channel 04 (AN4)
0101 = Channel 05 (AN5)
0110 = Channel 06 (AN6)
0111 = Channel 07 (AN7)
1000 = Channel 08 (AN8)
1001 = Channel 09 (AN9)
1010 = Channel 10 (AN10)
1011 = Channel 11 (AN11)
11xx = Unused
- bit 1 **GO/DONE:** A/D Conversion Status bit
When ADON = 1:
1 = A/D conversion in progress
0 = A/D Idle
- bit 0 **ADON:** A/D On bit
1 = A/D converter module is enabled
0 = A/D converter module is disabled

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REGISTER 2-2: ADCON1: A/D CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TRIGSEL	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 7 **TRIGSEL:** Special Trigger Select bit
 1 = Selects the special trigger from the CTMU
 0 = Selects the special trigger from the CCP2
- bit 6 **Unimplemented:** Read as '0'
- bit 5 **VCFG1:** Voltage Reference Configuration bit (VREF- source)
 1 = VREF- (AN2)
 0 = AVSS
- bit 4 **VCFG0:** Voltage Reference Configuration bit (VREF+ source)
 1 = VREF+ (AN3)
 0 = AVDD
- bit 3-0 **PCFG<3:0>:** A/D Port Configuration Control bits:

PCFG<3:0>	AN11	AN10	AN9	AN8	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
0000	A	A	A	A	A	A	A	A	A	A	A	A
0001	A	A	A	A	A	A	A	A	A	A	A	A
0010	A	A	A	A	A	A	A	A	A	A	A	A
0011	A	A	A	A	A	A	A	A	A	A	A	A
0100	D	A	A	A	A	A	A	A	A	A	A	A
0101	D	D	A	A	A	A	A	A	A	A	A	A
0110	D	D	D	A	A	A	A	A	A	A	A	A
0111	D	D	D	D	A	A	A	A	A	A	A	A
1000	D	D	D	D	D	A	A	A	A	A	A	A
1001	D	D	D	D	D	D	A	A	A	A	A	A
1010	D	D	D	D	D	D	D	A	A	A	A	A
1011	D	D	D	D	D	D	D	D	A	A	A	A
1100	D	D	D	D	D	D	D	D	D	A	A	A
1101	D	D	D	D	D	D	D	D	D	D	A	A
1110	D	D	D	D	D	D	D	D	D	D	D	A
1111	D	D	D	D	D	D	D	D	D	D	D	D

A = Analog input D = Digital I/O

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REGISTER 2-3: ADCON2: A/D CONTROL REGISTER 2

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 7 **ADFM:** A/D Result Format Select bit
 1 = Right justified
 0 = Left justified
- bit 6 **Unimplemented:** Read as '0'
- bit 5-3 **ACQT<2:0>:** A/D Acquisition Time Select bits
 111 = 20 TAD
 110 = 16 TAD
 101 = 12 TAD
 100 = 8 TAD
 011 = 6 TAD
 010 = 4 TAD
 001 = 2 TAD
 000 = 0 TAD⁽¹⁾
- bit 2-0 **ADCS<2:0>:** A/D Conversion Clock Select bits
 111 = FRC (clock derived from A/D RC oscillator)⁽¹⁾
 110 = FOSC/64
 101 = FOSC/16
 100 = FOSC/4
 011 = FRC (clock derived from A/D RC oscillator)⁽¹⁾
 010 = FOSC/32
 001 = FOSC/8
 000 = FOSC/2

Note 1: If the A/D FRC clock source is selected, a delay of one T_{CY} (instruction cycle) is added before the A/D clock starts. This allows the SLEEP instruction to be executed before starting a conversion.

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The analog reference voltage is software selectable to either the device's positive and negative supply voltage (AVDD and AVSS) or the voltage level on the RA3/AN3/VREF+ and RA2/AN2/VREF- pins.

The A/D converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

The output of the sample and hold is the input into the converter, which generates the result via successive approximation.

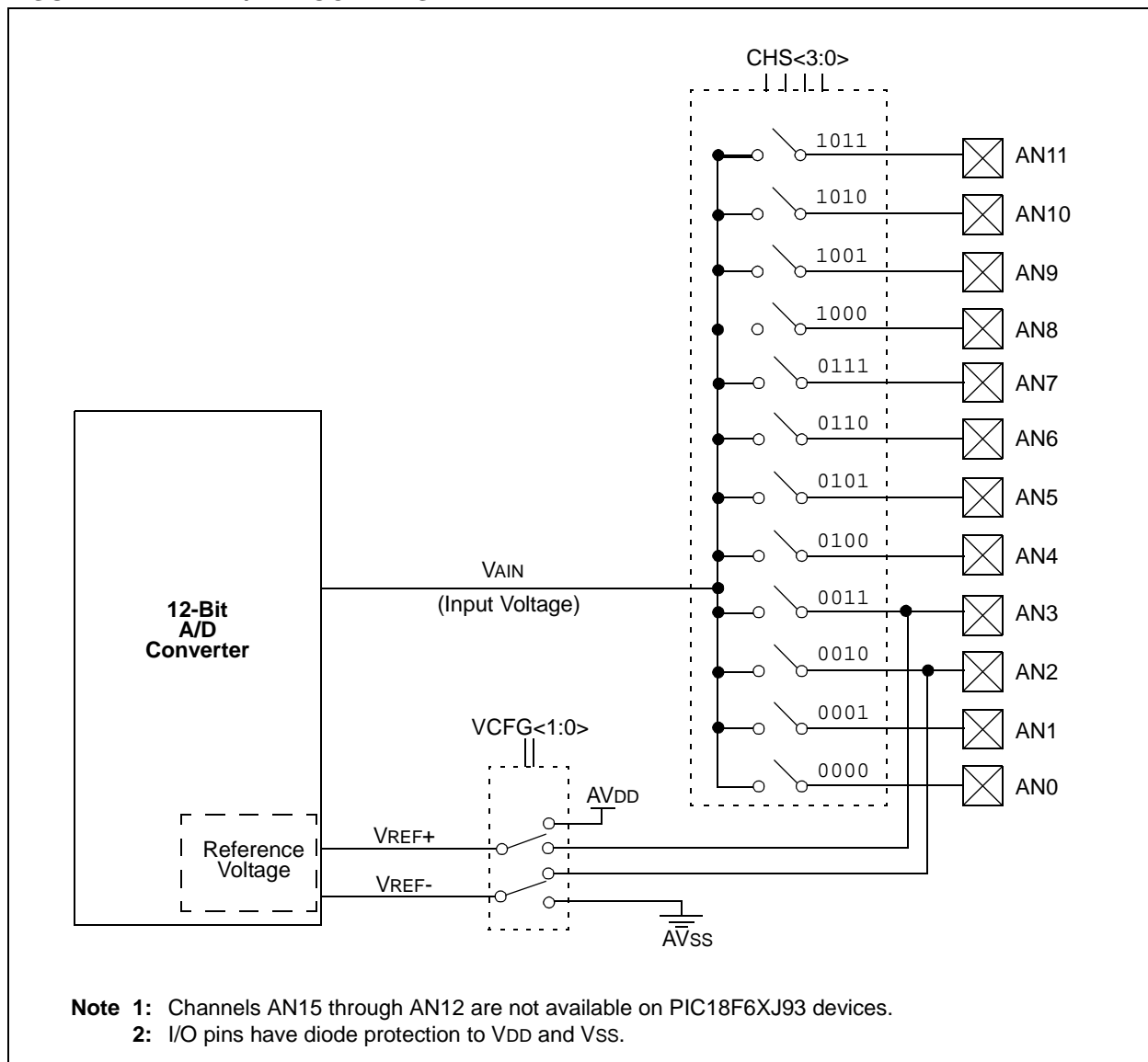
Each port pin associated with the A/D converter can be configured as an analog input or as a digital I/O. The ADRESH and ADRESL registers contain the result of the

A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRESH:ADRESL register pair, the GO/DONE bit (ADCON0<1>) is cleared and the A/D Interrupt Flag bit, ADIF, is set.

A device Reset forces all registers to their Reset state. This forces the A/D module to be turned off and any conversion in progress is aborted. The value in the ADRESH:ADRESL register pair is not modified for a Power-on Reset. These registers will contain unknown data after a Power-on Reset.

The block diagram of the A/D module is shown in Figure 2-1.

FIGURE 2-1: A/D BLOCK DIAGRAM^(1,2)



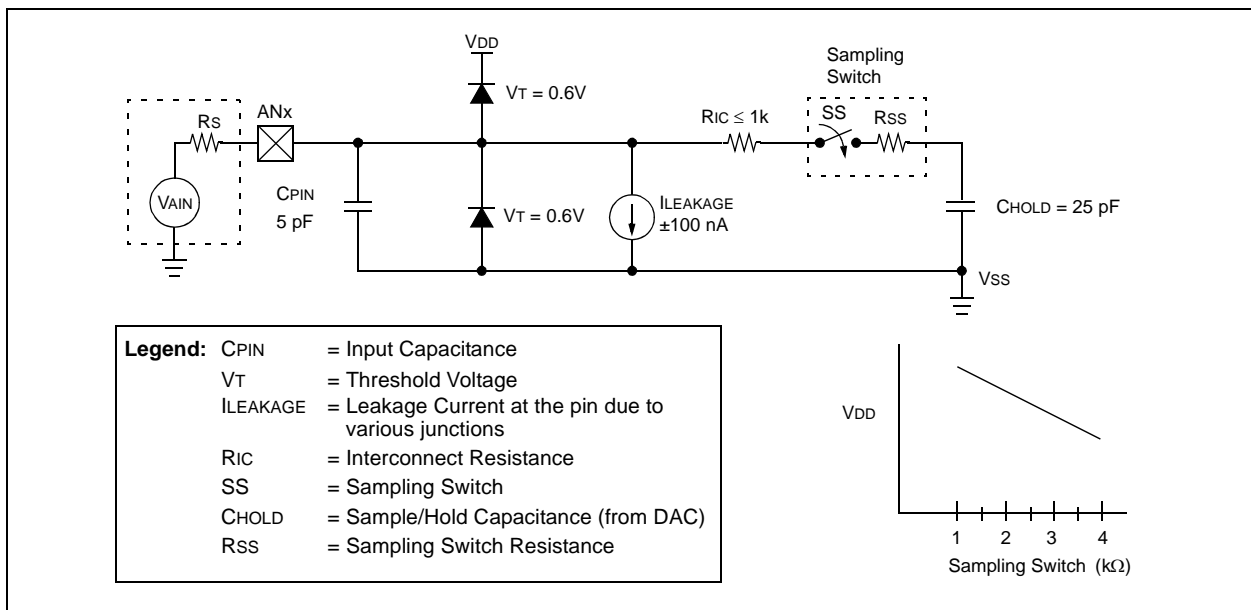
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After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as an input. To determine acquisition time, see **Section 2.1 “A/D Acquisition Requirements”**. After this acquisition time has elapsed, the A/D conversion can be started. An acquisition time can be programmed to occur between setting the GO/DONE bit and the actual start of the conversion.

The following steps should be followed to do an A/D conversion:

1. Configure the A/D module:
 - Configure analog pins, voltage reference and digital I/O (ADCON1)
 - Select A/D input channel (ADCON0)
 - Select A/D acquisition time (ADCON2)
 - Select A/D conversion clock (ADCON2)
 - Turn on A/D module (ADCON0)
2. Configure A/D interrupt (if desired):
 - Clear ADIF bit
 - Set ADIE bit
 - Set GIE bit
3. Wait the required acquisition time (if required).
4. Start conversion:
 - Set GO/DONE bit (ADCON0<1>)
5. Wait for A/D conversion to complete, by either:
 - Polling for the GO/DONE bit to be cleared
 - OR
 - Waiting for the A/D interrupt
6. Read A/D Result registers (ADRESH:ADRESL); clear ADIF bit, if required.
7. For next conversion, go to step 1 or step 2, as required. The A/D conversion time per bit is defined as TAD. A minimum wait of 2 TAD is required before next acquisition starts.

FIGURE 2-2: ANALOG INPUT MODEL



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2.1 A/D Acquisition Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 2-2. The source impedance (Rs) and the internal sampling switch (Rss) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (Rss) impedance varies over the device voltage (VDD). The source impedance affects the offset voltage at the analog input (due to pin leakage current). **The maximum recommended impedance for analog sources is 2.5 kΩ.** After the analog input channel is selected (changed), the channel must be sampled for at least the minimum acquisition time before starting a conversion.

Note: When the conversion is started, the holding capacitor is disconnected from the input pin.

To calculate the minimum acquisition time, Equation 2-1 may be used. This equation assumes that 1/2 LSb error is used (1,024 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

Equation 2-3 shows the calculation of the minimum required acquisition time, TACQ. This calculation is based on the following application system assumptions:

CHOLD	=	25 pF
Rs	=	2.5 kΩ
Conversion Error	≤	1/2 LSb
VDD	=	3V → Rss = 2 kΩ
Temperature	=	85°C (system max.)

EQUATION 2-1: ACQUISITION TIME

$$\begin{aligned} TACQ &= \text{Amplifier Settling Time} + \text{Holding Capacitor Charging Time} + \text{Temperature Coefficient} \\ &= TAMP + TC + TCOFF \end{aligned}$$

EQUATION 2-2: A/D MINIMUM CHARGING TIME

$$\begin{aligned} V_{HOLD} &= (V_{REF} - (V_{REF}/2048)) \cdot (1 - e^{-(TC/CHOLD)(RIC + R_{SS} + R_s)}) \\ \text{or} \\ TC &= -(CHOLD)(RIC + R_{SS} + R_s) \ln(1/2048) \end{aligned}$$

EQUATION 2-3: CALCULATING THE MINIMUM REQUIRED ACQUISITION TIME

$$\begin{aligned} TACQ &= TAMP + TC + TCOFF \\ TAMP &= 0.2 \mu s \\ TCOFF &= \begin{aligned} &(\text{Temp} - 25^\circ\text{C})(0.02 \mu s/^\circ\text{C}) \\ &(85^\circ\text{C} - 25^\circ\text{C})(0.02 \mu s/^\circ\text{C}) \\ &1.2 \mu s \end{aligned} \\ \text{Temperature coefficient is only required for temperatures } > 25^\circ\text{C. Below } 25^\circ\text{C, } TCOFF &= 0 \text{ ms.} \\ TC &= \begin{aligned} &-(CHOLD)(RIC + R_{SS} + R_s) \ln(1/2048) \mu s \\ &-(25 \text{ pF})(1 \text{ k}\Omega + 2 \text{ k}\Omega + 2.5 \text{ k}\Omega) \ln(0.0004883) \mu s \\ &1.05 \mu s \end{aligned} \\ TACQ &= \begin{aligned} &0.2 \mu s + 1 \mu s + 1.2 \mu s \\ &2.4 \mu s \end{aligned} \end{aligned}$$

2.2 Selecting and Configuring Automatic Acquisition Time

The ADCON2 register allows the user to select an acquisition time that occurs each time the GO/DONE bit is set.

When the GO/DONE bit is set, sampling is stopped and a conversion begins. The user is responsible for ensuring the required acquisition time has passed between selecting the desired input channel and setting the GO/DONE bit. This occurs when the ACQT<2:0> bits (ADCON2<5:3>) remain in their Reset state ('000') and is compatible with devices that do not offer programmable acquisition times.

If desired, the ACQT bits can be set to select a programmable acquisition time for the A/D module. When the GO/DONE bit is set, the A/D module continues to sample the input for the selected acquisition time, then automatically begins a conversion. Since the acquisition time is programmed, there may be no need to wait for an acquisition time between selecting a channel and setting the GO/DONE bit.

In either case, when the conversion is completed, the GO/DONE bit is cleared, the ADIF flag is set and the A/D begins sampling the currently selected channel again. If an acquisition time is programmed, there is nothing to indicate if the acquisition time has ended or if the conversion has begun.

2.3 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 11 TAD per 12-bit conversion. The source of the A/D conversion clock is software selectable.

There are seven possible options for TAD:

- 2 TOSC
- 4 TOSC
- 8 TOSC
- 16 TOSC
- 32 TOSC
- 64 TOSC
- Internal RC Oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be as short as possible but greater than the minimum TAD.

Table 2-1 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

TABLE 2-1: TAD vs. DEVICE OPERATING FREQUENCIES

AD Clock Source (TAD)		Maximum Device Frequency
Operation	ADCS<2:0>	
2 TOSC	000	2.86 MHz
4 TOSC	100	5.71 MHz
8 TOSC	001	11.43 MHz
16 TOSC	101	22.86 MHz
32 TOSC	010	40.0 MHz
64 TOSC	110	40.0 MHz
RC ⁽²⁾	x11	1.00 MHz ⁽¹⁾

- Note 1:** The RC source has a typical TAD time of 4 μs.
- 2:** For device frequencies above 1 MHz, the device must be in Sleep mode for the entire conversion or the A/D accuracy may be out of specification.

2.4 Configuring Analog Port Pins

The ADCON1, TRISA, TRISF and TRISH registers control the operation of the A/D port pins. The port pins needed as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the CHS<3:0> bits and the TRIS bits.

- Note 1:** When reading the PORT register, all pins configured as analog input channels will read as cleared (a low level). Pins configured as digital inputs will convert an analog input. Analog levels on a digitally configured input will be accurately converted.
- 2:** Analog levels on any pin defined as a digital input may cause the digital input buffer to consume current out of the device's specification limits.

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2.5 A/D Conversions

Figure 2-3 shows the operation of the A/D converter after the $\overline{\text{GO/DONE}}$ bit has been set and the $\text{ACQT}<2:0>$ bits are cleared. A conversion is started after the following instruction to allow entry into Sleep mode before the conversion begins.

Figure 2-4 shows the operation of the A/D converter after the $\overline{\text{GO/DONE}}$ bit has been set; the $\text{ACQT}<2:0>$ bits are set to '010' and a 4 TAD acquisition time is selected before the conversion starts.

Clearing the $\overline{\text{GO/DONE}}$ bit during a conversion will abort the current conversion. The A/D Result register pair will NOT be updated with the partially completed A/D conversion sample. This means the ADRESH:ADRESL registers will continue to contain the value of the last completed conversion (or the last value written to the ADRESH:ADRESL registers).

After the A/D conversion is completed or aborted, a 2 TAD wait is required before the next acquisition can be started. After this wait, acquisition on the selected channel is automatically started.

Note: The $\overline{\text{GO/DONE}}$ bit should NOT be set in the same instruction that turns on the A/D.

2.6 Use of the CCP2 Trigger

An A/D conversion can be started by the "Special Event Trigger" of the CCP2 module. This requires that the $\text{CCP2M}<3:0>$ bits ($\text{CCP2CON}<3:0>$) be programmed as '1011' and that the A/D module is enabled (ADON bit is set). When the trigger occurs, the $\overline{\text{GO/DONE}}$ bit will be set, starting the A/D acquisition and conversion, and the Timer1 (or Timer3) counter will be reset to zero. Timer1 (or Timer3) is reset to automatically repeat the A/D acquisition period with minimal software overhead (moving ADRESH:ADRESL to the desired location). The appropriate analog input channel must be selected and the minimum acquisition period is either timed by the user, or an appropriate TACQ time is selected before the Special Event Trigger sets the $\overline{\text{GO/DONE}}$ bit (starts a conversion).

If the A/D module is not enabled (ADON is cleared), the Special Event Trigger will be ignored by the A/D module but will still reset the Timer1 (or Timer3) counter.

FIGURE 2-3: A/D CONVERSION TAD CYCLES ($\text{ACQT}<2:0> = 000, \text{TACQ} = 0$)

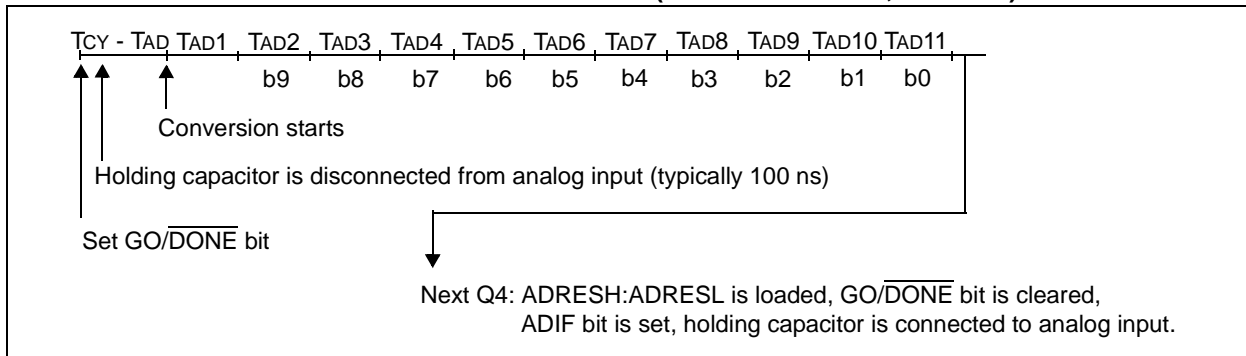
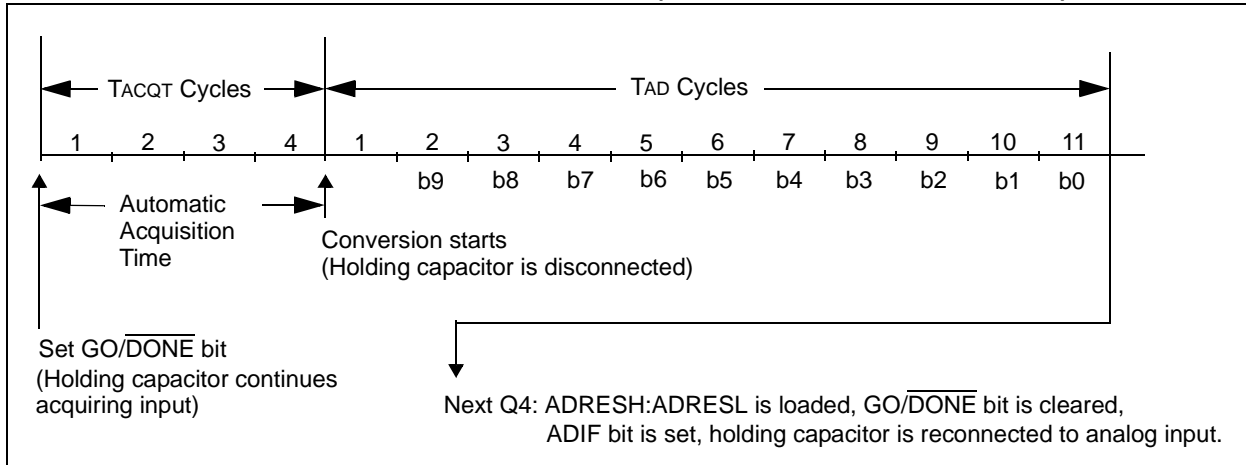


FIGURE 2-4: A/D CONVERSION TAD CYCLES ($\text{ACQT}<2:0> = 010, \text{TACQ} = 4 \text{TAD}$)



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2.7 A/D Converter Calibration

The A/D converter in the PIC18F87J93 family of devices includes a self-calibration feature which compensates for any offset generated within the module. The calibration process is automated and is initiated by setting the ADCAL bit (ADCON0<7>). The next time the GO/DONE bit is set, the module will perform a “dummy” conversion (which means it is reading none of the input channels) and store the resulting value internally to compensate for offset. Thus, subsequent offsets will be compensated.

The calibration process assumes that the device is in a relatively steady-state operating condition. If A/D calibration is used, it should be performed after each device Reset or if there are other major changes in operating conditions.

2.8 Operation in Power-Managed Modes

The selection of the automatic acquisition time and A/D conversion clock is determined in part by the clock source and frequency while in a power-managed mode.

If the A/D is expected to operate while the device is in a power-managed mode, the ACQT<2:0> and ADCS<2:0> bits in ADCON2 should be updated in accordance with the power-managed mode clock that will be used. After the power-managed mode is entered (either of the power-managed Run modes), an A/D acquisition or conversion may be started. Once an acquisition or conversion is started, the device should continue to be clocked by the same power-managed mode clock source until the conversion has been completed. If desired, the device may be placed into the corresponding power-managed Idle mode during the conversion.

If the power-managed mode clock frequency is less than 1 MHz, the A/D RC clock source should be selected.

Operation in Sleep mode requires the A/D RC clock to be selected. If bits, ACQT<2:0>, are set to ‘000’ and a conversion is started, the conversion will be delayed one instruction cycle to allow execution of the SLEEP instruction and entry to Sleep mode. The IDLEN and SCSx bits in the OSCCON register must have already been cleared prior to starting the conversion.

TABLE 2-2: SUMMARY OF A/D REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	2
PIR1	—	ADIF	RC1IF	TX1IF	SSPIF	—	TMR2IF	TMR1IF	2
PIE1	—	ADIE	RC1IE	TX1IE	SSPIE	—	TMR2IE	TMR1IE	2
IPR1	—	ADIP	RC1IP	TX1IP	SSPIP	—	TMR2IP	TMR1IP	2
PIR3	—	LCDIF	RC2IF	TX2IF	CTMUIF	CCP2IF	CCP1IF	RTCCIF	2
PIE3	—	LCDIE	RC2IE	TX2IE	CTMUIE	CCP2IE	CCP1IE	RTCCIE	2
IPR3	—	LCDIP	RC2IP	TX2IP	CTMUIP	CCP2IP	CCP1IP	RTCCIP	2
ADRESH	A/D Result Register High Byte								2
ADRESL	A/D Result Register Low Byte								2
ADCON0	ADCAL	—	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON	2
ADCON1	TRIGSEL	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	2
ADCON2	ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0	2
CCP2CON	—	—	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	2
PORTA	RA7 ⁽¹⁾	RA6 ⁽¹⁾	RA5	RA4	RA3	RA2	RA1	RA0	2
TRISA	TRISA7 ⁽¹⁾	TRISA6 ⁽¹⁾	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	2
PORTF	RF7	RF6	RF5	RF4	RF3	RF2	RF1	—	2
TRISF	TRISF5	TRISF4	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	—	2

Legend: — = unimplemented, read as ‘0’. Shaded cells are not used for A/D conversion.

Note 1: RA<7:6> and their associated latch and direction bits are configured as port pins only when the internal oscillator is selected as the default clock source (FOSC2 Configuration bit = 0); otherwise, they are disabled and these bits read as ‘0’.

2: For these Reset values, see **Section 4.0 “Reset”** of the “PIC18F87J90 Family Data Sheet” (DS39933).

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3.0 SPECIAL FEATURES OF THE CPU

Note 1: This section documents only the CPU features that are different from, or in addition to, the features of the PIC18F87J90 family devices.

2: For additional details on the Configuration bits, refer to **Section 24.1 “Configuration Bits”** in the *“PIC18F87J90 Family Data Sheet”* (DS39933).

3.1 Device ID Registers

The Device ID registers are “read-only” registers. They identify the device type and revision for device programmers and can be read by firmware using table reads.

TABLE 3-1: DEVICE ID REGISTERS

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value ⁽¹⁾	
3FFFFEh	DEVID1	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	xxxx xxxx ⁽²⁾
3FFFFFh	DEVID2	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	0000 10x1 ⁽²⁾

Legend: x = unknown, – = unimplemented. Shaded cells are unimplemented, read as ‘0’.

Note 1: Values reflect the unprogrammed state as received from the factory and following Power-on Resets. In all other Reset states, the configuration bytes maintain their previously programmed states.

2: See Register 3-1 and Register 3-2 for DEVID values. These registers are read-only and cannot be programmed by the user.

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REGISTER 3-1: DEVID1: DEVICE ID REGISTER 1 FOR PIC18F87J93 FAMILY DEVICES

R	R	R	R	R	R	R	R
DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0
bit 7							bit 0

Legend:

R = Read-only bit

bit 7-5 **DEV<2:0>**: Device ID bits

111 = PIC18F87J93

110 = PIC18F86J93

011 = PIC18F67J93

010 = PIC18F66J93

bit 4-0 **REV<4:0>**: Revision ID bits

These bits are used to indicate the device revision.

REGISTER 3-2: DEVID2: DEVICE ID REGISTER 2 FOR PIC18F87J93 FAMILY DEVICES

R	R	R	R	R	R	R	R
DEV10 ⁽¹⁾	DEV9 ⁽¹⁾	DEV8 ⁽¹⁾	DEV7 ⁽¹⁾	DEV6 ⁽¹⁾	DEV5 ⁽¹⁾	DEV4 ⁽¹⁾	DEV3 ⁽¹⁾
bit 7							bit 0

Legend:

R = Read-only bit

bit 7-0 **DEV<10:3>**: Device ID bits⁽¹⁾

These bits are used with the DEV<2:0> bits in the Device ID Register 1 to identify the part number.

0101 0000 = PIC18F87J93 family devices

Note 1: The values for DEV<10:3> may be shared with other device families. The specific device is always identified by using the entire DEV<10:0> bit sequence.

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4.0 ELECTRICAL CHARACTERISTICS

Note: Other than some basic data, this section documents only the PIC18F87J93 family devices' specifications that differ from those of the PIC18F87J90 family devices. For detailed information on the electrical specifications shared by the PIC18F87J93 family and PIC18F87J90 family devices, see the "PIC18F87J90 Family Data Sheet" (DS39933).

Absolute Maximum Ratings^(†)

Ambient temperature under bias	-40°C to +100°C
Storage temperature	-65°C to +150°C
Voltage on any digital only I/O pin or $\overline{\text{MCLR}}$ with respect to VSS (except VDD)	-0.3V to 6.0V
Voltage on any combined digital and analog pin with respect to VSS (except VDD and $\overline{\text{MCLR}}$).....	-0.3V to (VDD + 0.3V)
Voltage on VDDCORE with respect to VSS	-0.3V to 2.75V
Voltage on VDD with respect to VSS	-0.3V to 3.6V
Total power dissipation (Note 1)	1.0W
Maximum current out of VSS pin	300 mA
Maximum current into VDD pin	250 mA
Maximum output current sunk by PORTA<7:6> and any PORTB and PORTC I/O pins.....	25 mA
Maximum output current sunk by any PORTD, PORTE and PORTJ I/O pins	8 mA
Maximum output current sunk by PORTA<5:0> and any PORTF, PORTG and PORTH I/O pins	2 mA
Maximum output current sourced by PORTA<7:6> and any PORTB and PORTC I/O pins	25 mA
Maximum output current sourced by any PORTD, PORTE and PORTJ I/O pins	8 mA
Maximum output current sourced by PORTA<5:0> and any PORTF, PORTG and PORTH I/O pins	2 mA
Maximum current sunk by all ports combined	200 mA

Note 1: Power dissipation is calculated as follows:

$$P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$$

† **NOTICE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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FIGURE 4-1: VOLTAGE-FREQUENCY GRAPH, REGULATOR ENABLED (INDUSTRIAL)⁽¹⁾

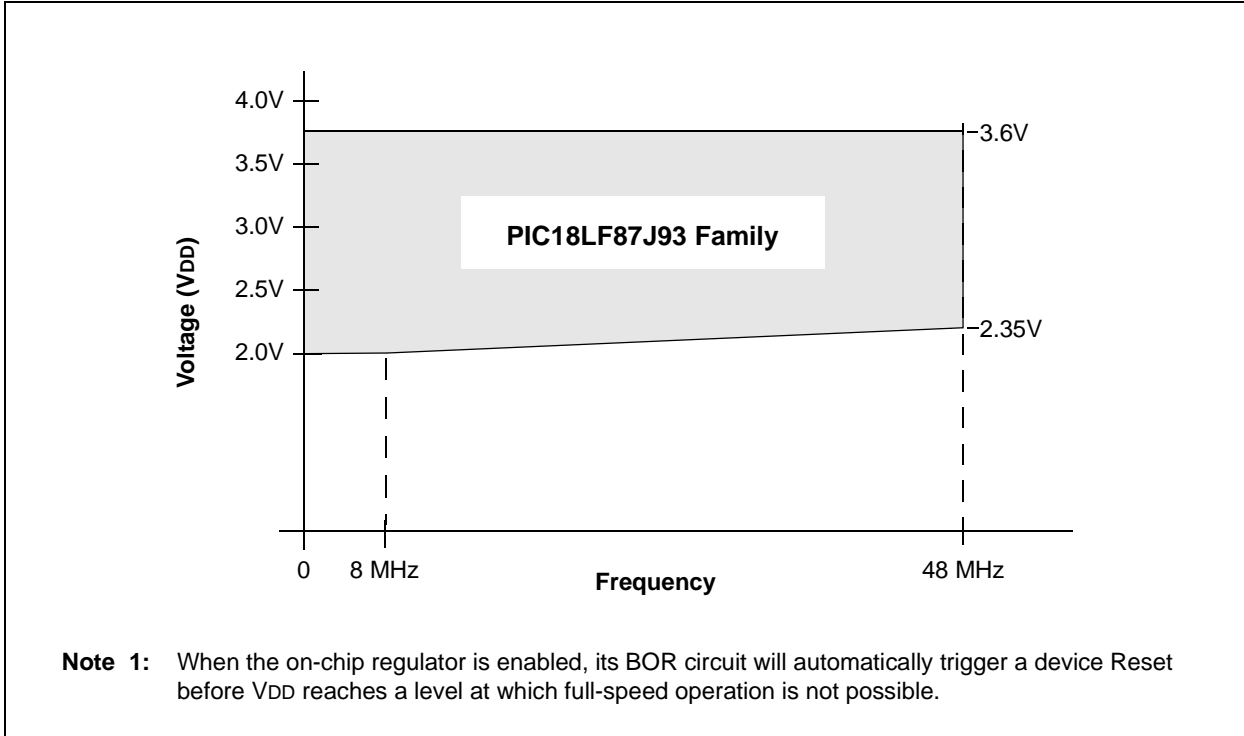
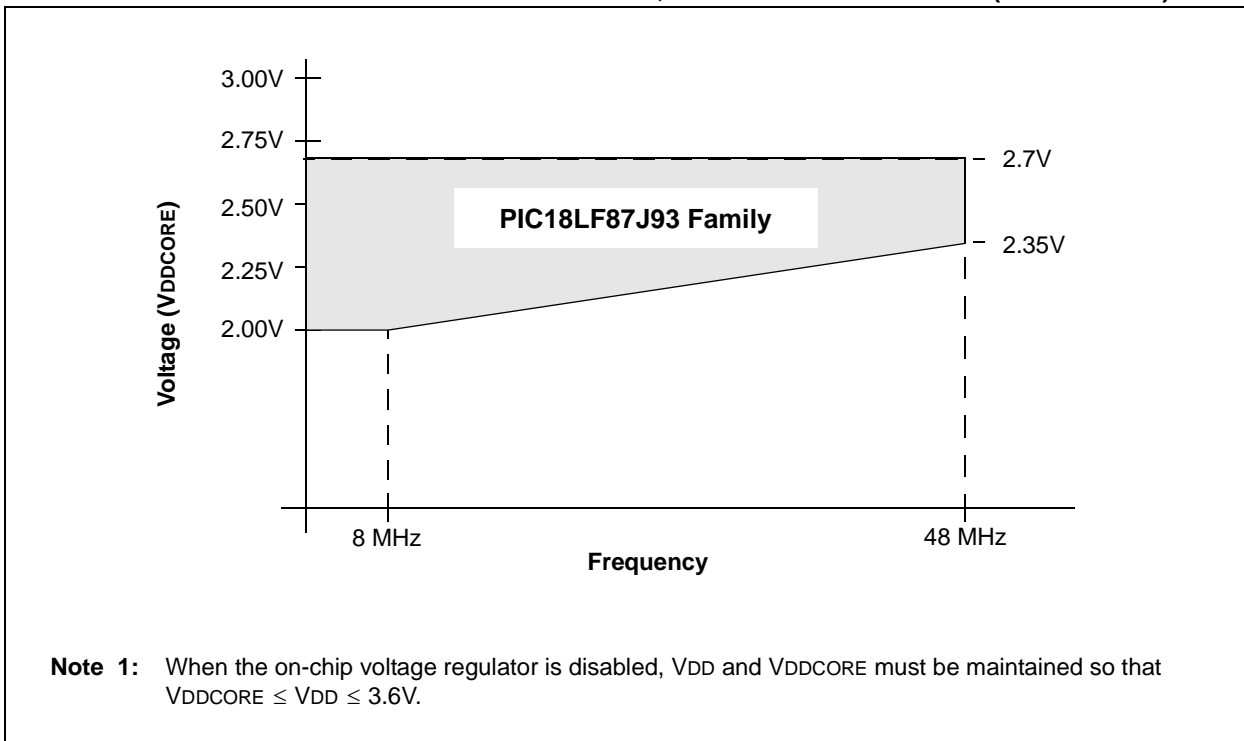


FIGURE 4-2: VOLTAGE-FREQUENCY GRAPH, REGULATOR DISABLED (INDUSTRIAL)⁽¹⁾



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TABLE 4-1: A/D CONVERTER CHARACTERISTICS: PIC18F87J93 FAMILY (INDUSTRIAL)

Param No.	Sym	Characteristic	Min	Typ	Max	Units	Conditions
A01	NR	Resolution	—	—	12	bit	$\Delta V_{REF} \geq 3.0V$
A03	EIL	Integral Linearity Error	—	$<\pm 1$	± 2.0	LSB	$\Delta V_{REF} \geq 3.0V$
A04	EDL	Differential Linearity Error	—	$<\pm 1$	± 1.5	LSB	$\Delta V_{REF} \geq 3.0V$
A06	E _{OFF}	Offset Error	—	$<\pm 1$	± 5	LSB	$\Delta V_{REF} \geq 3.0V$
A07	E _{GN}	Gain Error	—	$<\pm 1$	± 3	LSB	$\Delta V_{REF} \geq 3.0V$
A10	—	Monotonicity	Guaranteed ⁽¹⁾			—	$V_{SS} \leq V_{AIN} \leq V_{REF}$
A20	ΔV_{REF}	Reference Voltage Range (V _{REFH} – V _{REFL})	3	—	V _{DD} – V _{SS}	V	For 12-bit resolution
A21	V _{REFH}	Reference Voltage High	V _{SS} + 3.0V	—	V _{DD} + 0.3V	V	For 12-bit resolution
A22	V _{REFL}	Reference Voltage Low	V _{SS} – 0.3V	—	V _{DD} – 3.0V	V	For 12-bit resolution
A25	V _{AIN}	Analog Input Voltage	V _{REFL}	—	V _{REFH}	V	Note 2
A30	Z _{AIN}	Recommended Impedance of Analog Voltage Source	—	—	2.5	k Ω	
A50	I _{REF}	V _{REF} Input Current ⁽²⁾	—	—	5 150	μA μA	During V _{AIN} acquisition. During A/D conversion cycle.

Note 1: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

Note 2: V_{REFH} current is from the RA3/AN3/V_{REF+} pin or V_{DD}, whichever is selected as the V_{REFH} source. V_{REFL} current is from the RA2/AN2/V_{REF-}/CV_{REF} pin or V_{SS}, whichever is selected as the V_{REFL} source.

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FIGURE 4-3: A/D CONVERSION TIMING

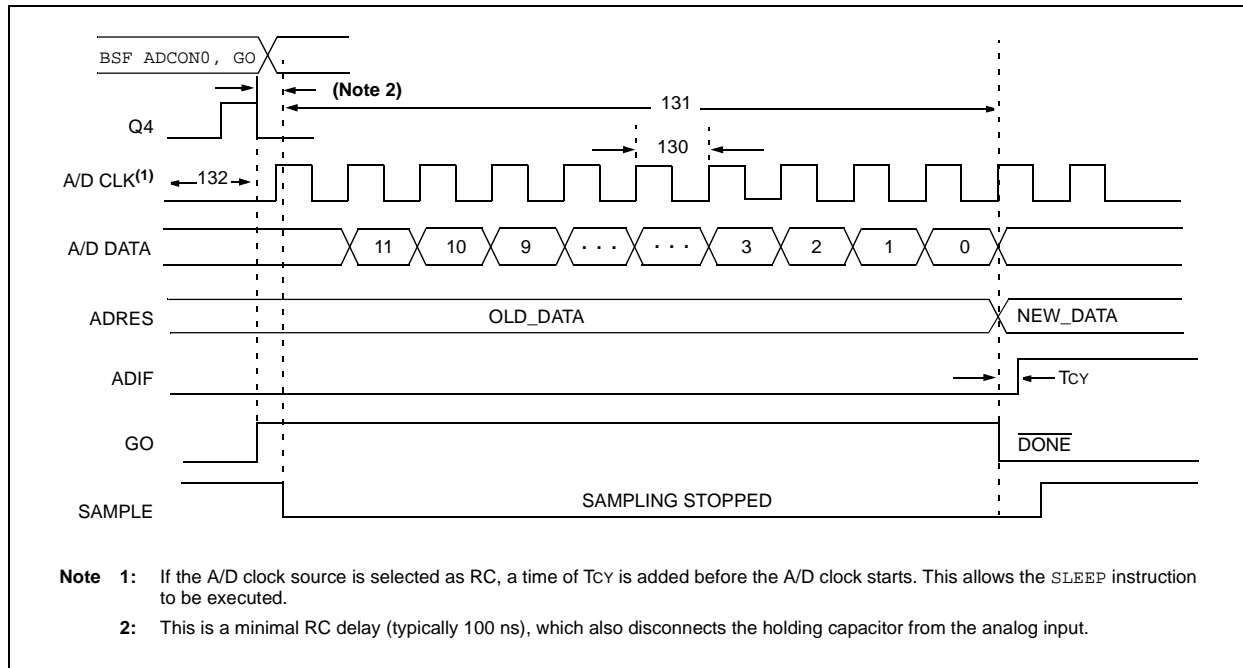


TABLE 4-2: A/D CONVERSION REQUIREMENTS

Param No.	Symbol	Characteristic	Min	Max	Units	Conditions
130	TAD	A/D Clock Period	0.8	12.5 ⁽¹⁾	μs	TOSC based, VREF ≥ 3.0V
131	T _{CNV}	Conversion Time (not including acquisition time) ⁽²⁾	13	14	TAD	
132	TACQ	Acquisition Time ⁽³⁾	1.4	—	μs	
135	T _{SWC}	Switching Time from Convert → Sample	—	(Note 4)		
137	T _{DIS}	Discharge Time	0.2	—	μs	

- Note 1:** The time of the A/D clock period is dependent on the device frequency and the TAD clock divider.
- Note 2:** ADRES registers may be read on the following T_{CY} cycle.
- Note 3:** The time for the holding capacitor to acquire the “New” input voltage when the voltage changes full scale after the conversion (VDD to VSS or VSS to VDD). The source impedance (R_S) on the input channels is 50Ω.
- Note 4:** On the following cycle of the device clock.

5.0 PACKAGING INFORMATION

For packaging information, see the “*PIC18F87J93 Family Data Sheet*” (DS39933).

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APPENDIX A: REVISION HISTORY

Revision A (June 2009)

Original data sheet for PIC18F87J93 family devices.

APPENDIX B: DEVICE DIFFERENCES

The differences between the devices listed in this data sheet are shown in Table B-1.

TABLE B-1: PIC18F87J93 FAMILY DEVICE DIFFERENCES

Features	PIC18F66J93	PIC18F67J93	PIC18F86J93	PIC18F87J93
Program Memory (Bytes)	64K	128K	64K	128K
Program Memory (Instructions)	32768	65536	32768	65536
Interrupt Sources	28	28	29	29
I/O Ports	Ports A, B, C, D, E, F, G	Ports A, B, C, D, E, F, G	Ports A, B, C, D, E, F, G, H, J	Ports A, B, C, D, E, F, G, H, J
Capture/Compare/PWM Modules	2	2	2	2
Enhanced Capture/Compare/PWM Modules	3	3	3	3
Packages	64-Pin TQFP	64-Pin TQFP	80-Pin TQFP	80-Pin TQFP

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APPENDIX C: CONVERSION CONSIDERATIONS

This appendix discusses the considerations for converting from previous versions of a device to the ones listed in this data sheet. Typically, these changes are due to the differences in the process technology used. An example of this type of conversion is from a PIC16C74A to a PIC16C74B.

Not Applicable

APPENDIX D: MIGRATION FROM BASELINE TO ENHANCED DEVICES

This section discusses how to migrate from a Baseline device (such as the PIC16C5X) to an Enhanced MCU device (such as the PIC18FXXX).

The following are the list of modifications over the PIC16C5X microcontroller family:

Not Currently Available

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Device ^(1,2)	PIC18F66J93, PIC18F66J93T PIC18F67J93, PIC18F67J93T PIC18F86J93, PIC18F86J93T PIC18F87J93, PIC18F87J93T		
Temperature Range	I = -40°C to +85°C (Industrial)		
Package	PT = TQFP (Thin Quad Flatpack)		
Pattern	QTP, SQTP, Code or Special Requirements (blank otherwise)		

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