Power Sequencing Controllers

The ISL6123, ISL6124, and ISL6125 are a family of four channel power sequencing controllers in a variety of functional and personality configurations. The ICs are designed for multiple-voltage systems that require arbitrary power sequencing of various ASIC and processor supply voltages.

The four channel **ISL6123** (ENABLE input), **ISL6124** (ENABLE# input) and **ISL6125** ICs offer the designer 4 rail control when it is required that all four rails are in minimal compliance prior to turn on and that compliance must be maintained during operation. The **ISL6123** has a low power standby mode when it is disabled, suitable for battery powered applications.

The **ISL6125** operates like the **ISL6124** but instead of charge pump driven gate drive outputs it has open drain logic outputs for direct interface to other circuitry.

External resistors provide flexible voltage threshold programming of monitored rail voltages. Delay and sequencing are provided by external capacitors for both ramp up and ramp down.

Each IC is provided with a RESET# output that deasserts once all monitored voltages are compliant. Additionally the IC has a SYSRST# input that immediately shuts down all outputs and asserts the RESET# signal.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6123IR	-40 to +85	24 Lead QFN	L24.4x4
ISL6124IR	-40 to +85	24 Lead QFN	L24.4x4
ISL6125IR	-40 to +85	24 Lead QFN	L24.4x4
ISL612XSEQEVAL1	Evaluation Platform		

Pinout

ISL6123, ISL6124, ISL6125 (24 LEAD QFN)
TOP VIEW

4mm x 4mm
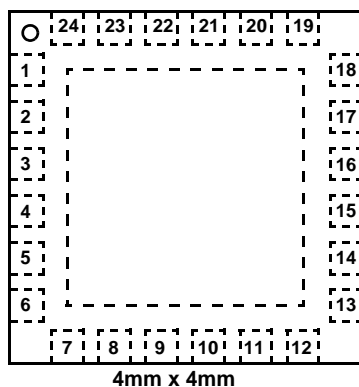
Features

- Enables arbitrary turn-on and turn-off sequencing of up to four power supplies (0.7V - 5V) in less area than 8 lead SOIC

- Operates from 1.5V to 5.5V supply voltage

- Supplies V_{DD} +5V of charge pumped gate drive

- Adjustable voltage slew rate for each rail

- Multiple sequencers can be daisy-chained to sequence an infinite number of independent supplies

- Glitch immunity

- Under voltage lockout for each supply

- Low Power Sleep State (**ISL6123**)

- Active high (**ISL6123**) or low (**ISL6124**) ENABLE# input

- Open drain version available (**ISL6125**)

- QFN Package:
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Package Outline
  - Near Chip Scale Package footprint, which improves PCB efficiency and has a thinner profile

Applications

- Graphics cards

- FPGA/ASIC/microprocessor/PowerPC supply sequencing

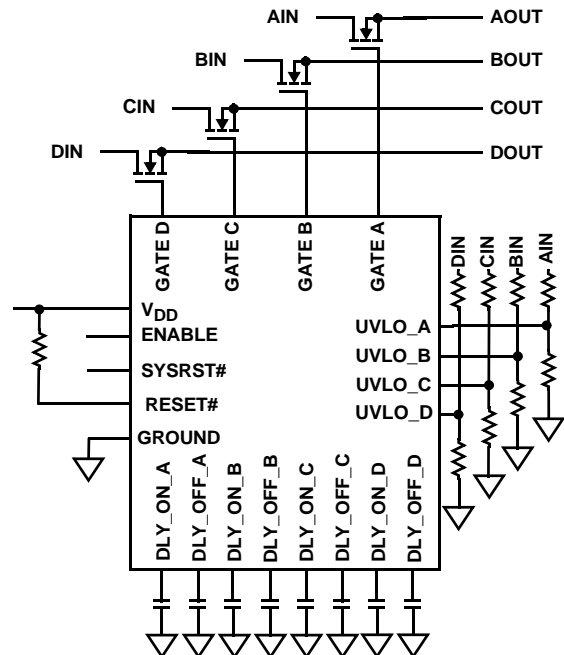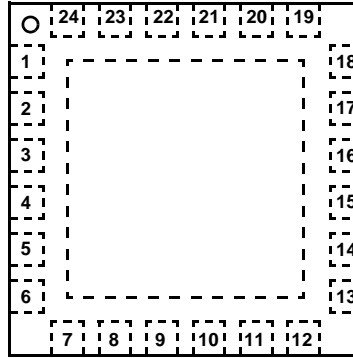- Network routers

- Telecommunications systems

FIGURE 1. TYPICAL ISL6123 APPLICATION USAGE

Pinout

4mm x 4mm

Pin Descriptions

PIN NUMBER	PIN NAME	FUNCTION	DESCRIPTION
	ISL6123/24 **ISL6125**		
23	V_{DD}	Chip Bias	Bias IC from 1.5V to 5.5V
10	GND	Bias Return	IC ground
1	ENABLE/ ENABLE#	Starts on/off sequencing of the power supplies.	Input to initiate the start of the programmed sequencing of supplies on or off. **ISL6123** has ENABLE. **ISL6124**, **ISL6125** have ENABLE#.
24	RESET#	Reset Output	RESET# provides a high signal ~160ms after all GATEs are fully enhanced. This delay is for stabilization of output voltages. RESET# will assert upon UVLO not being satisfied or ENABLE / ENABLE# being deasserted. The RESET# output is an open drain N channel FET and is guaranteed to be in the correct state for V_{DD} < 1V.
20	UVLO_A	Under Voltage Lock Out/Monitoring	These inputs provide for a programmable UV lockout referenced to an internal 0.633V reference and are filtered to ignore short (~ 30µs) transients below programmed UVLO level.
12	UVLO_B		
17	UVLO_C		
14	UVLO_D		
21	DLY_ON_A	Gate On Delay Timer Capacitor	Allows for programming the delay and sequence for VOUT turn-on. Each cap is charged with 1µA ~9ms after ENABLE / ENABLE# with an internal current source providing delay to the associated FETs turn-on.
8	DLY_ON_B		
16	DLY_ON_C		
15	DLY_ON_D		
18	DLY_OFF_A	Gate Off Delay Timer Capacitor	Allows for programming the sequence for Vout turn-off through ENABLE / ENABLE#. Each cap is charged with a 1µA internal current source to an internal reference voltage causing the corresponding gate to be pulled down turning-off the associated FET.
13	DLY_OFF_B		
3	DLY_OFF_C		
4	DLY_OFF_D		
2	GATE_A **LOGIC_A**	FET Gate Drive Output **ISL6125** Open Drain Outputs	Drives the external FETs with a 1µA current source to soft start ramp into the load. On the **ISL6125** only these are open drain inputs that can be pulled up to a maximum of V_{DD} voltage.
5	GATE_B **LOGIC_B**		
6	GATE_C **LOGIC_C**		
7	GATE_D **LOGIC_D**		
22	SYSRST#	System Reset	Allows for immediate unconditional latch-off of all GATE outputs when driven low. This input can also be used to initiate the programmed sequence with 'zero' wait (no 9ms stabilization delay) from input signal on this pin being driven high to first GATE.
9, 11, 19	No Connect	No Connect	No Connect

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ISL6123, ISL6124, ISL6125

Absolute Maximum Ratings

V$_{DD}$ . . . . +6.0V
GATE . . . . -0.3V to V$_{DD}$+6V
ISL6125 LOGIC OUT. -0.3V to V$_{DD}$ +0.3V
UVLO, ENABLE, ENABLE#, SYSRST# . . . . . . -0.3V to V$_{DD}$ +0.3V
DLY_ON, DLYOFF . . . . -0.3V to V$_{DD}$ +0.3V
ESD Classification . . . . 1.5kV (CDM)

Operating Conditions

V$_{DD}$ Supply Voltage Range . . . . +1.5V to +5.5V
Temperature Range (T$_A$) . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Notes 1, 2)   θ$_{JA}$ (^{o}C/W)   θ$_{JC}$ (^{o}C/W)
   4 x 4 QFN Package   48   9
Maximum Junction Temperature . . . . 150°C
Maximum Storage Temperature Range . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C
   (QFN - Leads Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ$_{JA}$ is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. For θ$_{JC}$, the "case temp" location is the center of the exposed metal pad on the package underside.
3. All voltages are relative to GND, unless otherwise specified.

Electrical Specifications   V$_{DD}$ = 1.5V to +5V, T$_A$ = T$_J$ = -40°C - 85°C, Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
UVLO						
Undervoltage Lockout Threshold	V$_{UVLOvth}$	T$_J$ = +25°C	619	633	647	mV
Undervoltage Lockout Threshold Temp Co	TC$_{UVLOvth}$	T$_J$ = -40°C to 85°C		40		nV/^{o}C
Undervoltage Lockout Hysteresis	V$_{UVLOhys}$		-	10	-	mV
Undervoltage Lock out Threshold Range	RUVLOvth	Max V$_{UVLOvth}$ - Min V$_{UVLOvth}$		7		mV
Undervoltage Lock out Delay	TUVLOdel	ENABLE satisfied		9		ms
Transient Filter Duration	TFIL	V$_{DD}$, UVLO, ENABLE glitch filter		30		μs
DELAY ON / OFF						
Delay Charging Current	DLY_ichg	V$_{DLY}$ = 0V	0.92	1	1.08	μA
Delay Charging Current Range	DLY_ichg_r	DLY_ichg(max) - DLY_ichg(min)		0.08		μA
Delay Charging Current Temp. Coeff.	TC_DLY_ichg			0.2		nA/^{o}C
Delay Threshold Voltage	DLY_Vth		1.238	1.266	1.294	V
Delay Threshold Voltage Temp. Coeff.	TC_DLY_Vth			0.2		mV/^{o}C
ENABLE / ENABLE#, RESET# & SYSRST# I/O						
ENABLE Threshold	V$_{ENh}$			1.2		V
ENABLE# Threshold	V$_{ENh}$			V$_{DD}$/2		V
ENABLE / ENABLE# Hysteresis	V$_{ENh}$ -V$_{ENl}$	Measured at V$_{DD}$ = 1.5V		0.2		V
ENABLE / ENABLE# Lock out Delay	TdelEN_LO	UVLO satisfied		9		ms
RESET# Pull-Down Current	I$_{\overline{RST}pd}$	$\overline{RST}$ = 0.1V		13		mA
RESET# Delay after GATE High	T$_{\overline{RST}del}$	GATE = V$_{DD}$+5V		160		ms
RESET# Output Low	V$_{\overline{RST}l}$	Measured at V$_{DD}$ = 1V			0.001	V
SYSRST# Low to GATE Turn-off	T$_{delSYS\_G}$	GATE = 80% of V$_{DD}$+5V		40		ns
GATE						
GATE Turn-On Current	I$_{GATEon}$	GATE = 0V	0.85	1	1.25	μA
GATE Turn-Off Current	I$_{GATEoff\_l}$	GATE = V$_{DD}$, Disabled	-1.25	-1	-0.85	μA
GATE Turn-On/Off Current Temp. Coeff.	TC_I$_{GATE}$			0.2		nA/^{o}C
GATE Pull-Down High Current	I$_{GATEoff\_h}$	GATE = V$_{DD}$, UVLO = 0V		88		mA
GATE High Voltage	V$_{GATEh}$	Gate High Voltage	V$_{DD}$+5V	V$_{DD}$+5.3V	-	V
GATE Low Voltage	V$_{GATE\_}$	Gate Low Voltage, V$_{DD}$ = 1V	-	0	0.1	V

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Electrical Specifications V_{DD} = 1.5V to +5V, T_A = T_J = -40°C - 85°C, Unless Otherwise Specified. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS						
IC Supply Current	I_{VDD_5V}	V_{DD} = 5V		0.20	0.5	mA
IC Supply Current	$I_{VDD\_3.3V}$	V_{DD} = 3.3V		0.14		mA
IC Supply Current	$I_{VDD\_1.5V}$	V_{DD} = 1.5V		0.10		mA
ISL6123 Stand By IC Supply Current	I_{VDD_sb}	V_{DD} = 5V, ENABLE = 0V		100		μA
V_{DD} Power On Reset	V_{DD_POR}				1	V

ISL6123, ISL6124, ISL6125 Descriptions and Operation

The **ISL6123, ISL6124, ISL6125** sequencer family consists of several four channel voltage sequencing controllers in various functional and personality configurations. All are designed for use in multiple-voltage systems requiring power sequencing of various supply voltages. Individual voltage rails are gated on and off by external N-Channel MOSFETs, the gates of which are driven by an internal charge pump to V_{DD} +5V (VQP) in a user programmed sequence.

With the four-channel **ISL6123** the ENABLE must be asserted and all four voltages to be sequenced must be above their respective user programmed Under Voltage Lock Out (UVLO) levels before programmed output turn on sequencing can begin. Sequencing and delay determination is accomplished by the choice of external cap values on the DLY_ON and DLY_OFF pins. Once all 4 UVLO inputs and ENABLE are satisfied for ~ 9ms, the four DLY_ON caps are simultaneously charged with 1μA current sources to the DLY_Vth level of ~ 1.27V. As each DLY_ON pin reaches the DLY_Vth level its associated GATE will then turn-on with a 1μA source current to the VQP voltage of V_{DD}+5V. Thus all four GATEs will sequentially turn on. Once at DLY_Vth the DLY_ON pins will discharge to be ready when next needed. After the entire turn on sequence has been completed and all GATEs have reached the charge pumped voltage (VQP), a 160ms delay is started to ensure stability after which the RESET# output will be released to go high. Subsequent to turn-on, if any input falls below its UVLO point for longer than the glitch filter period (~ 30μs) this is considered a fault. RESET# is asserted low and all GATEs are simultaneously pulled low. In this mode the GATEs are pulled low with 88mA. Normal shutdown mode is entered when no UVLO is violated and the ENABLE is deasserted. When ENABLE is deasserted, RESET# is asserted and pulled low. Next, all four shutdown ramp caps on the DLY_OFF pins are charged with a 1μA source and when any ramp-cap reaches DLY_Vth, a latch is set and a current is sunk on the respective GATE pin to turn off its external MOSFET. When the GATE voltage is approximately 0.6V, the GATE is pulled down the rest of the way at a higher current level. Each individual external FET is thus turned off removing the voltages from the load in the programmed sequence.

The **ISL6123** and **ISL6124** have the same functionality except for the ENABLE active polarity with the **ISL6124** having an ENABLE# input. Additionally the **ISL6123** also has an ultra low power sleep state when ENABLE is low.

The **ISL6125** has the same personality as the **ISL6124** but instead of charged pump driven GATE outputs it has open drain LOGIC outputs that can be pulled up to a maximum of V_{DD}.

During bias up the RESET# output is guaranteed to be in the correct state with V_{DD} lower than 1V.

The SYSRST# input once asserted low unconditionally shuts off all GATEs, see Figure 6. This input can be used as a no wait enabling input, if all inputs (ENABLE & UVLO) are satisfied. It is also useful when multiple sequencers are implemented in a design needing simultaneous shutdown (kill switch) across all sequencers.

After a fault, restart of the turn on sequence is automatic once all requirements are met. This allows for no interaction between the sequencer and a controller IC if desired. The ENABLE & RESET# I/O do allow for a higher level of feedback and control if desired.

If no capacitors are connected between DLY_ON or DLY_OFF pins and ground then all such related GATEs start to turn on immediately after the ~ 9ms($T_{UVLOdel}$) ENABLE stabilization time out has expired and the GATEs start to immediately turn off when ENABLE is asserted.

Table 1 illustrates the nominal time delay from the start of charging to the 1.24V reference for various capacitor values on the DLY_ON and DLY_OFF pins. This table does not include the ~ 9ms of enable lock out delay during a start up sequence but represents the time from the end of the enable lock out delay to the start of GATE transition. There is no enable lock out delay for a sequence off, so this table illustrates the delay to GATE transition from a disable signal. Bold fields in table illustrate most likely used range of delay periods.

TABLE 1.

NOMINAL DELAY TO SEQUENCING THRESHOLD	
DLY PIN CAPACITANCE	**TIME (s)**
Open	0.00006
100pF	0.00013
1000pF	**0.0013**
0.01μF	**0.013**
0.1μF	0.13
1μF	1.3
10μF	13

NOTE: Nom. T_{DEL_SEQ} = Cap (μF) * 1.3MΩ.

Figure 2 illustrates the turn-on and Figure 3 the nominal turnoff timing diagram of the **ISL6123** and **ISL6124** product.

The **ISL6125** is similar except the open drains instead of GATE pins are pulled up to V_{DD}.

Note the delay and flexible sequencing possibilities.
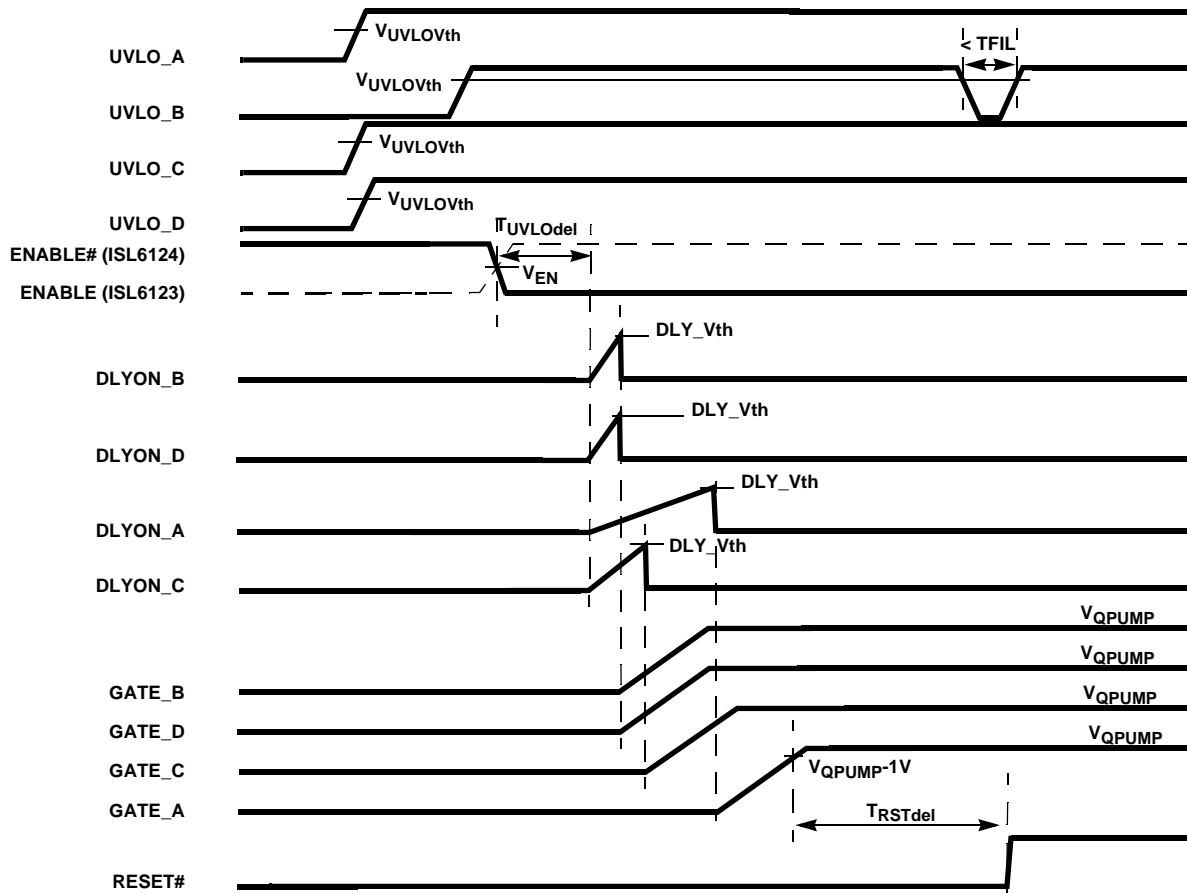
FIGURE 2. ISL6123/ISL6124 TURN-ON AND GLITCH RESPONSE TIMING DIAGRAM

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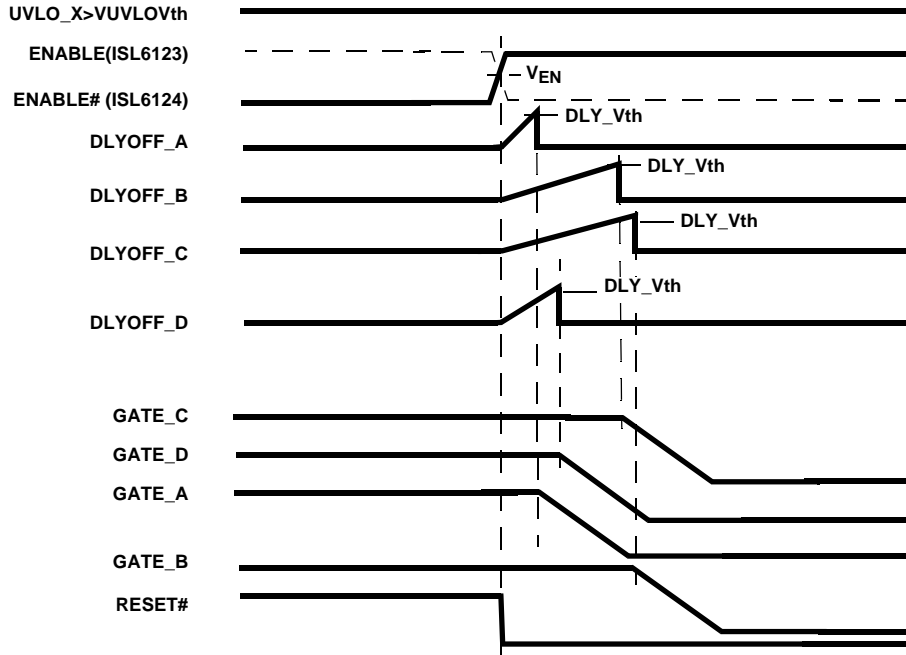
FIGURE 3. ISL6123/ISL6124 TURN-OFF TIMING DIAGRAM

Typical Performance Curves
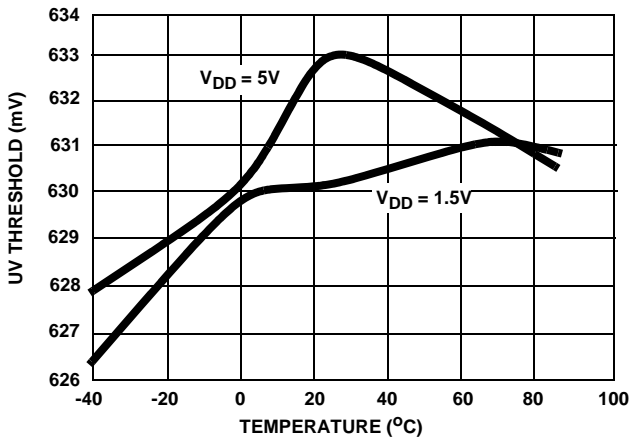
FIGURE 4. UVLO THRESHOLD VOLTAGE
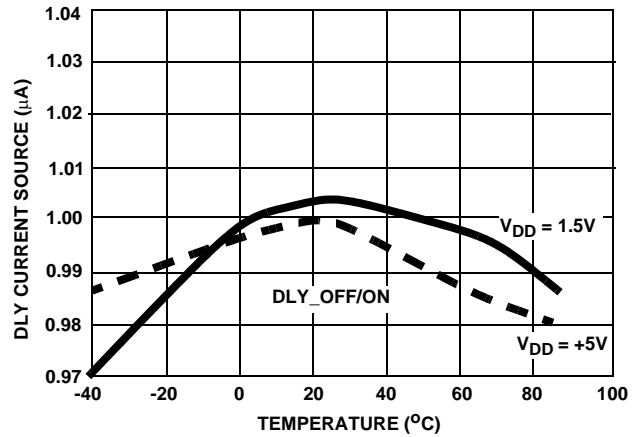
FIGURE 5. DLY CHARGE CURRENT

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Typical Performance Curves (Continued)
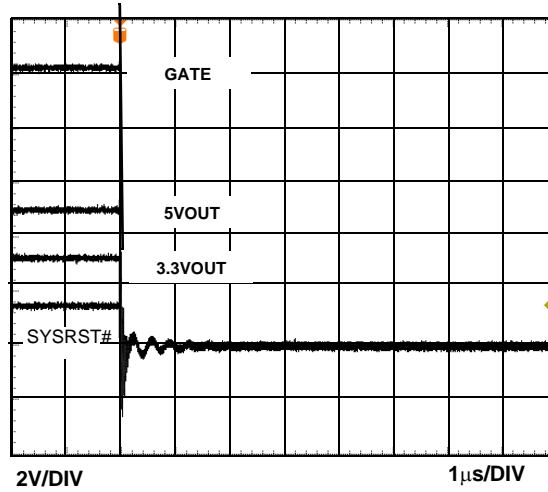

2V/DIV   **1μs/DIV**

FIGURE 6. SYSRST# LOW TO OUTPUT LATCH OFF

Using the ISL612XSEQEVAL1 Platform

The **ISL612XSEQEVAL1** platform is the primary evaluation board for this family. The board has 2 complete, separate and electrically identical circuits, see Figure 11 for schematic and Figure 12 for a photo.

In the top right hand corner of the board is a SMD layout with a **ISL6123** illustrating the full functionality and small implementation size for an application having the highest component count.

The majority of the board is given over to a socket and discrete through-hole components circuit for ease of evaluation flexibility through IC variant swapping and modification of UVLO levels and sequencing order by passive component substitution.

The board is shipped with the **ISL6123** installed in both locations and with two each of the other released variant types loose packed. As this sequencer family has a common function pinout there are no major modifications to the board necessary to evaluate the other ICs. The **ISL6125** due to its having open drain outputs can be evaluated on the **ISL612XSEQEVAL1** with a minor modification or on the **ISL613XSUPEREVAL2** evaluation platform. To modify for **ISL6125** evaluation, pull-up resistors must be added from the GATE outputs to a pull-up voltage of 1.5V to prevent FET turn-on or remove FETs to eliminate this voltage restriction.

To the left, right and above the socket are four test point strips (TP1-TP4). These give access to the labeled IC I/O pins during evaluation. Remember that significant current or capacitive loading of particular I/O pins will affect functionality and performance.

Attention to orientation and placement of variant ICs in the socket must be paid to prevent IC damage or faulty evaluation.

The default configuration of the **ISL612XSEQEVAL1** circuitries was built around the following design presumptions:

1. Using the **ISL6123IR** or **ISL6124IR**

2. The four supplies being sequenced are 5V (IN_A), 3.3V (IN_B), 2.5V (IN_C) and 1.5V (IN_D), the UVLO levels are ~ 80% of nominal voltages. Resistors chosen such that the total resistance of each divider is ~ 10K using standard value resistors to approximate 80% of nominal = 0.63V on UVLO input.

3. The desired order turn-on sequence is first both 5V and 3.3V supplies together and then the 2.5V supply about 75ms later and lastly the 1.5V supply about 45ms later.

4. The desired turn-off sequence is first both 1.5V and 3.3V supplies at the same time then the 2.5V supply about 50ms later and lastly the 5V supply about 72ms after that.

Figures 7 and 8 illustrate the desired turn-on and turn-off sequences respectively. The sequencing order and delay between voltages sequencing is set by external capacitance values so other than illustrated can be accomplished.

Figures 9 and 10 illustrate the timing relationships between the EN input, RESET#, DLY and GATE outputs and the VOUT voltage for a single channel being turned on and off respectively. RESET# is not shown in Figure 9 as it asserts 160ms after the last GATE goes high.
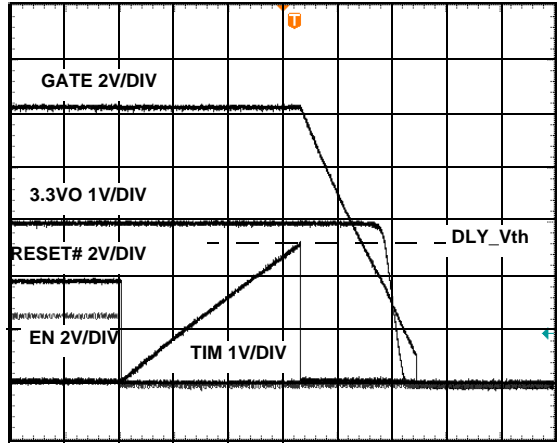
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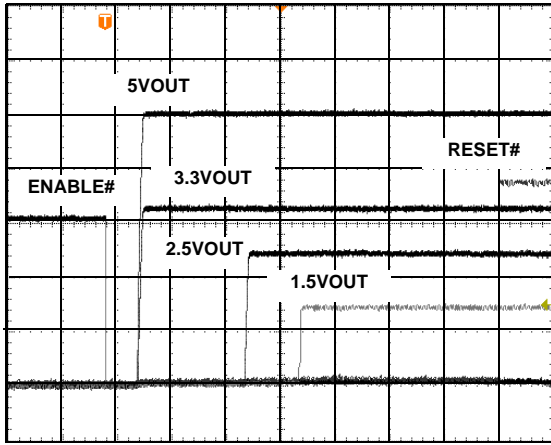
1V/DIV   **40ms/DIV**

FIGURE 7. ISL6124 SEQUENCED TURN-ON
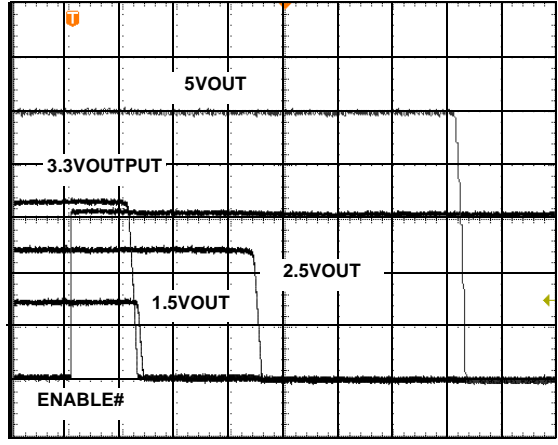
1V/DIV   **20ms/DIV**

FIGURE 8. ISL6124 SEQUENCED TURN-OFF
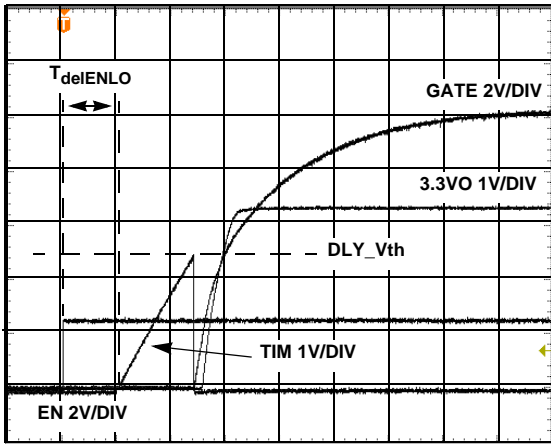
10ms/DIV

FIGURE 9. ISL6123 SINGLE CHANNEL TURN-ON

4ms/DIV

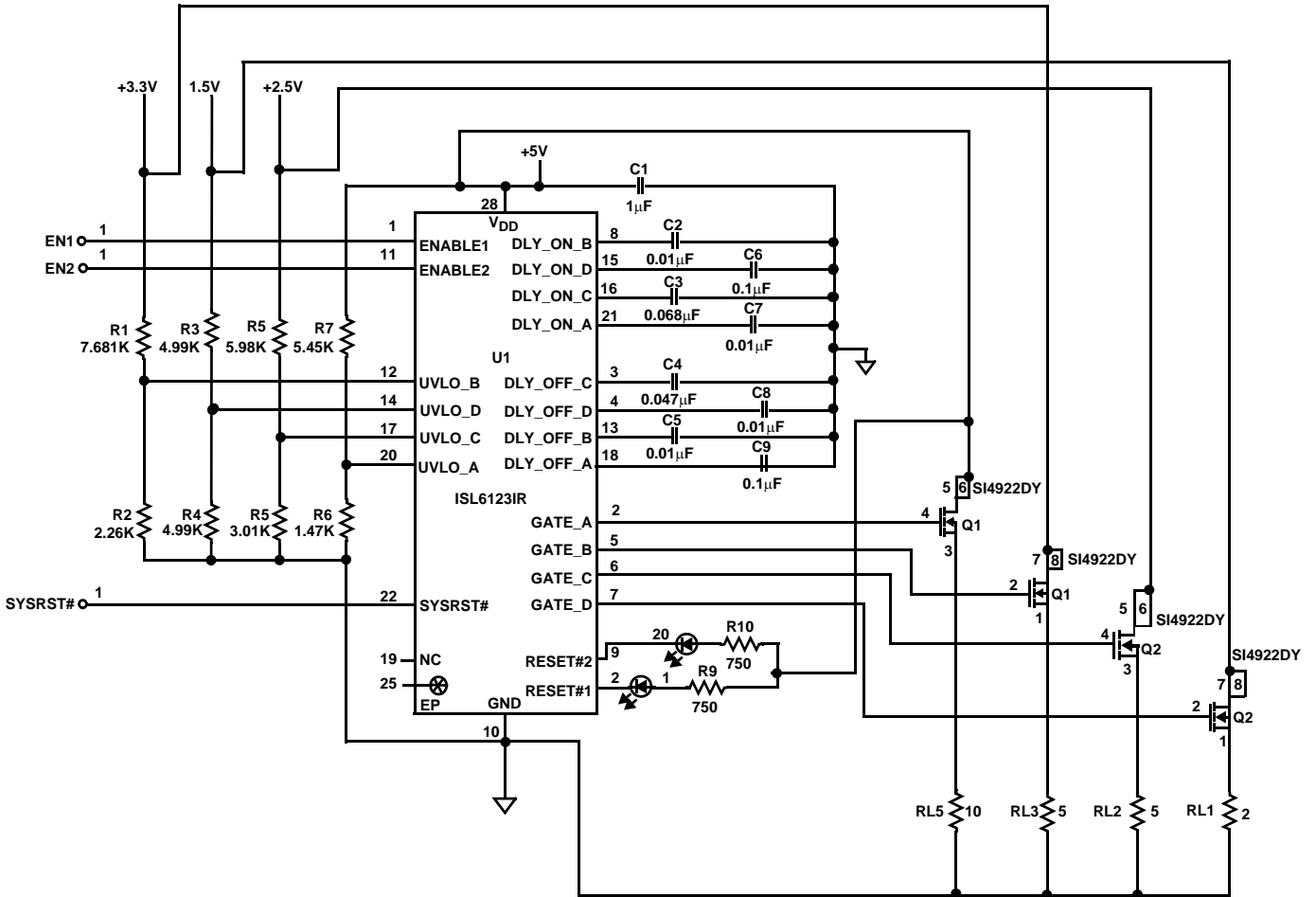**FIGURE 10. ISL6123 SINGLE CHANNEL TURN-OFF**
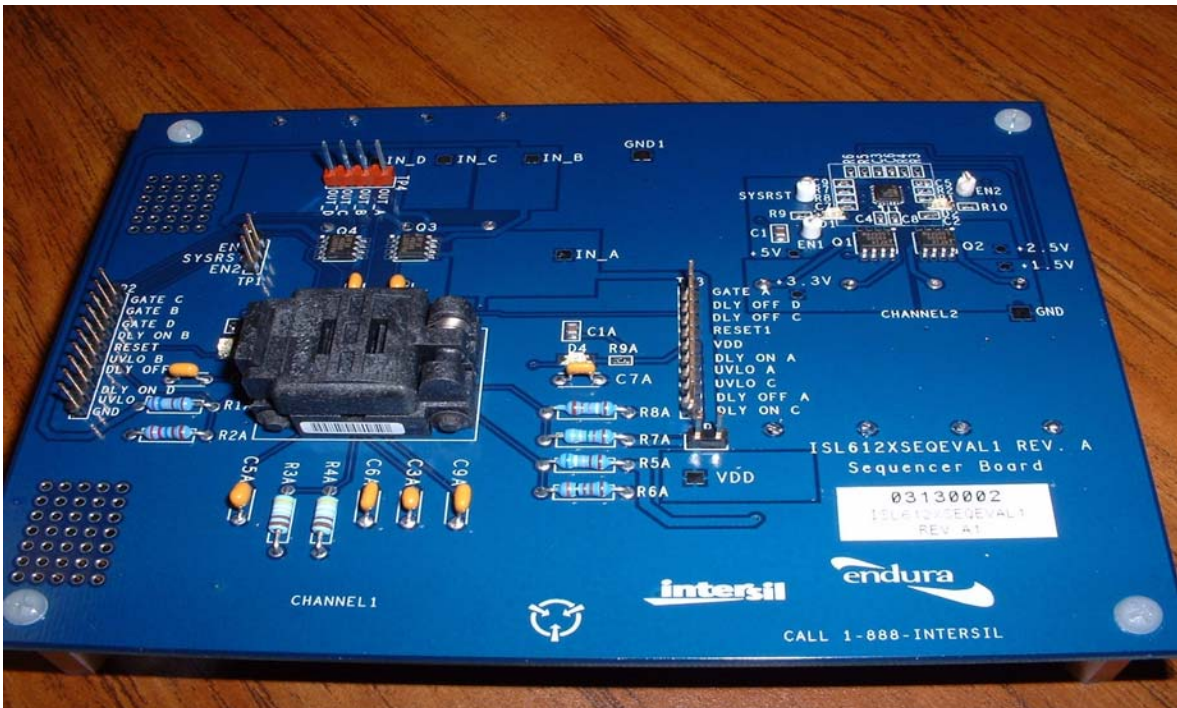
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FIGURE 11. EVAL BOARD SCHEMATIC

FIGURE 12. EVAL BOARD PHOTO

TABLE 1. ISL612XSEQEVAL1 BOARD COMPONENT LISTING

COMPONENT DESIGNATOR	COMPONENT FUNCTION	COMPONENT DESCRIPTION
DUT1	**ISL6124**, 4 Supply Sequencer	Intersil, **ISL6124IR** 4 Supply Sequencer
Q1, Q2	Voltage Rail Switches	SI4922DY or equiv, Dual 8A, 30V, 0.018Ω, N-Channel MOSFET
R7	5V to UVLO_A Resistor for Divider String	8.45kΩ 1%, 0402
R8	UVLO_A to GND Resistor for Divider String	1.47kΩ 1%, 0402
R1	3.3V to UVLO_B Resistor for Divider String	7.68kΩ 1%, 0402
R2	UVLO_B to GND Resistor for Divider String	2.26kΩ 1%, 0402
R5	2.5V to UVLO_C Resistor for Divider String	6.98kΩ 1%, 0402
R6	UVLO_C to GND Resistor for Divider String	3.01kΩ 1%, 0402
R3	1.5V to UVLO_D Resistor for Divider String	4.99kΩ 1%, 0402
R4	UVLO_D to GND Resistor for Divider String	4.99kΩ 1%, 0402
R9	RESET#1 LED Current Limiting Resistor	750Ω 10%, 0805
R10	RESET#2 LED Current Limiting Resistor	750Ω 10%, 0805
C7	5V turn-on Delay Cap. (13ms)	0.01μF 10%, 6.3V, 0402
C9	5V turn-off Delay Cap. (130ms)	0.1μF 10%, 6.3V, 0402
C2	3.3V turn-on Delay Cap. (13ms)	0.01μF 10%, 6.3V, 0402
C5	3.3V turn-off Delay Cap. (3ms)	0.01μF 10%, 6.3V, 0402
C3	2.5V turn-on Delay Cap. (88ms)	0.068μF 10%, 6.3V, 0402
C4	2.5V turn-off Delay Cap. (61ms)	0.047μF 10%, 6.3V, 0402
C6	1.5V turn-on Delay Cap. (130ms)	0.1μF 10%, 6.3V, 0402
C8	1.5V turn-off Delay Cap. (13ms)	0.01μF 10%, 6.3V, 0402
C1	Decoupling Capacitor	0.1μF, 0805
D1	RESET#1 Indicating LED	0805, SMD LEDs Red
D2	RESET#2 Indicating LED	0805, SMD LEDs Red
TP1 - TP24	Test Points Number Corresponds to DUT Pin Number	
RL5	5V Load Resistor	10Ω 20%, 3W Carbon
RL3	3.3V Load Resistor	5Ω 20%, 3W Carbon
RL2	2.5V Load Resistor	5Ω 20%, 3W Carbon
RL1	1.5V Load Resistor	2Ω 20%, 3W Carbon

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)

L24.4x4

24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VGGD-2 ISSUE C)
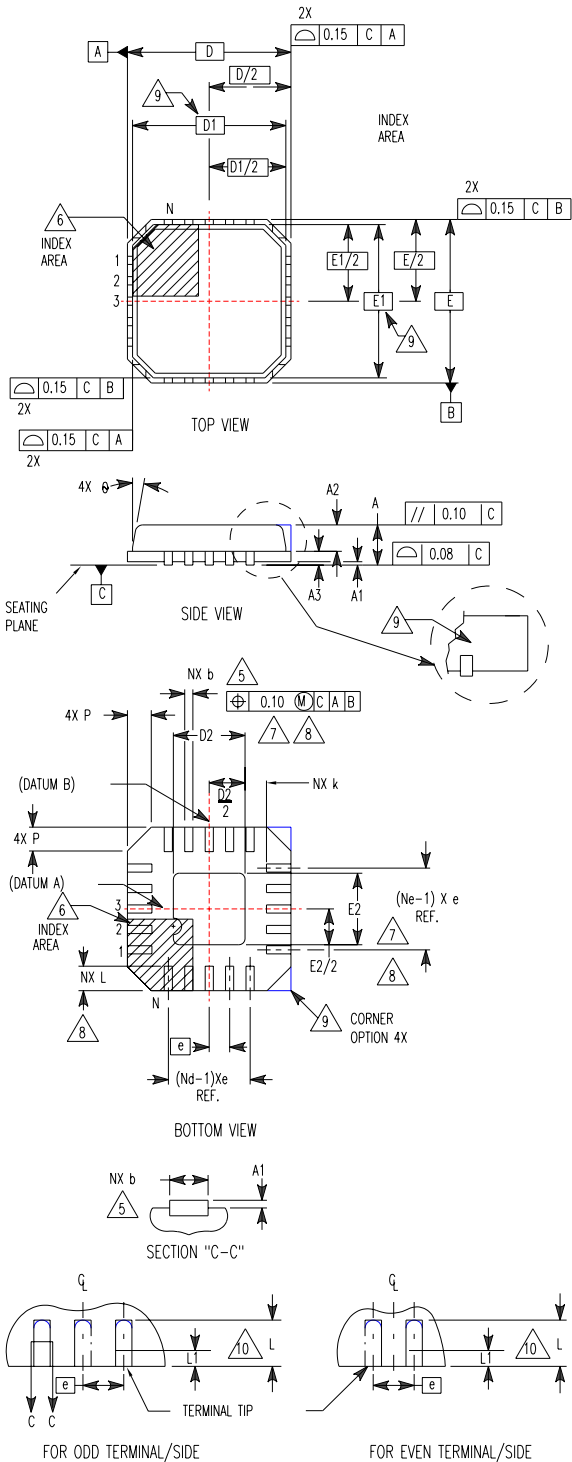
SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3	0.20 REF			9
b	0.18	0.23	0.30	5, 8
D	4.00 BSC			-
D1	3.75 BSC			9
D2	1.95	2.10	2.25	7, 8
E	4.00 BSC			-
E1	3.75 BSC			9
E2	1.95	2.10	2.25	7, 8
e	0.50 BSC			-
k	0.25	-	-	-
L	0.30	0.40	0.50	8
L1	-	-	0.15	10
N	24			2
Nd	6			3
Ne	6			3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 2 10/02

TOP VIEW

SIDE VIEW

BOTTOM VIEW

SECTION "C-C"

FOR ODD TERMINAL/SIDE

FOR EVEN TERMINAL/SIDE

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.

2. N is the number of terminals.

3. Nd and Ne refer to the number of terminals on each D and E.

4. All dimensions are in millimeters. Angles are in degrees.

5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.

6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.

8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.

9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.

10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
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