Kodak

DEVICE
PERFORMANCE
SPECIFICATION

KODAK KSC-3000 Color Processor

Real time color processor for megapixel progressive-scan imaging systems

May 8, 2003

Rev. 1.0

www.kodak.com/go/imagers 585-722-4385 Email: imagers@kodak.com

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Copyright Notice

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Figure 1 - Xilinx Copyright

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Device Description

Architecture

The KSC-3000 is implemented in a single Xilinx Virtex II device part number XC2V1000. An architectural overview of this device is shown in Figure 2 - Xilinx Virtex II Overview. For more complete information use this URL. http://direct.xilinx.com/bvdocs/publications/ds031-1.pdf

Virtex-II Array Overview

Virtex-II devices are user-programmable gate arrays with various configurable elements. The Virtex-II architecture is optimized for high-density and high-performance logic designs. As shown in Figure 1, the programmable device is comprised of input/output blocks (IOBs) and internal configurable logic blocks (CLBs).

Programmable I/O blocks provide the interface between package pins and the internal configurable logic. Most popular and leading-edge I/O standards are supported by the programmable IOBs.

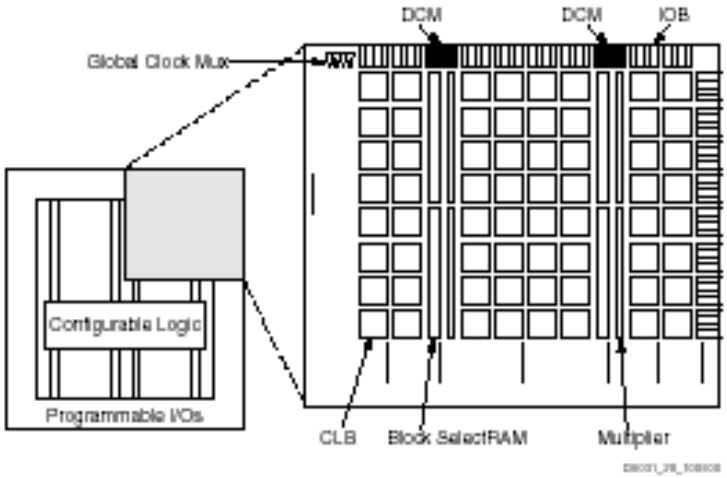


Figure 1: Virtex-II Architecture Overview

Figure 2 - Xilinx Virtex II Overview

Functional Description

The KSC-3000 is image-processing code designed to work with the Kodak KAI-1020CM interline CCD, which incorporate color filter arrays. The KSC-3000 provides all the processing steps required to convert the raw image into a full color image at 30 frames per second. The KSC-3000 provides a number of controls that allow the user to set various input image parameters to control the processing done on the image.

The KSC-3000 has three interfaces. The first is a three wire serial interface. This interface allows setup, algorithm control and configuration, and status read back. The second is the input data interface. The interface consists of the 10 bit data values, a frame valid indication, and a line valid indication. The third is the output data interface. The interface consists of 24 bit data values (8 bits each for red, green, and blue), a frame valid indication, and a line valid indication.

The KSC-3000 datapath is illustrated in Figure 3, a brief description of each block is given here. Most digital imagers use a single color image sensor that provides only one color value for each pixel. In this case, the pixels on the image sensor are covered with a mosaic of transmissive filters (typically red, green and blue), commonly known as a color filter array (CFA). Many digital cameras use the "Bayer" pattern CFA, named after its inventor, Kodak scientist Bryce Bayer. In the "Bayer" CFA pattern, 50% of the pixels are green, 25% are red, and 25% are blue. (The human eye gets most of its sharpness information from green light, which is why the CFA pattern was designed to have more green pixels.)

To get a good color image, the processing must provide white balancing. While both daylight and indoor lighting provide "white" light, daylight actually has more energy in the blue portion of the light spectrum and indoor lighting provides more energy in the red portion of the spectrum. Your eyes and brain automatically adapt to this difference, so that a white piece of paper appears white under all normal lighting conditions. An image sensor, by itself, cannot compensate for the illumination. Therefore, the image-processing datapath allows the user to adjust the red and blue signal strengths to match the green signal strength in white and neutral areas of the picture.

To create a complete full-color image, a digital image-processing step called CFA interpolation is used to "fill in" the missing color values for each pixel. Interpolation takes the sequence of single-channel color pixels and creates a full three-channel RGB color image. A sophisticated algorithm decides if the "missing" color values are in a smooth

area of the image or along an edge, and adaptively determines the best digital code value to use for each missing color value. Interpolation provides a full-color, but not yet perfect, image.

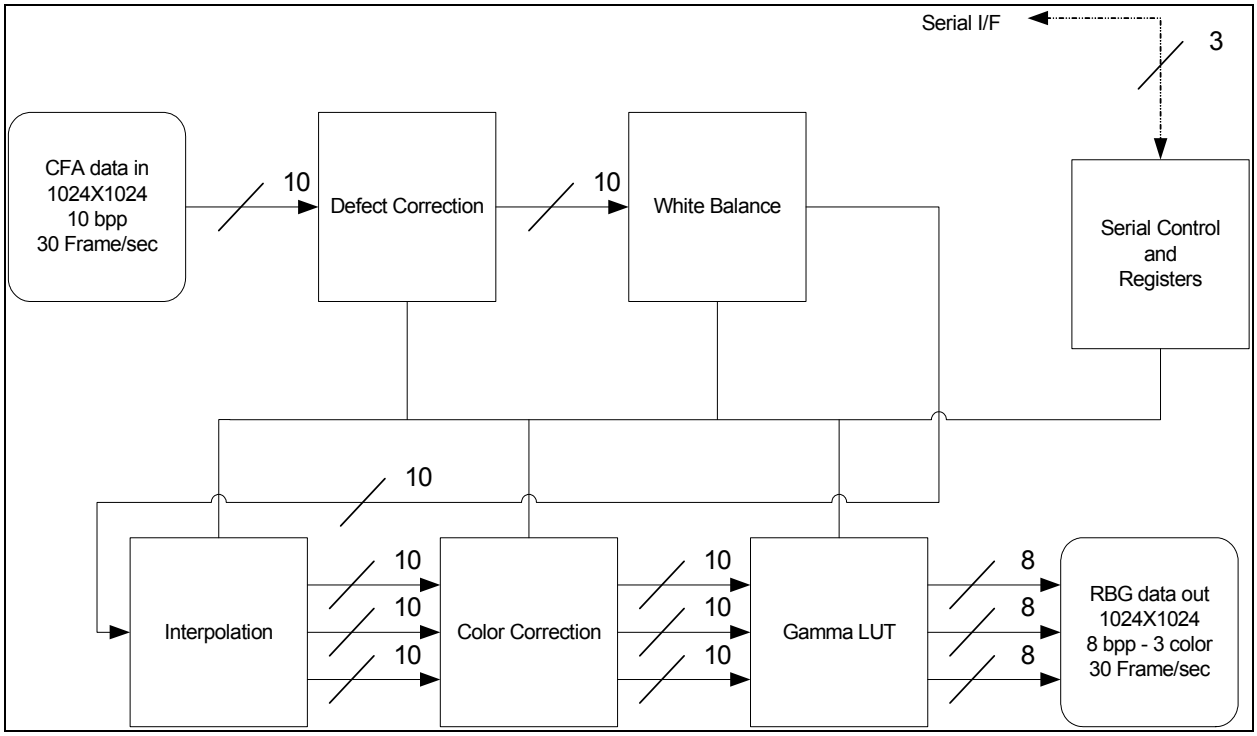


Figure 3 - Image Processing Chain Block Diagram

The next step in the image processing chain is color correction. The RGB spectral sensitivities of the image sensor do not perfectly match the way your eyes see colors. As a result, the color image typically appears desaturated, muting bright colors like red and blue. Color correction digitally compensates for this, improving the color reproduction.

The final step is to transform the digital image into the output color space. The default output color space used is described in Equation 1 - Gamma Calculation. This color space is used because it is designed to be ready for display on a typical monitor. It does the conversion using a gamma correction of 0.45 (when using its default settings).

$$\text{if } (x \le 0.018) \text{ then}$$
$$y = 4.5 * x$$
$$\text{else}$$
$$y = (1.099 * (x^{0.45})) - 0.099$$

For 10 bit data x is normalized using $\left(x = \frac{x}{1023} \right)$.

A CRT has a non-linear response with a gamma of 2.2.

The above compensation computes a gamma of $\left(\frac{1}{2.2} \right)$.

Equation 1 - Gamma Calculation

It is possible for the user to change this conversion by loading the GammaLUT with new values to alter the gamma conversion performed by the KSC-3000.

In addition to the image processing chain shown in Figure 3 the KSC-3000 contains an image scaling block and internal diagnostic elements. These consist of a paxel generator, a test image generator (TIG), and a signature generator (SIG). The TIG and SIG elements can be commanded via the serial interface to pass data through the entire image processing chain and verify correct operation. The TIG is internally connected to the inputs and the SIG is internally connected to the outputs.

The paxel generator is essentially a block to scale the image to a smaller size. A small representation of the image can be useful for additional image calculations. The paxelizer control register specifies the number of lines and pixels per paxel block, and the location to begin generating paxels. The hardware then generates a new image representation that is 36 x 24 elements. The data consists of four elements for each paxel (one for each of the Bayer pattern locations within each paxel). The paxel data is appended to the end of the image data stream of every frame. Due to bandwidth limitations only 12 bits of each paxel element value is output with two 12 bit values produced per clock cycle. Any data values in the last three lines that are not used for paxel data will be filled with zeros.

The TIG can be programmed to use a linear feedback shift register (LFSR) to produce pseudo-random data or it can be programmed to produce various patterns. For more information about the data it can generate see Table 8 – KSC-3000 Memory Map. The data can be programmed to occur one or more times.

The SIG also uses a multiple input shift register (MISR) to accumulate data and provide a unique signature for a given data stream. The TIG and SIG can be used in combination to provide a built-in self test (BIST) capability. The value it produces is available for read back via a register, see Table 8 – KSC-3000 Memory Map.

Physical Description

The following table lists the user I/O. The remainder of the I/O, other than power, ground, and programming pins, is unused. For information on how to connect the programming interface please refer to the board reference schematic.

Click on the following link to reference complete Xilinx pinout information.
http://direct.xilinx.com/bvdocs/publications/ds031-4.pdf

Pin Number	Signal Name	Pin Usage	Pin Name	Direction	IO Std	IO Bank	Drive (mA)	Slew Rate	Pullup Pulldown	IOB Delay
AC5	SerData	IOB	IO_L06P_5	BIDIR	LVTTL	5	12	SLOW	NONE	IFD
AD11	ClockIn	IOB	IO_L96P_5/GCLK6P	INPUT	LVTTL	5				NONE

AB2	FrameValidIn	IOB	IO_L01P_6	INPUT	LVTTL	6			Pulldown	IFD
AB12	LineValidIn	IOB	IO_L95P_5/GCLK4P	INPUT	LVTTL	5			Pulldown	IFD
R1	PixelIn(0)	IOB	IO_L52N_6	INPUT	LVTTL	6				IFD
T2	PixelIn(1)	IOB	IO_L54N_6	INPUT	LVTTL	6				IFD
T1	PixelIn(2)	IOB	IO_L52P_6	INPUT	LVTTL	6				IFD
U1	PixelIn(3)	IOB	IO_L49N_6	INPUT	LVTTL	6				IFD
U2	PixelIn(4)	IOB	IO_L49P_6	INPUT	LVTTL	6				IFD
V2	PixelIn(5)	IOB	IO_L24N_6	INPUT	LVTTL	6				IFD
W1	PixelIn(6)	IOB	IO_L22N_6	INPUT	LVTTL	6				IFD
Y1	PixelIn(7)	IOB	IO_L22P_6	INPUT	LVTTL	6				IFD
AA1	PixelIn(8)	IOB	IO_L21P_6	INPUT	LVTTL	6				IFD
AB1	PixelIn(9)	IOB	IO_L01N_6	INPUT	LVTTL	6				IFD
AC17	PixelValidIn	IOB	IO_L22P_4	INPUT	LVTTL	4			Pulldown	NONE
AD21	PLD_CFG_RST_n	IOB	IO_L01P_4/INIT_B	INPUT	LVTTL	4				NONE
AD17	ResetAsync	IOB	IO_L52N_4	INPUT	LVTTL	4			Pullup	NONE
W13	SerClock	IOB	IO_L95P_4/GCLK2P	INPUT	LVTTL	4				NONE
AD4	SerLoad	IOB	IO_L19P_5	INPUT	LVTTL	5				NONE
AA20	SPR_D0	IOB	IO_L02N_4/D0	INPUT	LVTTL	4				NONE
R20	BPixelOut(0)	IOB	IO_L51N_3/VREF_3	OUTPUT	LVTTL	3	8	FAST	NONE	
U19	BPixelOut(1)	IOB	IO_L43N_3	OUTPUT	LVTTL	3	8	FAST	NONE	
T20	BPixelOut(2)	IOB	IO_L52P_3	OUTPUT	LVTTL	3	8	FAST	NONE	
U20	BPixelOut(3)	IOB	IO_L43P_3	OUTPUT	LVTTL	3	8	FAST	NONE	
V20	BPixelOut(4)	IOB	IO_L02N_3/VRP_3	OUTPUT	LVTTL	3	8	FAST	NONE	
W20	BPixelOut(5)	IOB	IO_L03P_3	OUTPUT	LVTTL	3	8	FAST	NONE	
U18	BPixelOut(6)	IOB	IO_L01N_3	OUTPUT	LVTTL	3	8	FAST	NONE	
T19	BPixelOut(7)	IOB	IO_L24N_3	OUTPUT	LVTTL	3	8	FAST	NONE	
AA24	ClockOut	IOB	IO_L19N_3	OUTPUT	LVTTL	3	8	FAST	NONE	
W24	FrameValidOut	IOB	IO_L49N_3	OUTPUT	LVTTL	3	8	FAST	NONE	
N20	GPixelOut(0)	IOB	IO_L94N_3	OUTPUT	LVTTL	3	8	FAST	NONE	
N19	GPixelOut(1)	IOB	IO_L93N_3/VREF_3	OUTPUT	LVTTL	3	8	FAST	NONE	
N17	GPixelOut(2)	IOB	IO_L91N_3	OUTPUT	LVTTL	3	8	FAST	NONE	
R17	GPixelOut(3)	IOB	IO_L22P_3	OUTPUT	LVTTL	3	8	FAST	NONE	
R19	GPixelOut(4)	IOB	IO_L51P_3	OUTPUT	LVTTL	3	8	FAST	NONE	
T18	GPixelOut(5)	IOB	IO_L24P_3	OUTPUT	LVTTL	3	8	FAST	NONE	
P17	GPixelOut(6)	IOB	IO_L91P_3	OUTPUT	LVTTL	3	8	FAST	NONE	
R18	GPixelOut(7)	IOB	IO_L22N_3	OUTPUT	LVTTL	3	8	FAST	NONE	
G3	LedGrnSink_n(0)	IOB	IO_L43P_7	OUTPUT	LVTTL	7	8	SLOW	NONE	
F2	LedGrnSink_n(1)	IOB	IO_L48N_7	OUTPUT	LVTTL	7	8	SLOW	NONE	

E2	LedGrnSink_n(2)	IOB	IO_L19N_7	OUTPUT	LVTTL	7	8	SLOW	NONE
D3	LedGrnSink_n(3)	IOB	IO_L06N_7	OUTPUT	LVTTL	7	8	SLOW	NONE
G2	LedRedSink_n(0)	IOB	IO_L46N_7	OUTPUT	LVTTL	7	8	SLOW	NONE
F1	LedRedSink_n(1)	IOB	IO_L48P_7	OUTPUT	LVTTL	7	8	SLOW	NONE
E1	LedRedSink_n(2)	IOB	IO_L19P_7	OUTPUT	LVTTL	7	8	SLOW	NONE
D2	LedRedSink_n(3)	IOB	IO_L06P_7	OUTPUT	LVTTL	7	8	SLOW	NONE
W23	LineValidOut	IOB	IO_L49P_3	OUTPUT	LVTTL	3	8	FAST	NONE
Y24	PixelValidOut	IOB	IO_L21N_3/VREF_3	OUTPUT	LVTTL	3	8	FAST	NONE
U23	RPixelOut(0)	IOB	IO_L48N_3	OUTPUT	LVTTL	3	8	FAST	NONE
T23	RPixelOut(1)	IOB	IO_L54N_3	OUTPUT	LVTTL	3	8	FAST	NONE
V22	RPixelOut(2)	IOB	IO_L45N_3/VREF_3	OUTPUT	LVTTL	3	8	FAST	NONE
U22	RPixelOut(3)	IOB	IO_L46N_3	OUTPUT	LVTTL	3	8	FAST	NONE
T22	RPixelOut(4)	IOB	IO_L54P_3	OUTPUT	LVTTL	3	8	FAST	NONE
N22	RPixelOut(5)	IOB	IO_L96P_3	OUTPUT	LVTTL	3	8	FAST	NONE
V23	RPixelOut(6)	IOB	IO_L48P_3	OUTPUT	LVTTL	3	8	FAST	NONE
N23	RPixelOut(7)	IOB	IO_L96N_3	OUTPUT	LVTTL	3	8	FAST	NONE
D22	TestBusOut(0)	IOB	IO_L01N_2	OUTPUT	LVTTL	2	8	SLOW	NONE
D23	TestBusOut(1)	IOB	IO_L01P_2	OUTPUT	LVTTL	2	8	SLOW	NONE
G20	TestBusOut(10)	IOB	IO_L04N_2	OUTPUT	LVTTL	2	8	SLOW	NONE
G19	TestBusOut(11)	IOB	IO_L04P_2	OUTPUT	LVTTL	2	8	SLOW	NONE
J22	TestBusOut(12)	IOB	IO_L52N_2	OUTPUT	LVTTL	2	8	SLOW	NONE
J23	TestBusOut(13)	IOB	IO_L52P_2	OUTPUT	LVTTL	2	8	SLOW	NONE
H18	TestBusOut(14)	IOB	IO_L06N_2	OUTPUT	LVTTL	2	8	SLOW	NONE
J17	TestBusOut(15)	IOB	IO_L06P_2	OUTPUT	LVTTL	2	8	SLOW	NONE
D24	TestBusOut(2)	IOB	IO_L19N_2	OUTPUT	LVTTL	2	8	SLOW	NONE
E23	TestBusOut(3)	IOB	IO_L19P_2	OUTPUT	LVTTL	2	8	SLOW	NONE
E24	TestBusOut(4)	IOB	IO_L21N_2	OUTPUT	LVTTL	2	8	SLOW	NONE
F24	TestBusOut(5)	IOB	IO_L21P_2/VREF_2	OUTPUT	LVTTL	2	8	SLOW	NONE
E21	TestBusOut(6)	IOB	IO_L02N_2/VRP_2	OUTPUT	LVTTL	2	8	SLOW	NONE
E22	TestBusOut(7)	IOB	IO_L02P_2/VRN_2	OUTPUT	LVTTL	2	8	SLOW	NONE
F21	TestBusOut(8)	IOB	IO_L03N_2	OUTPUT	LVTTL	2	8	SLOW	NONE
F20	TestBusOut(9)	IOB	IO_L03P_2/VREF_2	OUTPUT	LVTTL	2	8	SLOW	NONE
M23	TestClockOut	IOB	IO_L91N_2	OUTPUT	LVTTL	2	8	SLOW	NONE

Table 1 - KSC-3000 User I/O

The next table, Table 2 - Diagonstic Connections, lists the names and functions of extra signals that are available. Some of them may are of value to the user as indications of status and activity. Other signals were for debug use and are of no value to the user.

Pin Name	Pin Function	Reference Board Connection
LedGrnSink_n(0)	KSC-3000 is successfully programmed	DS-4 Greeen
LedGrnSink_n(1)	Serial I/F control register bit 0	DS-3 Green
LedGrnSink_n(2)	Signature 0 match	DS-1 Green
LedGrnSink_n(3)	Signature 1 match	DS-2 Green
LedRedSink_n(0)	General Serial I/F error	DS-4 Red
LedRedSink_n(1)	Invalid Serial I/F address	DS-3 Red
LedRedSink_n(2)	Invalid Serial I/F data word size	DS-1 Red
LedRedSink_n(3)	Invalid Serial I/F register write	DS-2 Red
TestBusOut	Not used	Header

Table 2 - Diagonstic Connections

The circuit board design in the Reference Design section, uses full surface mount technology. The fine line ball grid array package for the FPGA is an advanced circuit board technology. To enable the high pad count on the FPGA to be used on the small circuit board (2" x 2") the circuit board was fabricated using 8 layers with micro vias and buried vias. There are no vias that go completely through the board from the top layer to the bottom layer. Part of the design process included a full power analysis of the board and components to ensure a reliable power source for the FPGA.

It should be noted that this design used a larger part and package than required to allow for experimentation. A product version of this design could easily be implemented in a smaller device and package to lower costs.

Figure 4 shows the package outline drawing. The figure shows the reference mark used to locate pin 1.

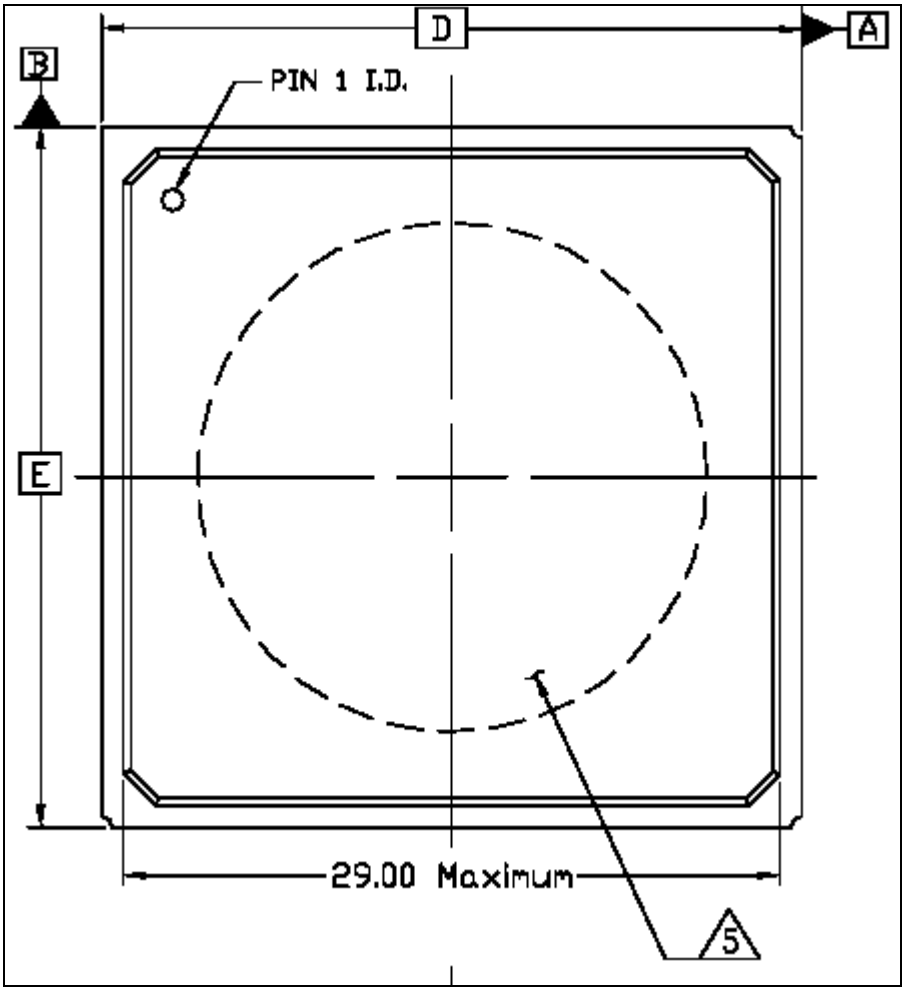


Figure 4 - Package Pin 1 Location

Performance

Speed and Bit Depth

The KSC-3000 is designed to process input pixels represented by 10 bit values. It outputs pixel triplets of red, green, and blue values. Each of the red, green, and blue values is represented by 8 bits. The KSC-3000 is designed to work at continuous pixel rates of up to 40 MHz.

Power

Here is a link to information on the thermal characteristics of Xilinx packages.
http://www.xilinx.com/products/virtex/handbook/ug002_ch4_therm.pdf

Static power for the KSC-3000 is calculated to be 200 mW, dynamic power of 425 mW, and total power of 625mW.

Operation

The KSC-3000 produces signals on its output that are compatible with the National Instruments 1424 frame grabber. For more information refer to the National Instruments documentation describing this interface. The valid signals frame the data in a manner which guarantees that the inter-line and inter-frame minimum times will be met. This results from the KSC-3000 internally accumulating data until complete lines are available and producing them in

bursts. The functioning of the algorithms guarantee that minimum inter-frame delays will be met, but registers are available to program the output delays to greater than the minimums subject to the constraints of meeting the input data rate.

The information in **Table 3** and Error! Reference source not found. was obtained from the document referenced by this link. http://www.xilinx.com/partinfo/ds031-3.pdf (Check this site for current values.)

Maximum Ratings

Absolute Maximum Ratings

Symbol	Description	Rating	Units
V_{CCINT}	Internal supply voltage relative to ground	-0.5 to 1.65	V
V_{CCAUX}	Auxiliary supply voltage relative to ground	-0.5 to 4.0	V
V_{CCO}	Output drivers supply voltage relative to ground	-0.5 to 4.0	V
V_{BATT}	Key memory battery backup supply	-0.5 to 4.0	V
V_{REF}	Input reference voltage	-0.5 to V_{CCO}+0.5	V
V_{IN}	Input voltage relative to GND (user and dedicated I/Os)	-0.5 to V_{CCO}+0.5	V
V_{TS}	Voltage applied to 3-state output (user and dedicated I/Os)	-0.5 to 4.0	V
T_{STG}	Storage temperature (ambient)	-65 to +150	°C
T_{SOL}	Maximum soldering temperature	+220	°C
T_J	Operating junction temperature	+125	°C

Notes:

1. Stresses beyond those listed under Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under is not implied. Exposure to Absolute Maximum Ratings for extended periods of time might affect device reliability.
2. For soldering guidelines and thermal considerations see *Device Packaging* information on the Xilinx website.

Table 3- Xilinx Virtex II Maximum Ratings

DC Operating Conditions

Symbol	Description		Min	Max	Units
V_{CCINT}	Internal supply voltage relative to GND T_j = 0°C to +85°C	Commercial	1.425	1.575	V
	Internal supply voltage relative to GND T_j =-40°C to +85°C	Industrial	1.425	1.575	V
V_{CCAUX}	Auxiliary supply voltage relative to GND T_j = 0°C to +85°C	Commercial	3.135	3.465	V
	Auxiliary supply voltage relative to GND T_j = -40°C to +85°C	Industrial	3.135	3.465	V
V_{CCO}	Supply voltage relative to GND T_j = 0°C to +85°C	Commercial	1.2	3.6	V
	Supply voltage relative to GND T_j = -40°C to +85°C	Industrial	1.2	3.6	V
V_{BATT}	Battery supply relative to GND T_j = 0°C to +85°C	Commercial	1.0	3.6	V
	Battery supply relative to GND T_j = -40°C to +85°C	Industrial	1.0	3.6	V

Notes:

1. If a battery is not used, do not connect V_{BATT}.
2. Recommended maximum voltage droop for V_{CCAUX} ia 10mV/ms.
3. The thresholds for Power On Reset are V_{CCINT} > 1.2V, V_{CCAUX} > 2.5V, and V_{CCO} (Bank 4) > 1.5V.
4. Limit the noise at the power supply to be within 200mV peak-to-peak.
5. For power bypassing guidelines, see XAPP623 at the Xilinx website.

Table 4 - Virtex II Operating Conditions

AC Operating Conditions

The following tables list setup and hold times as well as the clock to output times for the data clock and the serial interface clock. These numbers are not typical values, they are the actual values produced by doing a timing analysis of the KSC-3000 design.

Setup/Hold to clock ClockIn (ns)

	Setup to	Hold to
Source Pad	clk (edge)	clk (edge)
FrameValidIn	1.144(R)	0.065(R)
LineValidIn	1.249(R)	-0.040(R)
PixelIn(0)	1.163(R)	0.046(R)
PixelIn(1)	1.166(R)	0.043(R)
PixelIn(2)	1.163(R)	0.046(R)
PixelIn(3)	1.155(R)	0.054(R)
PixelIn(4)	1.155(R)	0.054(R)
PixelIn(5)	1.146(R)	0.063(R)

PixelIn(6)	1.147(R)	0.062(R)
PixelIn(7)	1.147(R)	0.062(R)
PixelIn(8)	1.149(R)	0.060(R)
PixelIn(9)	1.144(R)	0.065(R)

Table 4 - Data Clock Setup and Hold Times

Setup/Hold to clock SerClock (ns)		
	Setup to	Hold to
Source Pad	clk (edge)	clk (edge)
SerData	14.422(R)	0.052(R)
SerData	18.255(F)	-2.609(F)

Table 5 - Serial Interface Setup and Hold Times

Clock ClockIn to Pad (ns)	
	clk (edge)
Destination Pad	to PAD
BPixelOut(0)	5.925(R)
BPixelOut(1)	5.936(R)
BPixelOut(2)	5.921(R)
BPixelOut(3)	5.936(R)
BPixelOut(4)	5.942(R)
BPixelOut(5)	5.940(R)
BPixelOut(6)	5.942(R)
BPixelOut(7)	5.937(R)
ClockOut	6.742(X)
FrameValidOut	5.929(R)
GPixelOut(0)	5.935(R)
GPixelOut(1)	5.934(R)
GPixelOut(2)	5.931(R)
GPixelOut(3)	5.937(R)
GPixelOut(4)	5.925(R)
GPixelOut(5)	5.937(R)
GPixelOut(6)	5.931(R)

GPixelOut(7)	5.937(R)
LedGrnSink_n(2)	12.541(R)
LedGrnSink_n(3)	12.551(R)
LineValidOut	5.929(R)
PixelValidOut	5.935(R)
RPixelOut(0)	5.931(R)
RPixelOut(1)	5.918(R)
RPixelOut(2)	5.935(R)
RPixelOut(3)	5.934(R)
RPixelOut(4)	5.918(R)
RPixelOut(5)	5.936(R)
RPixelOut(6)	5.931(R)
RPixelOut(7)	5.936(R)

Table 6 - Data Clock to Data Out Times

Clock SerClock to Pad (ns)	
	clk (edge)
Destination Pad	to PAD
LedGrnSink_n(1)	11.775(R)
LedRedSink_n(0)	10.524(R)
LedRedSink_n(1)	10.991(R)
LedRedSink_n(2)	11.650(R)
LedRedSink_n(3)	11.760(R)
SerData	8.072(F)
TestClockOut	11.245(X)

Table 7 - Serial Interface Clock to Data Out Times

Input Clock Requirements

The input data clock, ClockIn, should be a free running signal with a maximum frequency of 40 MHz. It should have a 50% duty cycle (± 10%). It is suggested that the device providing data to the KSC-3000 produce data on the rising edge of the clock but then provide an inverted clock to the KSC-3000 ClockIn pin. This provides large timing margins for setup and hold times, provided the clock and data signals are produced at the same time and location with similar path lengths to minimize skew. A similar method is used at the red, green, and blue data outputs of the KSC-3000. The data at the outputs is changed on the rising edge of ClockIn but the output clock, ClockOut, is an inverted version of this clock to provide increased timing margins at the receiving device and to account for signal skew.

Input and Output Timing

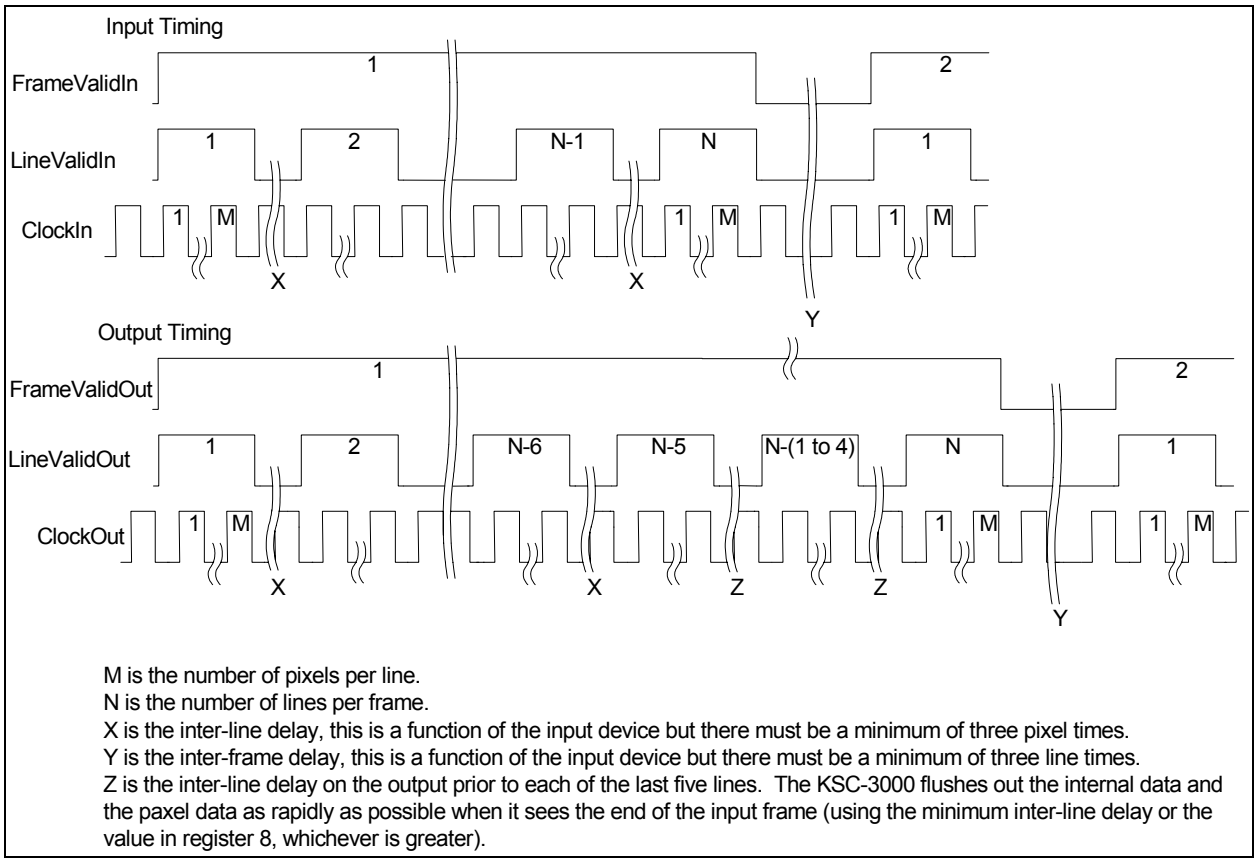


Figure 5 – Input and Output Timing

Reference Design

For schematics showing a reference design for a board that uses the KSC-3000 please contact Kodak Image Sensor Solutions.

Memory Map

Table 8 contains the memory map for the KSC-3000 device. The table shows the address used to access the various locations when the KSC-3000 is selected. It also shows the information necessary to write to the device to control it, or interpret the data that is read back. Note that in the access type column some locations are marked Read/Reset. This indicates that the location may be read to determine it's current contents, but that a correctly formatted write of any data to this location will cause the contents to revert to the reset value.

KSC-3000 Memory Map

Address	Width	Access Type	Function	Bit(s)	Defintion	Enumeration	Reset Value	Comments
000	1	Read/Write	Serial I/F Control	0	LedGrnSink_N(1)	1 = enable	0	
001	44	Read/Write	TIG Control	0	Enable TIG	1 = enable	0	
				3:1	Reserved		000	
				5:4	Image gen mode	00 = LFSR	00	

						01 = Pixel Ramp 10 = Line Ramp 11 = Frame Ramp		
				7:6	Num frames mode	00 = One frame 01 = 10 frames 10 = 1000 frames 11 = cont. frames	00	
				18:8	Blanks b/w pixels	unsigned	0	measured in pixels
				19	Reserved		0	
				30:20	Blanks b/w lines	unsigned	0	measured in pixels min. 3 blanking pixels will be inserted
				31	Reserved		0	
				42:32	Blanks b/w frames	unsigned	0	measured in lines min. 3 blanking lines will be inserted
				43	Reserved		0	
002	1	Read/Write	SIG Control	0	Reset signature	0 = run 1 = reset	0	
003	1	Read/Write	Defect Correct Control	0	Reserved		0	
004	48	Read/Write	Paxelizer Control	11:0	Pixels per paxel	unsigned	0	if pixels per paxel or
				23:12	Lines per paxel	unsigned	0	lines per paxel are set
				35:24	First sample pixel	unsigned	0	to 0, paxel data is
				47:36	First sample line	unsigned	0	replaced with 0s
005	1	Read/Write	White Balance Control	0	Reserved		0	
006	8	Read/Write	Haneda Control	7:0	SKEdge parameter	unsigned	32 (20h)	Note that sThrC is 64.
007	1	Read/Write	Color Correct Control	0	Reserved		0	
008	12	Read/Write	Output FIFO Control	10:0	Minimum blanks b/w lines	unsigned	0	measured in pixels min. 3 blanking pixels will be inserted
				11	Reserved		0	
009	38	Read/Write	Image Info	10:0	Pixels per line	unsigned	1000 (3E8h)	
				11	Reserved		0	
				22:12	Lines per frame	unsigned	1000 (3E8h)	
				23	Reserved		0	
				33:24	Dark Offset	unsigned	0	
				35:34	Reserved		00	
				36	CFA start pixel	1 = odd	0	
				37	CFA start line	1 = odd	0	
00A	48	Read/Write	Color Correct Red Coefficients	12:0	Coeff A	signed	1717 (06B5h)	
				15:13	Reserved		000	
				28:16	Coeff B	signed	-458 (1E36h)	

				31 :29	Reserved		000	
				44:32	Coeff C	signed	-235 (1F15h)	
				47:45	Reserved		000	
00B	48	Read/Write	Color Correct Green Coefficients	12:0	Coeff A	signed	-77 (1FB3h)	
				15:13	Reserved		000	
				28:16	Coeff B	signed	1267 (04F3h)	
				31 :29	Reserved		000	
				44:32	Coeff C	signed	-166 (1F5Ah)	
				47:45	Reserved		000	
00C	48	Read/Write	Color Correct Blue Coefficients	12:0	Coeff A	signed	92 (005Ch)	
				15:13	Reserved		000	
				28:16	Coeff B	signed	-473 (1E27h)	
				31 :29	Reserved		000	
				44:32	Coeff C	signed	1405 (057D)	
				47:45	Reserved		000	
00D	36	Read/Write	White Balance Coefficients	11:0	Red coeff	unsigned	1024 (400h)	
				23:12	Green coeff	unsigned	1024 (400h)	
				35:24	Blue coeff	unsigned	1024 (400h)	
020	7	Read/Reset	Serial I/F Status	0	State Machine Err	1 = error	0	
				1	Addresing Err	1 = error	0	
				2	Write Size Err	1 = error	0	
				3	Read Size Err	1 = error	0	
				4	Invalid Write Err	1 = error	0	
				5	Invalid Read Err	1 = error	0	
				6	General Err	1 = error	0	
021	1	Read/Reset	TIG Status	0	Image gen complete	1 = complete	0	
022	2	Read/Reset	SIG Status	0	Sig0 Match	1 = match	0	
				1	Sig1 Match	1 = match		
023	1	Read/Reset	Defect Correct Status	0	Reserved		0	
024	1	Read/Reset	Paxelizer Status	0	Reserved		0	
025	1	Read/Reset	White Balance Status	0	Reserved		0	
026	1	Read/Reset	Haneda Status	0	Reserved		0	
027	1	Read/Reset	Color Correct Status	0	Reserved		0	
028	2	Read/Reset	Output FIFO Status	0	FIFO overflow	1 = overflow	0	
				1	FIFO underflow	1 = undeflow	0	
040	16	Read Only	ID Register	15:0	Device/program ID	unsigned	4120 (1018h)	fixed value
041	24	Read Only	SIG Result	23:0	Result value	unsigned	1	
060 - 069	24	Read/Write	Defect Location	10:0	Pixel location (col.)	unsigned	0	Defects in first/last two cols are ignored

				11	Reserved		0	
				22:12	Line location (row)	unsigned	0	Defects in first/last row are ignored
				23	Reserved		0	*Reset values imply no defect correction*
100 - 4FF	8	Read/Write	Red Gamma LUT	7:0	Red pixel value	unsigned	CCIR709	
500 - 8FF	8	Read/Write	Green Gamma LUT	7:0	Green pixel value	unsigned	CCIR709	
900 - CFF	8	Read/Write	Blue Gamma LUT	7:0	Blue pixel value	unsigned	CCIR709	

Table 8 – KSC-3000 Memory Map

Serial I/F Control (Register 000)

Default: 0

This register contains a test bit that is used to turn on/off the DS4 LED.

TIG Control (Register 001)

Default: 0

This register controls the behavior of the test image generator (TIG). The TIG is an internal pattern generator that emulates an incoming image stream so that the internal operation of the device can be tested without being connected to an input device. The TIG is intended as a debug tool only. Note that the pixel clock input must still be operational in order to generate a TIG image.

The TIG is capable of producing four different pattern types according to the setting of the image generation mode bits. The LFSR is a pseudo-random pattern, the pixel ramp increments each new output pixel by one, the line ramp increments the output pixel by one for each new line that is generated, and the frame ramp increments the output pixel by one for each new frame that is generated. Note that when viewed on an output device, the LFSR pattern will look like dynamic static, the pixel and line ramps will create rolling images, and the frame ramp will produce a fade to black effect.

Also, the number of sequential frames to be generated by the TIG is specified by setting the num frames mode bits. Options available are one frame, ten frames, 1000 frames or a continuous stream of frames until the TIG is disabled.

Additionally, the blanking interval between lines and the blanking interval between frames can also be adjusted on the output of the TIG to more closely emulate the timing of a specific input device. The pixel blanking interval was not implemented and should be left at its reset value. The TIG line blanking interval should never be set lower than the line blanking interval specified in the Gamma LUT control register when the TIG is enabled.

The TIG may be used in conjunction with the signature analyzer to perform a built in self test (BIST) on the device to verify its internal functionality.

SIG Control (Register 002)

Default: 0

This register contains only one control bit that is used to reset the signature generated by the signature analyzer to "0x000001". The control bit must be asserted and deasserted while the FrameValid input is inactive and the TIG is not enabled in order to guarantee a clean reset.

Interpolation (Register 006)

Default: 32

The color interpolation stage uses a patented adaptive cubic spline interpolation algorithm. The algorithm computes a smoothing spline and a sharpening spline, and uses them to adaptively preserve edges and suppress noise. Increasing the value of the Edge parameter will increase the weighting of the sharpening spline over the smoothing spline. A large value will cause aggressive edge enhancement. A small value will cause aggressive smoothing. The default value of 32 produces an image with a good balance of sharpening and smoothing.

The interpolator uses a 4x4 kernel, which results in the output image having three fewer lines than the input image.

Output FIFO Control (Register 008)

Default: 0

This register specifies the minimum line blanking interval (LBI) between lines on the output of the device. The following paragraph is a contextual description that explains the purpose of this register value.

The C1 design contains an output FIFO to collect pixels so that a line transfer does not begin on the output until a full line is available. Therefore, the LBI on the output is generally constrained by the LBI on the input. However, once a full image has been received at the input, the portion of the image that remains in the pipeline of the C1 FPGA must be flushed out in order to complete the image on the output. At this point, the LBI on the output is no longer being constrained by the LBI on the input and, therefore, the output LBI is controlled by the output FIFO control register. Since the pipeline stores two image lines in addition to the paxel data that is output in the last three lines, there are a total of five lines* at the end of the image that will be output with the minimum LBI specified in the output FIFO control register.

This minimum LBI value should be set the same as or lower than LBI on the input of the device during normal operation, or the LBI specified in the TIG control register when the TIG is enabled. Otherwise, an overflow and/or underflow condition may occur in the output FIFO.

* It is assumed that the FrameValid and LineValid inputs will deassert simultaneously at the end of each frame. If this is not the case, the delay between the deassertion of LineValid and FrameValid will be added to the LBI preceding the fifth last line on the output. This is due to the fact that the end of frame must be fully qualified by the deassertion of both LineValid and FrameValid before flushing of the internal pipeline can begin.

Dark Offset Correction (Register 009)

Default: 0

Setting the dark offset register to values other than 0 will cause the value each pixel in the image to be reduced by the value of the register setting, up to a maximum of 255.

Color Correction (Registers 00A – 00C)

Default:

$$\begin{bmatrix} 1717 & -458 & -235 \\ -77 & 1267 & -166 \\ 92 & -473 & 1405 \end{bmatrix}$$

The color correction stage applies a 3x3 color correction matrix to the image data. The appropriate matrix will convert the raw image data to a color space compatible with the display device used.

The default matrix yields optimal color reproduction for a Kodak KAI-1020CM pigment CFA imager with an IR cut filter, and an sRGB-compatible display device. The register values are floating point matrix coefficients, scaled by 1024 to produce a 12-bit integer equivalent.

White Balance (Register 00D)

Default: 1024|1024|1024

Setting the digital white balance gain registers to values other than 1024 will change the overall level of the corresponding color channel. The gain multiplier is calculated as:

$$\text{GAIN} = \text{Register Setting} / 1024$$

A register setting of 1536 will multiply every pixel in the color channel by 1536/1024, or 1.5.

The gains should be normalized so that the smallest value is 1024 (1.0) to preserve maximum dynamic range. However, if the maximum gain setting of 4095 (4.0) is insufficient, the smallest gain setting may be reduced below the nominal setting.

Serial I/F Status (Register 020)

Default: 0

This register indicates errors detected by the serial interface logic. A state machine error is an internal error. An addressing error indicates that SerLoad was deasserted while sending address data. A write size error indicates that too much or too little data was provided for a given register during a write. A read size error indicates that too much or too little data was clocked out from a given register during a read. An invalid write error indicates that a register address was provided during a write cycle that is either read-only or non-existent. An invalid read error indicates that a register address was provided during a read cycle that is non-existent. A general error is asserted when any serial i/f error is detected.

All “status” registers latch any detected errors/conditions and must be explicitly cleared by writing an arbitrary value (of the correct length) to their address.

TIG Status (Register 021)

Default: 0

This register contains one bit that indicates whether the TIG has completed generating the specified number of frames once it has been enabled.

Output FIFO Status (Register 028)

Default: 0

This register indicates errors that occur due to overflow or underflow conditions within the output FIFO. Once this type of error is detected during a frame, the remainder of the frame is discarded. The most likely cause of this type of error is an incorrect setting in the output FIFO control and/or TIG control registers.

ID Register (Register 040)

Default: 4120 (1018h)

This register contains an identification string that describes the version of the FPGA bit file.

SIG Result (Register 041)

Default: 1

This register indicates the current signature contained in the signature analyzer. This register is read-only, and the signature can only be reset using the SIG control register.

Defect Correction (Registers 060 – 069)

Default: None

A valid entry in the defect map will cause the pixel value at the referenced location to be replaced by the average value of its nearest neighbors. For a green pixel, a 4-way average is used. For a red or blue pixel, a two-way average is used.

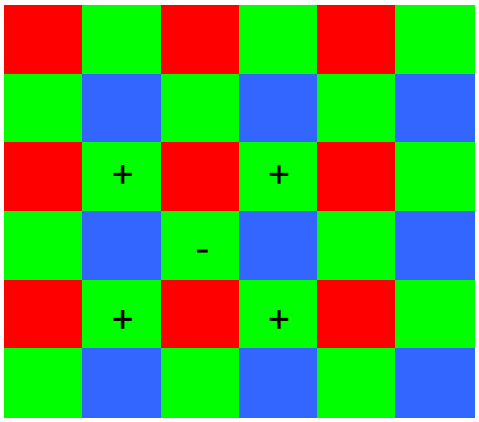


Figure 5 - Defective Green Pixel

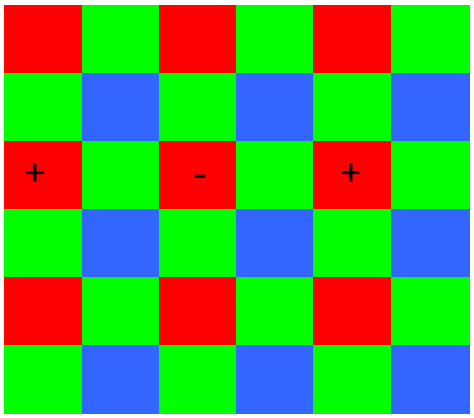


Figure 5 - Defective Red or Blue Pixel

Invalid entries in the defect map are ignored. An entry is invalid if it appears in the first or last row of the image, or in the first or last two columns of the image.

Image Information

The pixels per line and lines per frame value should be programmed to indicate the actual number of pixels the KSC-3000 will be receiving*. Pixels per line are the number of elements within each line valid, and pixels per frame are the number of elements within each frame valid.

The color filter array (CFA) start pixel and start line bits are intended to be set according to the staring point of the Bayer pattern generated by the CFA. By default, it is assumed that the first pixel received will be a green pixel on a row with green and red pixels.

* If the user wants to generate paxel data the pixels per line should not be set to less than 576 or there will not be enough clocks cycles during the last three lines to append all of the paxel data to the image data. 24X36 paxels = 864, times 4 data elements per paxel = 3456, divided by 2 paxel elements produced per clock cycle = 1728, divided by 3 line times = 576.

Serial Communications

The serial interface is a three-wire bi-directional communication channel. It consists of a clock signal (SCK or SerClock), a bi-directional data signal (SDATA or SerData), and a load signal (SL or SerLoad) that operates as a chip select to enable communications on the channel. The serial interface provides access to KCS-3000 internal registers and memory locations. Please refer to Table 8 – KSC-3000 Memory Map for a description of the accessible registers/memories.

The serial interface supports read and write cycles as shown in Figure 6 and Figure 7. All data provided to the KCS-3000 on SerData are qualified by the rising edge of SerClock and the assertion of SerLoad. The SerLoad signal is used to frame a read/write cycle. In a read cycle, the data is driven onto SerData on the falling edge of the clock. The number of SerClock pulses provided to read/write the data before SerLoad is deasserted must exactly match the register/memory width that is being accessed.

The interface also supports burst mode transactions (not shown) such that the address is only specified for the first location to be read/written and subsequent address values are calculated internally by the KCS-3000. This is accomplished by extending the SerLoad signal at the end of a single read/write transaction and providing the correct number of SerClock pulses to clock out/in the read/write data for the next sequential address location. The format of a single read/write cycle is merely a burst mode cycle that provides enough data for only the first address location. Note that burst mode transactions are not possible across non-contiguous addresses.

The serial interface also includes some error detection logic. These errors are latched into the serial interface status register and will remain persistent until the serial interface status register is explicitly cleared via a write cycle. Since certain error conditions may result in the serial interface being unable to provide read access to the status register, some of these status bits are routed to LEDs on the reference design. Please refer to Table 2 - Diagonstic Connections for these details.

Parameter	Description	Min	Typ	Max	Units
f_sck	Maximum SCK Frequency			14	MHz
t_ls	SL to SCK Setup Time	10			ns
t_lh	SCK to SL Hold Time	10			ns
t_ds	SDATA Valid to SCK Rising Edge Setup Time	10			ns
t_dh	SCK Rising Edge to SDATA Valid Hold Time	10			ns
t_dv	SCK Falling Edge to SDATA Valid Read	10			ns

Table 9 - Serial I/F Timing Parameters

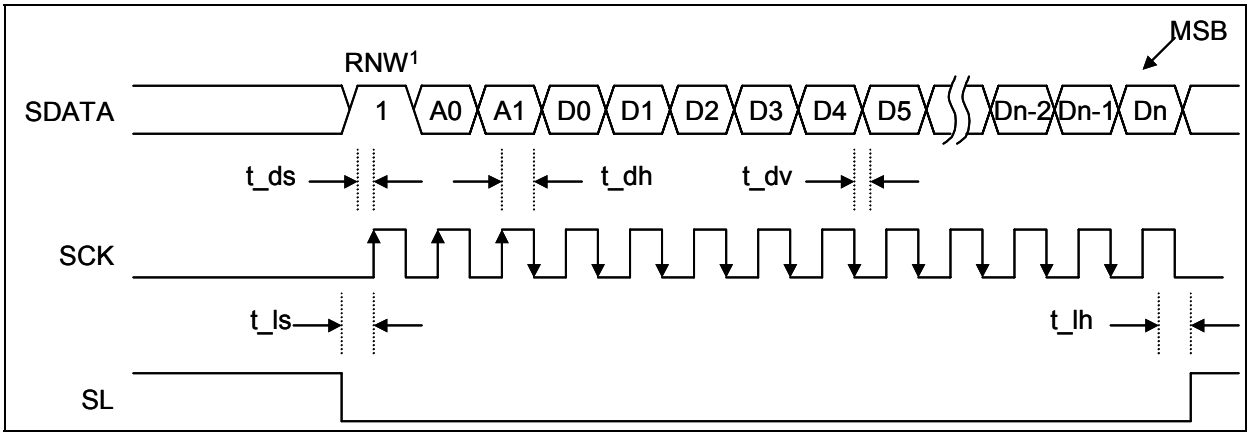


Figure 6 Serial interface read timing

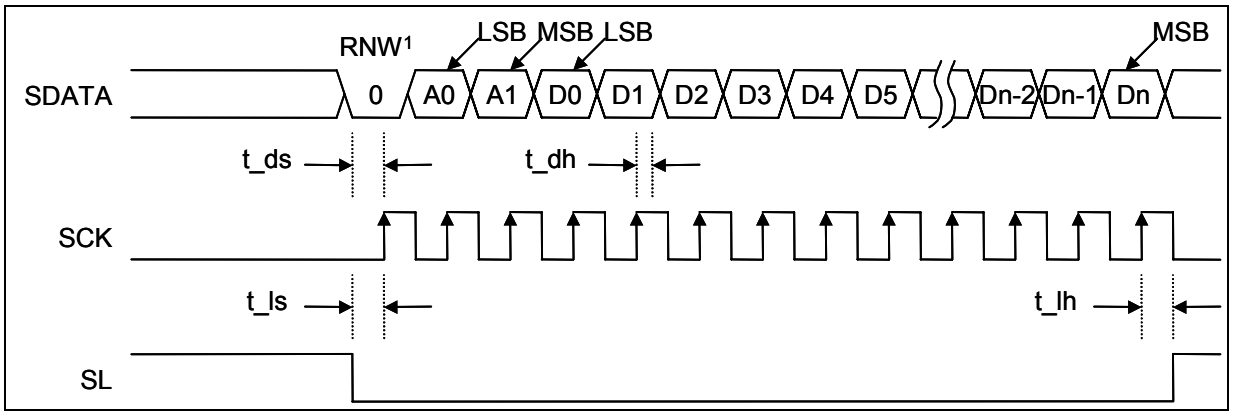


Figure 7 - Serial interface write timing

Storage and Handling

Storage Conditions

Information on package moisture sensitivity can be found at the following link.

http://www.xilinx.com/publications/products/packaging/moisture.htm

A few of the relevant sections from the Xilinx documentation are reproduced here.

Handling Parts in Sealed Bags:

Storage: The sealed bag should be stored, unopened, in an environment of not more than 90% RH and 40°C. Nothing in part appearance can verify moisture levels.

Other Conditions: Open the bag when parts are to be used. After opening, strictly adhere to factory floor life conditions to ensure that devices are maintained below critical moisture levels. Note that factory floor life is cumulative. Any period of time when MBB is opened must be added to all other opened periods.

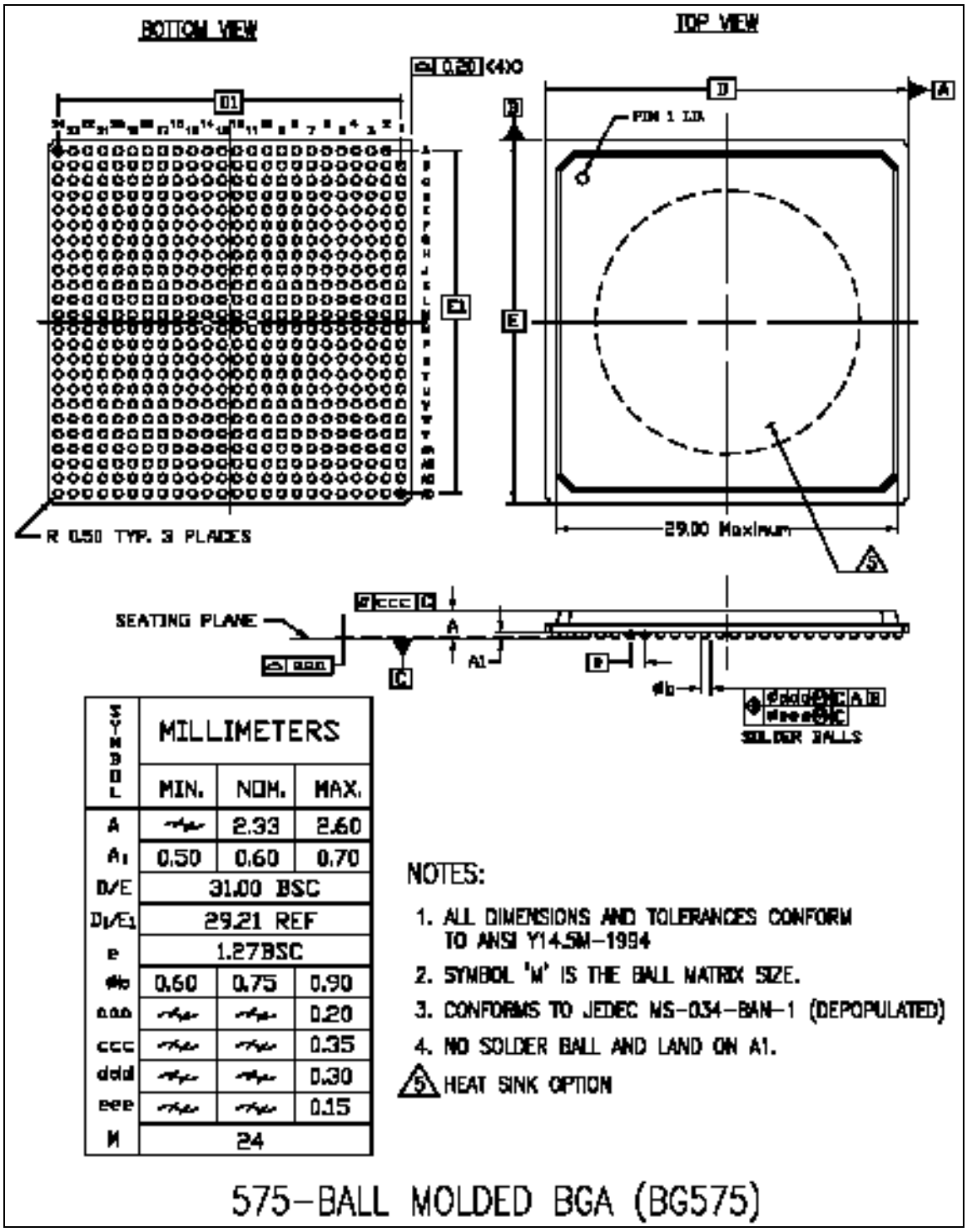
Information on electrostatic and latch-up information can be found at the following link.

http://www.xilinx.com/products/qa_data/relreprt.pdf

The XC2V class devices are rated at a latch-up of ±200 mA, human body model of ±1500V to ±2000V, and a charge device model of ±500V.

Mechanical Drawings

Package Drawing



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A		2.33	2.60
A1	0.50	0.60	0.70
D/E	31.00 BSC		
D1/E1	29.21 REF		
e	1.27BSC		
ϕb	0.60	0.75	0.90
aaa			0.20
ccc			0.35
ddd			0.30
eee			0.15
M	24		

Figure 8 - Package Drawing

Ordering Information

Address all inquiries and purchase orders to:

Image Sensor Solutions
Eastman Kodak Company
Rochester, New York 14650-2010
Phone: (585) 722-4385
Fax: (585) 477-4947
E-mail: imagers@kodak.com

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WARNING: LIFE SUPPORT APPLICATIONS POLICY

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury or property or other consequential damages.