Kodak

DEVICE
PERFORMANCE
SPECIFICATION

KODAK KSC-1000 Timing Generator

July 12, 2003
Revision 1.0

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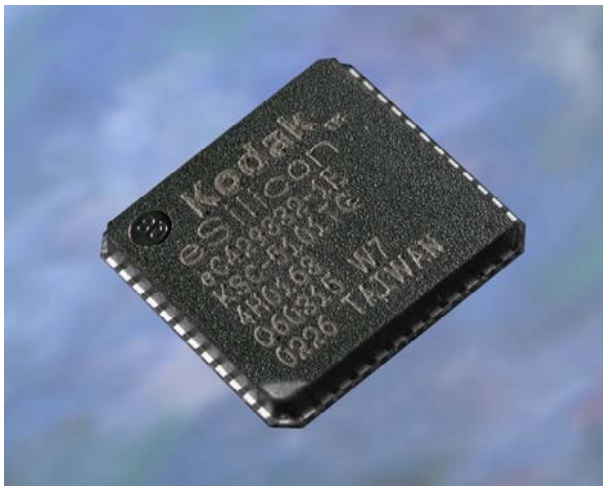
KODAK KSC-1000 Timing Generator



Description

The Kodak KSC-1000 Timing Generator simplifies camera design by providing all of the timing signals necessary to operate the entire family of Kodak area array image sensors (Full Frame and Interline CCDs) and associated analog front-end (AFE) circuits. Full programability through a simple 3-wire serial interface allows maximum flexibility in sensor operation. Frame tables and line tables, in conjunction with control registers, permit the customization of the timing outputs to meet application-specific requirements. Multiple outputs, binning, electronic shuttering, and fast line dump are fully supported. The use of a Delay Locked Loop (DLL) circuit provides for precise control and sub-pixel positioning of timing signals, and stability over variations in voltage and temperature.

KSC-1000 Rev. 1.0
July 12, 2003

Parameter	Value
Maximum Image Size	8192 (H) x 8192 (V)
Pixel Rate	4.13MHz to 60 MHz
Integration Time	1 pixel clock to infinity
Packaging	8 mm x 8 mm, 56-pin MLF
Power Dissipation	265mW @40MHz, 12mA Pixel Rate Clock Output Drive Level
Power Supply Voltage	1.8 and 3.3 V
Input Clock	2x pixel clock
Input Clock Requirements	8.26 MHz to 10 MHz Clock Oscillator 10 MHz to 60 MHz Crystal Oscillator or Clock Oscillator 60 MHz to 120 MHz Clock Oscillator
Vertical Binning	no limit
Horizontal Binning	x4 max
V pulse min	1 pixel clock
V pulse max	8192 pixel clocks
Independent HCLK control	Duty cycle: 25% to 75% Offset: 1/64 pixel period
Independent reset gate (RG) and AFE signal control	Width: to 50% Offfset: 1/64 pixel period
Pixel Rate Clock Output Drive Levels	12mA or 24mA
Asynchronous triggered capture	supported
Operating Temperature	-20°C to +70°C

DEVICE DESCRIPTION

Architecture

Overall

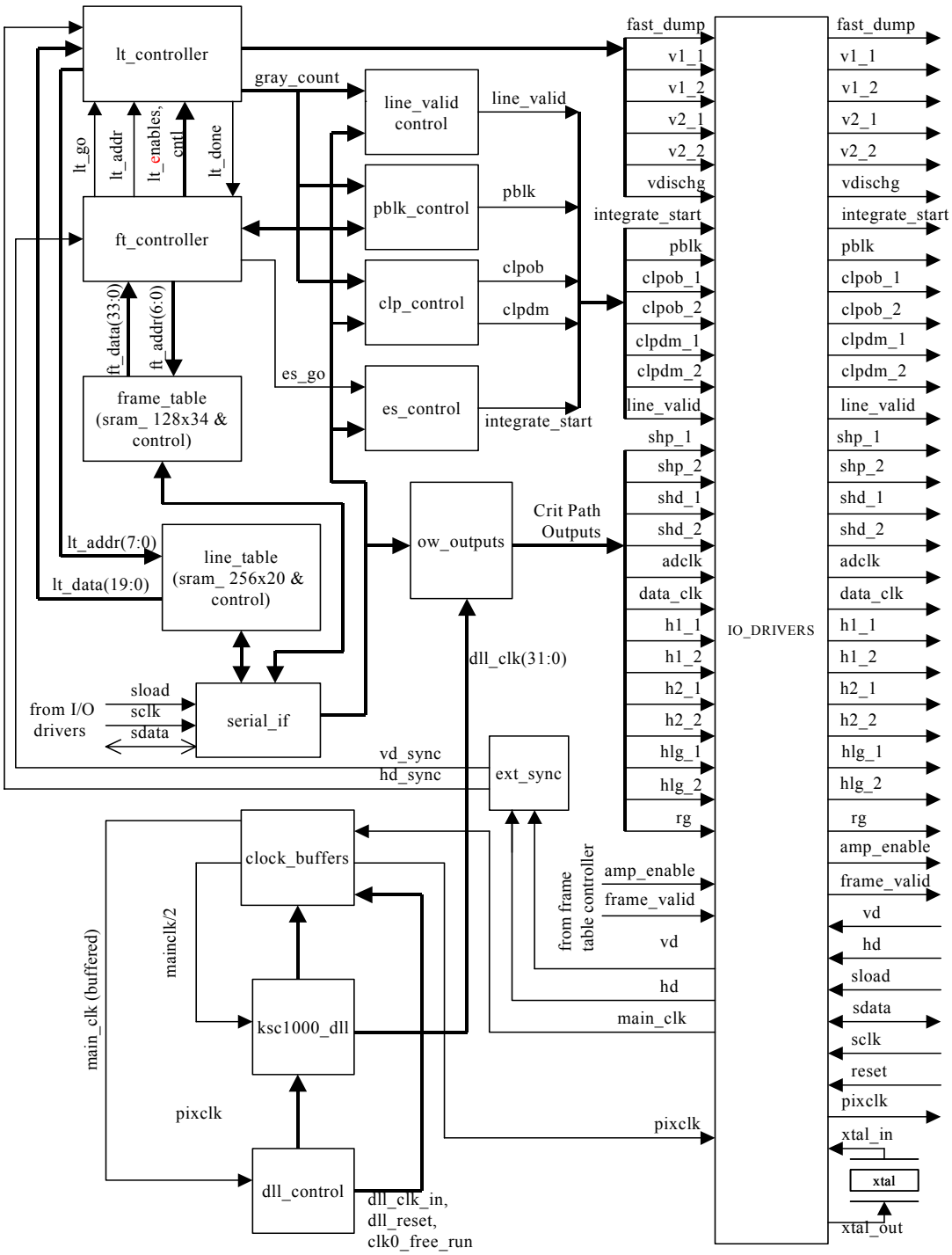


Figure 1 KSC 1000 Block Diagram

The KSC-1000 provides all of the signals necessary for an imaging system using Kodak Full Frame (KAF) or Interline (KAI) family of image sensors. It also provides the signals necessary for operation of 2 analog front-end (AFE) chips, enabling independent optimization of the AFE chips for dual channel readout devices.

The KSC-1000 utilizes a Delay Locked Loop (DLL) to maintain precise control of the pixel clock rate signals over process, temperature and voltage variations. There are 8 independent DLLs, with only one being switched on at any given time. The DLLs operate from 4.13MHz to 60MHz. The output frequency of the DLL is ½ the input oscillator frequency. The output of the DLL provides 64 positions within the pixel clock period for precise control of the positioning of the pixel rate clock signals.

The KSC-1000 has 8 control registers, along with 2 blocks of Static Random Access Memory (SRAM) configured as Frame Tables and Line Tables. The fast dump gate signal and vertical clocks are defined in the line tables in terms of number of pixel clocks. This architecture provides complete flexibility in positioning these signals relative to one another. For example, 3 line tables could be used to define a flush, integrate and readout sequence. There are 16 line tables available. Line Table sequencing is controlled by Frame Tables.

In conjunction with the control registers, frame tables are used to control AFE clamping and blanking pulses, horizontal binning, frame and line valid signals, AFE clocks, a CCD video amplifier power supply switch and integration control. Sequencing between frame table entries or between frame tables can occur either by a programmed counts, or can be synchronized by an external controller.

The KSC-1000 supports imager array sizes up to 8192 pixels by 8192 pixels. Gray coding is used on the internal horizontal pixel counter to minimize the risk of digital noise coupling into the analog signal processing. A 3 wire serial interface is used to program the device. Binary to Gray code conversion is performed internally where needed to allow programming using standard binary counts.

Sequence of Operations

The KSC-1000 must be programmed via the serial interface prior to operation. A sequence of operations is initiated by placing the device in execution mode and full power mode in the General Control register. Execution will start at the first entry of the frame table indicated in the frame table pointer register.

Each frame table entry will either execute a line table sequence or perform a jump instruction.

Figure 2 is a flow diagram of the sequence of operation. Normally a line table will be called by the first entry of the frame table. After the line table sequence is executed, a test is performed to see if the INTG_STRT signal needs to be asserted. This could occur if the Force INTG_STRT bit is set in the frame table entry, or if the line counter equals the value set in the INTG_STRT Line Register and the Check and Increment Line Counter bit is set in the frame table entry. If the test is positive, the INTG_STRT sequence is inserted immediately after completion of the line table.

Next, another test is performed to determine if the horizontal counter needs to be started. This would be the case for image readout. However for image sensor flush operations, the counter would not be started. Setting the hclk_h bit in the last valid line table entry forces the horizontal counter to start.

Finally a test is performed to determine if the frame table entry needs to be executed again. If this frame table entry has been executed the number of times indicated in the count field, operation continues with the next entry in the frame table. Otherwise this entry is executed again.

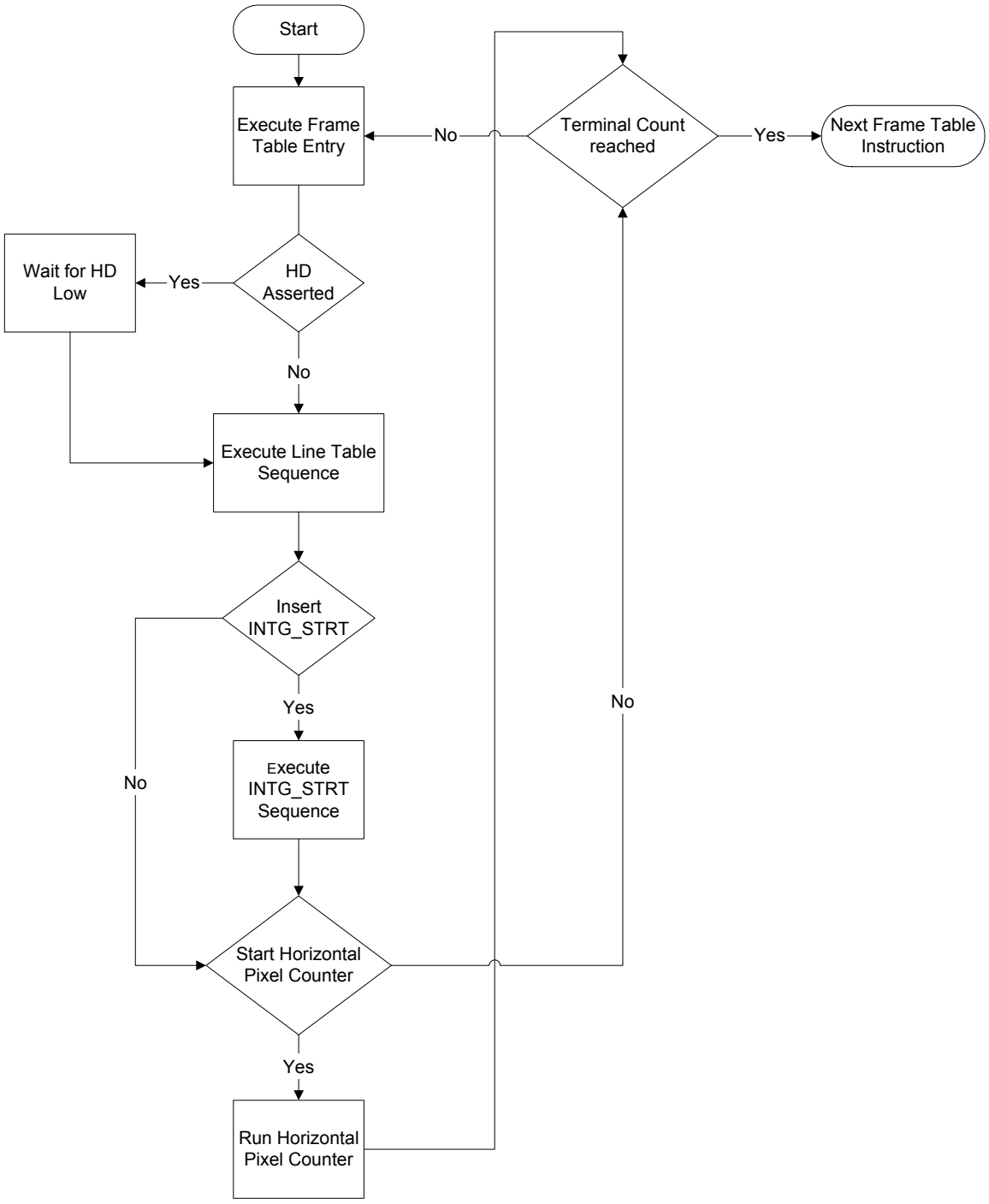


Figure 2 KSC-1000 Sequence Flow Diagram

Horizontal Line Synchronization

Horizontal line timing is controlled by the state of the HD signal. Asserting the HD signal high prior to reaching the terminal count of the horizontal pixel counter holds off the start of line table execution (start of the vertical interval counter). Line table execution will not begin until HD is driven low. This feature allows an external controller to synchronize horizontal line readout. Holding the HD signal low gives the KSC-1000 full control over horizontal line readout. HD functionality is illustrated in Figure 3.

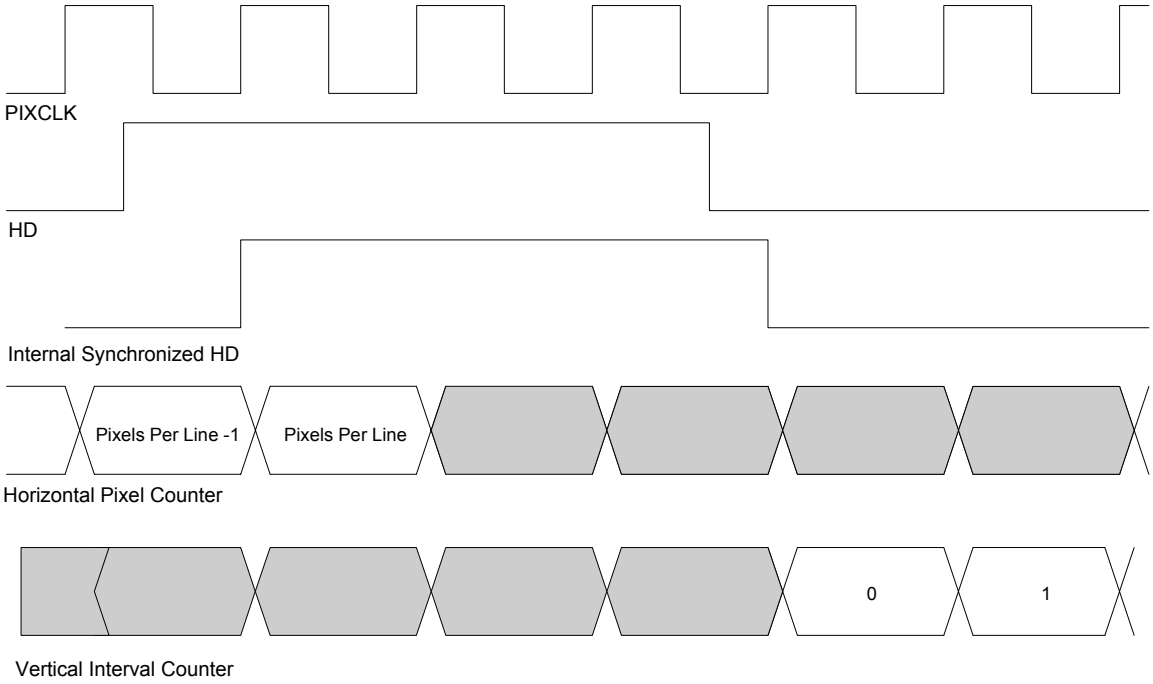


Figure 3 HD Functionality

Physical Description

Pin Description and Device Orientation

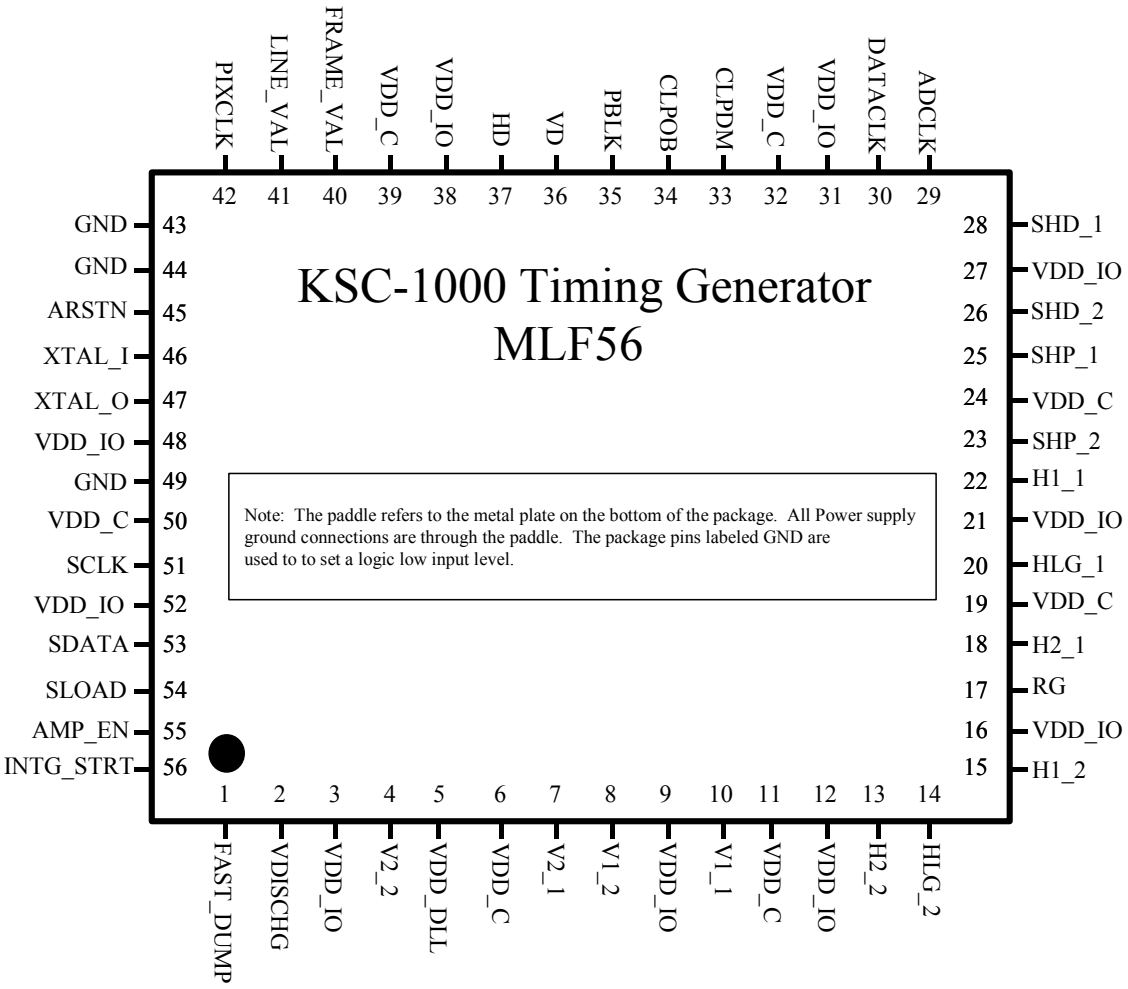


Figure 4 KSC-1000 Pin Diagram

Pin	Name	Description
1	FAST_DUMF	Fast Dump Gate Output
2	VDISCHG	Vertical Phase Discharge Switch Control Output
3	VDD_IO	3.3V I/O Power Supply
4	V2_2	Vertical Clock Phase 2 Output 2
5	VDD_DLL	1.8V DLL Power Supply
6	VDD_C	1.8V Core Logic Power Supply
7	V2_1	Vertical Clock Phase 2 Output 1
8	V1_2	Vertical Clock Phase 1 Output 2

9	VDD_IO	3.3V I/O Power Supply
10	V1_1	Vertical Clock Phase 1 Output 1
11	VDD_C	1.8V Core Logic Power Supply
12	VDD_IO	3.3V I/O Power Supply
13	H2_2	Horizontal Clock Phase 2 Output 2
14	HLG_2	Horizontal Last Gate Output 2
15	H1_2	Horizontal Clock Phase 1 Output 2
16	VDD_IO	3.3V I/O Power Supply
17	RG	Reset Gate Output Pulse
18	H2_1	Horizontal Clock Phase 2 Output 1
19	VDD_C	1.8V Core Logic Power Supply
20	HLG_1	Horizontal Last Gate Output 1
21	VDD_IO	3.3V I/O Power Supply
22	H1_1	Horizontal Clock Phase 1 Output 1
23	SHP_2	AFE 2 Reset Level Sampling Pulse
24	VDD_C	1.8V Core Logic Power Supply
25	SHP_1	AFE 1 Reset Level Sampling Pulse
26	SHD_2	AFE 2 Video Level Sampling Pulse
27	VDD_IO	3.3V I/O Power Supply
28	SHD_1	AFE 1 Video Level Sampling Pulse
29	ADCLK	A/D Clock
30	DATACLK	Data Latch Clock
31	VDD_IO	3.3V I/O Power Supply
32	VDD_C	1.8V Core Logic Power Supply
33	CLPDM	AFE Input Optical Black Level Clamp
34	CLPOB	AFE Post Analog to Digital Conversion Optical Black Level Clamp
35	PBLK	AFE Pre-Blanking Clock
36	VD	Vertical Sync (Frame Request) Input
37	HD	Horizontal Sync (Line Request) Input
38	VDD_IO	3.3V I/O Power Supply
39	VDD_C	1.8V Core Logic Power Supply
40	FRAME_VAL	Frame Valid (Vertical Sync) Output
41	LINE_VAL	Line Valid (Horizontal Sync) Output
42	PIXCLK	Pixel Clock Output
43	GND	Ground
44	GND	Ground
45	ARSTN	Asynchronous Reset Input

46	XTAL_I	Crystal Oscillator or Clock Oscillator Input (2X Pixel Clock)
47	XTAL_O	Crystal Oscillator Output (2X Pixel Clock)
48	VDD_IO	3.3V I/O Power Supply
49	GND	Ground
50	VDD_C	1.8V Core Logic Power Supply
51	SCLK	Serial Clock Input
52	VDD_IO	3.3V I/O Power Supply
53	SDATA	Serial Data I/O
54	SLOAD	Serial Load Input
55	AMP_EN	Video Amplifier Enable Control Output
56	INTG_STRT	Integration initiation pulse

Table 1 KSC-1000 Pin Descriptions

OPERATING CONDITIONS

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
IO Supply Voltage	VDD_IO	VSS – 0.3	4.6	V
Core Supply Voltage	VDD_C	VSS – 0.3	2.5	V
DLL Supply Voltage	VDD_DLL	VSS – 0.3	2.5	V
All Input Voltages	V_I	VSS – 0.3	VDD_IO + 0.3	V
Temperature Range Storage	T_{STG}	-55	+150	°C

Table 2 KSC-1000 Absolute Maximum Ratings

Long term exposure to absolute maximum ratings may affect device reliability and damage may occur if exposed to conditions exceeding the absolute maximums.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
IO Supply Voltage	VDD_IO	3.0	3.3	3.6	V
DLL Supply Voltage	VDD_DLL	1.7	1.8	1.9	V
Core Supply Voltage	VDD_CORE	1.7	1.8	1.9	V
Temperature Range Operating	T_{OPR}	-20		+70	°C

Table 3 KSC-1000 Recommended Operating Conditions

Decoupling, Grounding and Power-Up Requirements

Each of the power supply pins (VDD_C, VDD_IO, VDD_DLL) shall have at a minimum, local 0.1uF ceramic de-coupling capacitors. It is recommended that the IO_VDD_3P3V connections also have 10 uF de-coupling where possible to supply current during simultaneous switching of multiple outputs. Preferred configuration for the VDD_DLL is a 10uF tantalum, 0.1 uF ceramic, and 100 pF ceramic connected from the pin to ground, with a 10 ohm series resistance connecting the pin to the 1.8 V supply.

A single, common ground plane is recommended to reduce ground loops and local Eddy currents. The Micro Lead Frame (MLF) package of the KSC-1000 has a die attach 'paddle' on the PCB side of the package. This paddle is connected internally to the VSS nodes for VDD_C, VDD_IO, and VDD_DLL. It must be externally connected to the ground plane of the PCB during manufacturing.

To prevent latch-up, it is required that the higher voltage (3.3 V) supply be powered up first. To minimize the potential from power drain (crowbar effects) during power-up, the 1.8 V supply should follow the 3.3V supply relatively soon after. Since a linear regulator is required for the 1.8 V supply, it is recommended that the 1.8 V regulator be driven off of the 3.3 V regulated supply on board. In this manner, the above conditions should be obtained. The DLL supply (VDD_DLL) and the core supply (VDD_C) should be brought up together.

Alternately, a Schottky barrier diode can be applied between the 3.3V and 1.8V voltage supply pins to prevent race condition issues. In this implementation, the anode should be attached to the lower voltage supply (1.8 V) and the cathode to the higher voltage supply (3.3 V). In this case, if power is applied to the lower voltage first, the upper supply will track the lower less the threshold of the diode, thus preventing latch-up.

Electrostatic Discharge Protection

The KSC-1000TG contains protection circuitry that is rated class B using the machine model for Electrostatic Discharge (ESD) testing. Proper ESD precautions are recommended to avoid performance degradation or device failure.

Power Dissipation

Power dissipation is a function of the operating frequency, the number of outputs that are enabled, and the drive level of the pixel rate outputs. The table below lists current requirements of VDD_IO, VDD_C and VDD_DLL as a function of frequency and pixel rate output drive level.

Frequency (MHz)	VDD_DLL (mA Max)	VDD_C (mA Max)	Single CCD Output 12mA Drive (mA Max)	Single CCD Output 24mA Drive (mA Max)	Dual CCD Outputs 12mA Drive (mA Max)	Dual CCD Outputs 24mA Drive (mA Max)
4.13	0.25	4.9	24	27	31	50
5.94	0.32	5.8	25	28	33	52
8.53	0.37	7.1	26	29	36	55
13.82	0.42	9.1	29	35	42	61
17.55	0.53	10.8	32	39	45	66
26.04	0.66	14.2	37	47	55	76
31.88	0.80	16.9	41	52	61	85
42.22	0.98	21.4	49	60	74	98
60	1.40	30	64	80	97	128

Table 4 Power Supply Current Requirements

Conditions:

Values for VDD_IO at 3.3V, VDD_C and VDD_DLL at 1.8V

Outputs driving CMOS gate load.

Enabled Outputs for Single CCD Output Cases: H1_1, H2_1, HLG_1, RG, ADCLK, DATACLK, SHP_1, SHD_1, and PIXCLK along with all line and frame rate outputs

Enabled Outputs for Single CCD Output Cases: All pixel rate outputs, along with all line and frame rate outputs.

Electrical Characteristics

DC Characteristics

(Conditions: VDD = 3.0 ~3.6V, Ta = -20°C ~ +70°C)

Pin Name	Symbol	Parameter	Min	Typ	Max	Unit
Inputs:	V_{IH}	High Level Input Voltage	2.0			V
VD, HD, SCLK, SLOAD, SDATA, ARSTN	V_{IL}	Low Level Input Voltage			0.8	V
	I_{IH}	High Level Input Current			10	uA
	I_{IL}	Low Level Input Current			10	uA
	C_{IN}	Input Capacitance			10	pF
All Outputs	V_{OH}	High Level Output Current I_{OUT} = -50uA	2.9	VDD		V
		High Level Output Current I_{OUT} = -8mA	2.6	VDD		V
	V_{OL}	Low Level Output Current I_{OUT} = 50uA		0	0.1	V
		Low Level Output Current I_{OUT} = 8mA		0	0.4	V
ADCLK, DATACLK, H1_1, H1_2, H2_1, H2_2, HLG_1, HLG_2, PIXCLK, RG, SHD_1, SHD_2, SHP_1, SHP_2,	I_{Omax}	Maximum Output Current	-24		24	mA
AMP_EN, CLPDM, CLPOB, FRAME_VAL, FAST_DUMP, LINE_VAL, PBLK, V1_1, V1_2, V2_1, V2_2, VDISCHG	I_{Omax}	Maximum Output Current	-12		12	mA

Table 5 KSC-1000 DC Characteristics

AC Characteristics

(Conditions: Vdd = 3.0V – 3.6V, Ta = -20°C - +70°C)

Pin Name	Symbol	Parameter	Min	Typ	Max	Units	C_{LOAD}
ADCLK, DATACLK , H1_1, H1_2, H2_1, H2_2, HLG_1, HLG_2, PIXCLK, RG, SHD_1, SHD_2, SHP_1, SHP_2,	t_{RHF}	High Speed Clock Rise Time @ 24mA Drive	445	580	840	pS	10pf
	t_{FHF}	High Speed Clock Fall Time @ 24mA Drive	445	580	890	pS	10pf
	t_{RHS}	High Speed Clock Rise Time 12mA drive	770	1030	1500	pS	10pf
	t_{FHS}	High Speed Clock Fall Time 12mA drive	820	1070	1630	pS	10pf
	t_{PDRH}	Rise Time Delta Propagation Delay	1	5	10	nS	
	t_{PDFH}	Fall Time Delta Propagation Delay	1	5	10	nS	
AMP_EN, CLPDM, CLPOB, FAST_DUMP, FRAME_VAL, LINE_VAL, PBLK, INTG-STRT, V1_1, V1_2, V2_1, V2_2, VDISCGH,	t_{RV}	Low Speed Clock Rise Time	770	1030	1500	pS	10pf
	t_{FV}	Low Speed Clock Fall Time	820	1070	1630	pS	10pf
	t_{PDRV}	Rise Time Delta Propagation Delay		1	5	nS	
	t_{PDFV}	Fall Time Delta Propagation Delay		1	5	nS	

Table 6 KSC-1000 AC Characteristics

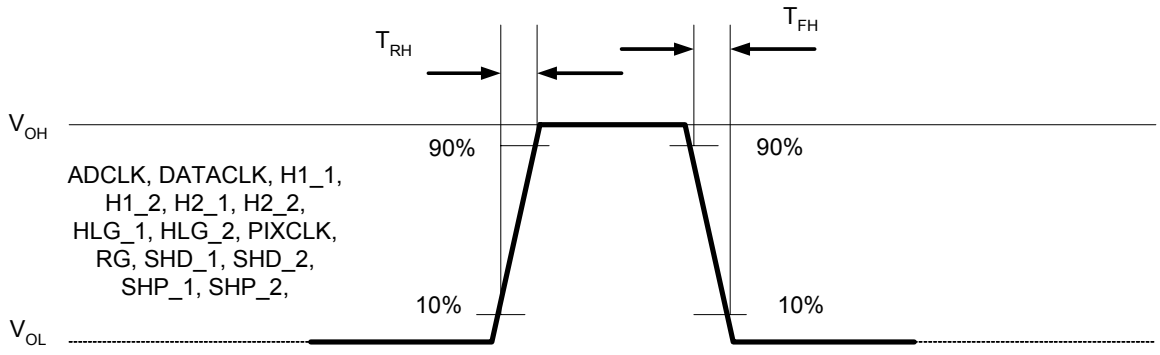


Figure 5 Pixel Rate Signal Rise and Fall Time

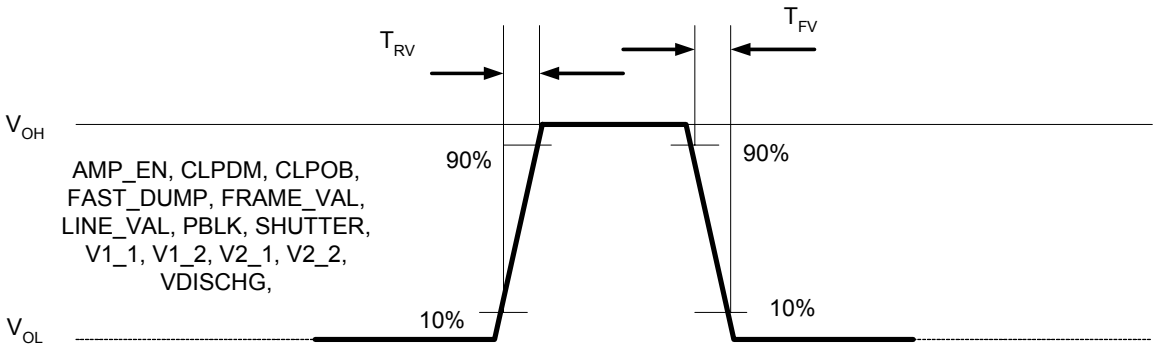


Figure 6 Line and Frame Rate Signal Rise and Fall Time

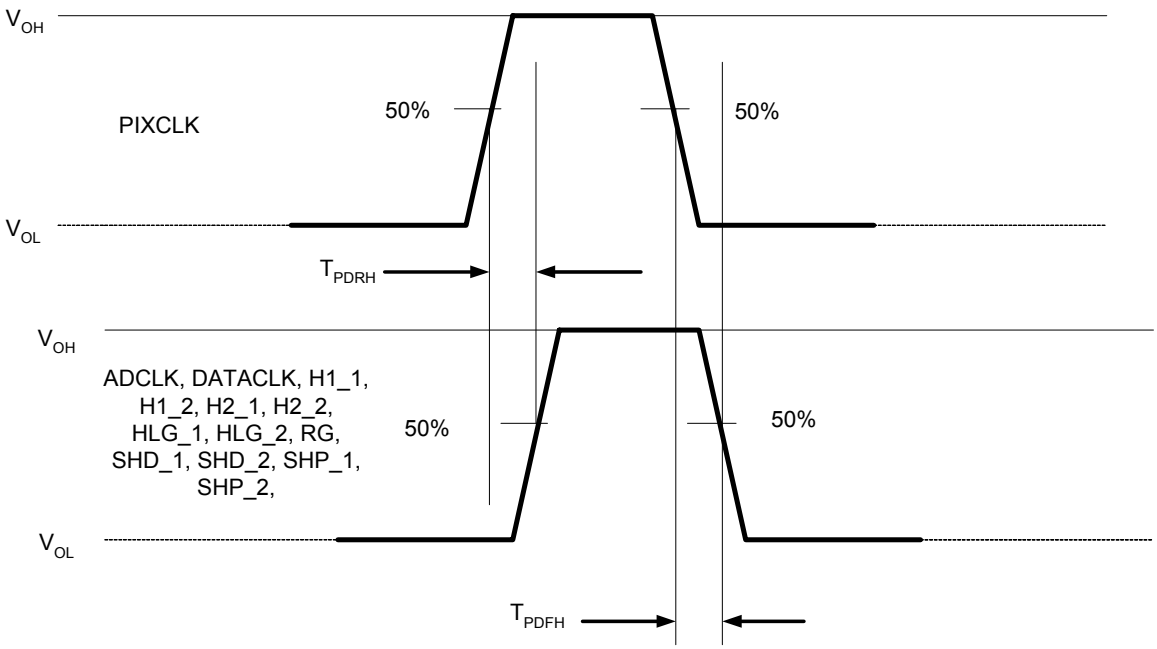


Figure 7 Pixel Rate Signal Rise and Fall Time Delta Propagation Delay

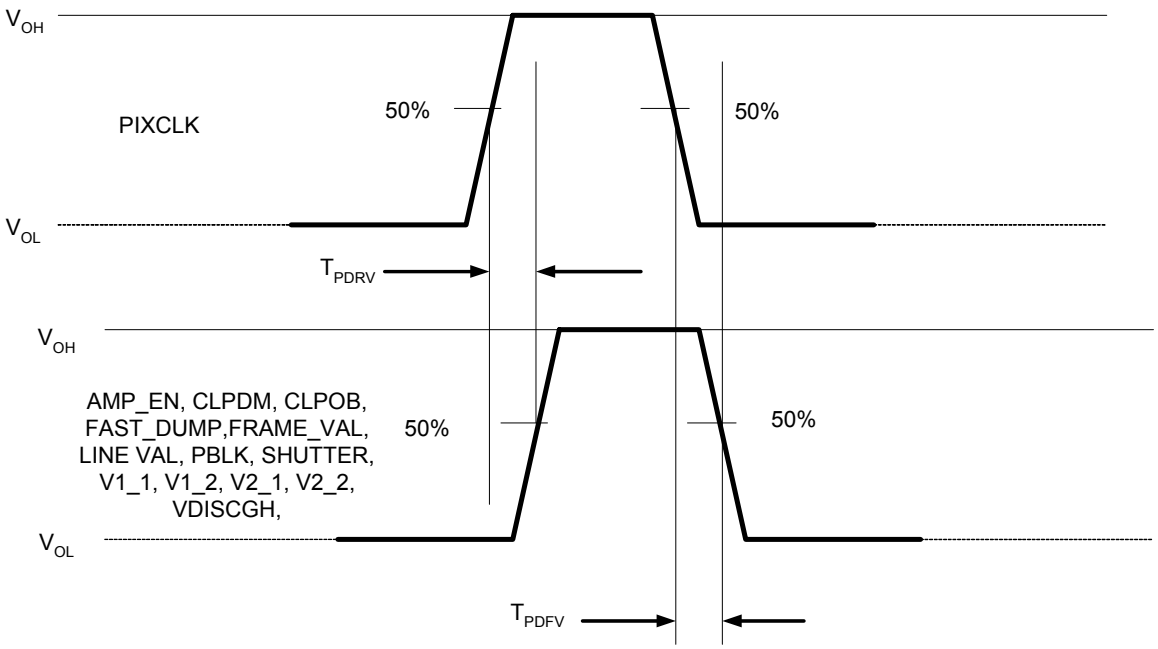


Figure 8 Line and Frame Rate Signal Rise and Fall Time Delta Propagation Delay

Oscillator Buffer Characteristics

Pin Name	Symbol	Parameter	Min	Typ	Max	Unit	Comments
Xtal_I Xtal_O	f	Operating Frequency	8.26		120	MHz	8.26MHz to 10MHz input, as well as 60MHz to 120MHz operation require the use of a clock oscillator. 10MHz to 60MHz input may use a crystal oscillator or a clock oscillator.
On Chip Resistor	R1	Resistance		1		Mohm	On chip resistor formed in N-well diffusion
	TC1	Temperature Coefficient		2.97 e-3			R = R0 * (1 + (TC1 * dT) + (TC2 * dT * dT)), where dT = T - 25°C
	TC2	Temperature Coefficient		1.1e-5			
	C_{R1}	Parasitic Capacitance	858	908	957	fF	Parasitic Capacitance between N-well diffusion and the substrate.
	R2	Series Resistor		30		ohms	
	C1	Crystal Load Capacitance		5.1		pf	
	C2	Crystal Load Capacitance		5.1		pf	

Table 7 Oscillator Buffer Characteristics

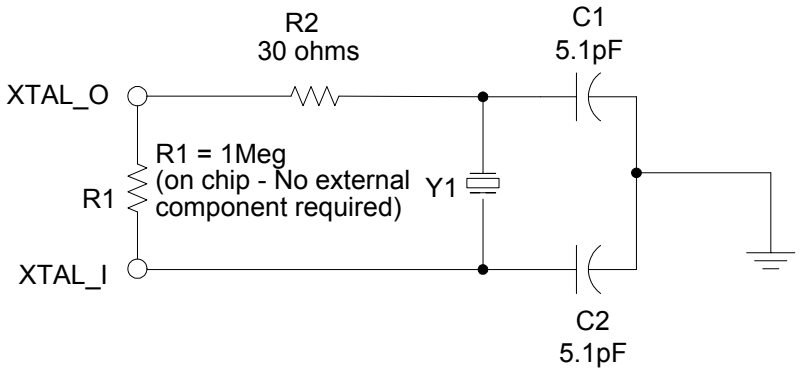


Figure 9 Crystal Oscillator Circuit

DLL Specifications

Pin Name	Parameter	Symbol	Min	Typ	Max	Unit	Comments
CLK_IN (input)	Lock Range	f_{RANGE}	4		65	MHz	Dividing the xtal_in input by 2 will create the clk_in input signal. This guarantees a 50% duty cycle
	Lock Time	t_{LOCK}			10	mS	
	Duty Cycle	d_{CLK_IN}		50		%	
	Input Clk Freq	f_{CLK_IN}	3.26		120	MHz	
CLK(0:63) (output)	Output Clk Freq.	f_{CLK_OUT}	4.13		60	MHz	t_{PHASE_INC} = 1/64 * t_{CLK_IN} where t_{CLK_IN} is the period of clk_in t_{TAP_TOL} = percentage of t_{PHASE_INC} clk(0) offset = (0 * t_{PHASE_INC}) +/- t_{TAP_TOL} clk(1) offset = (1 * t_{PHASE_INC}) +/- t_{TAP_TOL} clk(2) offset = (2 * t_{PHASE_INC}) +/- t_{TAP_TOL} ...etc... clk(63) offset = (63 * t_{PHASE_INC}) +/- t_{TAP_TOL}
	Output Clk Phase Increment	t_{PHASE_INC}	260		3783	pS	
	Output Clk Tap Tolerance	t_{TAP_TOL}	0		50	%	
	Output Clk Duty Cycle	d_{CLK_OUT}		50		%	

Table 8 DLL Specifications

SERIAL INTERFACE SPECIFCATIONS

Timing Specifications

The KSC-1000 utilizes a 3 wire serial interface. Both read and write operations are supported. Individual Registers can be written/read by writing the appropriate address bits and asserting SCLK only for the number of bits in that register. Multiple registers can be written/read by writing the appropriate starting address and asserting SCLK for the total number of bits in the desired registers. When the last bit of one register is reached, the next SCLK assertion writes/reads to the first bit of the next register in the address map. After the last bit of the last register is reached, the serial interface stops writing/reading data, regardless of the state of SL. Note that all address and data transfers proceed from their respective LSBs to MSBs.

For read operation, the address bits are latched on the rising edge. After the 4 address bits are latched in, the data is presented on the subsequent SCLK falling edges.

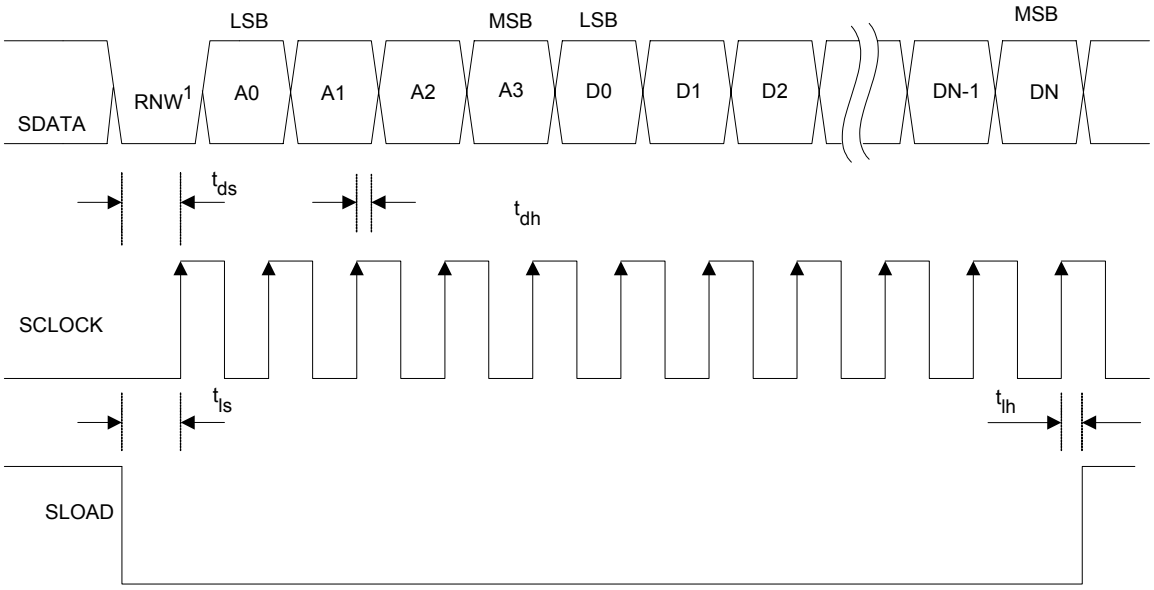


Figure 10 Serial Write Timing

Note 1: RNW Read-Not-Write. Set low for write operation and high for read operation.

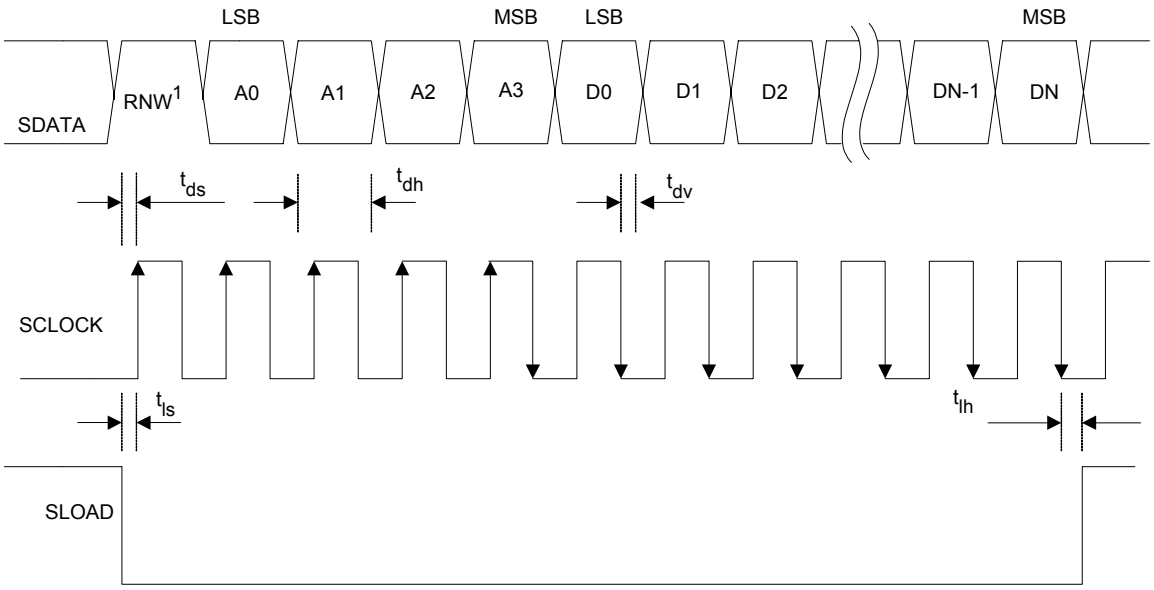


Figure 11 Serial Read Timing

Note 1: RNW Read-Not-Write. Set low for write operation and high for read operation.

Parameter	Description	Min	Typ	Max	Units
f_{sck}	SCLK frequency			20	MHz
t_{ls}	SLOAD to SCLK setup time	10			nS
t_{lh}	SCLK to SLOAD hold time	10			nS
t_{ds}	SDATA valid to SCLK rising edge setup time	10			nS
t_{dh}	SCLK rising edge to SDATA valid hold time	10			nS
t_{dv}	SCLK falling edge to SDATA valid read	10			nS

Table 9 Serial Interface Timing Specifications

Register Descriptions

Register Map

Register Name	Address A0	A1	A2	A3	Total Bits	LSB	MSB
Frame Table Pointer	0	0	0	0	3	Frame Table Address (0)	Frame Table Address (2)
General Setup	1	0	0	0	202	Pixels Per Line (0)	DLL Frequency Range Select (3)
General Control	0	1	0	0	2	Low Power Enable	Memory Table Mode
INTG_STRT Setup	1	1	0	0	30	Electronic Shutter Setup Clocks (0)	Electronic Shutter Hold Clocks (9)
INTG_STRT Line	0	0	1	0	13	Integrate Start Pulse Line Number (0)	Integrate Start Pulse Line Number (12)
Signal Polarity	1	0	1	0	25	H1_1_IDLE _VAL	FAST_DUMP_IDLE_VAL
Offset	0	1	1	0	78	H1_1_OFFSET	DATA_CLK_OFFSET
Width	1	1	1	0	65	H1_1_WIDTH	DATA_CLK_WIDTH
Frame Table Access	0	0	0	1	34	Frame Table Entry (0)	Address (3)
Line table Access	1	0	0	1	20	Line Table Entry (0)	V1_1
Status	0	1	0	1	31	DLL Locked	Line Counter Value (12)

Table 10 Serial Interface Register Map

Frame Table Pointer Register

The KSC-1000 uses frame tables to define the clocking sequence of an image sensor. The Frame Table Register entry points to one of the unique frame tables. The KSC-1000 frame table implementation supports sequencing from mode to mode without writing to the frame pointer register. Writes to the frame pointer register supercede the sequence defined by the frame table and are executed immediately as long as the Memory Table Mode bit in the General Setup Register is set. The low power mode is the only mode where the operation of KSC-1000 is pre-determined and therefore does not require a unique frame table. KSC-1000 supports up to 8 frame tables. The numbering of the frame tables is arbitrary. A frame table can potentially describe a single or multiple operating modes. Conversely, a complex operating mode could require multiple frame tables concatenated together.

Register 0	Frame Table Pointer	Default
Data Length	Register Field	Decimal
3 bits	Frame Table Address (0 through 7)	0

Table 11 Frame Table Pointer Register Map

General Setup Register

The General Setup Register controls the following parameters:

- Horizontal Line Length
- Line sync start and stop pixel locations
- AFE clamping signal start and stop pixel locations
- AFE blanking signal start and stop pixel locations
- Pixel rate clock signal enables
- Pixel rate clock signal drive levels
- DLL frequency range select

Pixels Per Line defines the number of pixels in a horizontal line. Horizontal clocking ends after the number of clock cycles entered in this field has occurred. This count includes all dark, active, buffer, and over-clocked pixels. The Horizontal Pixel Counter starts at count 0 and counts up to the number entered in this field – 1. At that point the vertical clocking interval defined by the current line table starts.

Line Valid Pixel Start defines the pixel on which the line valid signal is asserted. Line Valid Quadrature Start defines where the LINE_VALID signal is asserted relative to the PIXCLK signal. Refer to the Line Valid Quadrature Start Descriptor Table below for a description of the functionality of these bits. Line Valid Pixel End defines the pixel on which the line valid signal is de-asserted. If Line Valid Pixel Start and Line Valid Pixel End are programmed to the same value, the LINE_VALID output will not be asserted.

The CLPOB1_Pix_Start, CLPOB2_Pix_Start, CLPDM1_Pix_Start, CLPDM2_Pix_Start, and PBLK_Pix_Start entries define the pixel on which these signals are asserted. The CLPOB1_Pix_End, CLPOB2_Pix_End, CLPDM1_Pix_End, CLPDM2_Pix_End and PBLK_Pix_End entries define the pixel on which these signals are de-asserted. The lines on which the signals are enabled are defined in the frame table. The polarity of the signals is defined in the Signal Polarity Register, except for PBLK. PBLK polarity is defined in the frame table. If the Start and End entries are the same value, the signals will not be asserted. Note that there are only a single CLOPB and CLPDM output pins. The purpose of having CLPOB1, CLOPB2, CLPDM1, and CLPDM2 register settings is to permit 2 unique pulse width signals to be used at different points in the image capture sequence. For example, CLPDM and CLPOB could be asserted for the entire line during the readout of dark lines and during the dark pixels of active image readout lines. If the PBLK signal is used, it is asserted at its programmed location on the end of a line, remains asserted during the entire vertical clocking interval, and is de-asserted at the programmed location on the new line. Therefore, the minimum PBLK pulse width is the vertical clocking interval period + 1 pixel.

There are enable bits for the following signals: RG, H1_1, H2_1, HLG_1, SHP_1, SHD_1, ADCLK, DATACLK, PIXCLK, H1_2, H2_2, HLG_2, SHP_2, and SHD_2. Clearing these signals drives the outputs to the state defined in the signal polarity register. Setting these signals allows them to toggle as defined in the frame tables. The PIXCLK signal is not controlled within the frame table, therefore the PIXCLK_Enable bit functions as a global enable bit. Setting PIXCLK Enable bit low drives the PIXCLK output low, while setting the bit high allows the PIXCLK signal to toggle. The purpose of the rest of the enable bits is to disable those signals that are not needed for any given application.

The High Speed Clock Drive Select bit sets the output current drive capability of the following outputs: RG, H1_1, H2_1, HLG_1, SHP_1, SHD_1, ADCLK, DATACLK, PIXCLK, H1_2, H2_2, HLG_2, SHP_2, and SHD_2. The 12mA setting allows for power savings and slower rise and fall times for those applications that run at slower clock frequencies.

The DLL Frequency Select bits are used to select the appropriate DLL. The definition of the frequency ranges is described in the register field below.

Register 1	General Setup Register	Default
Data Length	Register Field	Decimal
13 bits	Pixels Per Line	1024
13 bits	Line Valid Pixel Start	0
2 bits	Line Valid Pixel Quadrature Start	0
13 bits	Line Valid Pixel End	0
13 bits	CLPOB1_Pix_Start (Dark Line Frame Rate Clamp)	0
13 bits	CLPOB1_Pix_End (Dark Line Frame Rate Clamp)	0
13 bits	CLPOB2_Pix_Start (Active Readout Line Rate Clamp)	0
13 bits	CLPOB2_Pix_End (Active Readout Line Rate Clamp)	0
13 bits	CLPDM1_Pix_Start (Dark Line Frame Rate Clamp)	0
13 bits	CLPDM1_Pix_End (Dark Line Frame Rate Clamp)	0
13 bits	CLPDM2_Pix_Start (Active Readout Line Rate Clamp)	0
13 bits	CLPDM2_Pix_End (Active Readout Line Rate Clamp)	0
13 bits	PBLK_Pix_Start	0
13 bits	PBLK_Pix_End	0
1 bit	RG_Enable (0 = RG at Idle State, 1 = RG enabled to toggle)	1
1 bit	H1_1_Enable (0 = H1_1 at Idle State, 1 = H1_1 enabled to toggle)	1
1 bit	H2_1_Enable (0 = H2_1 at Idle State, 1 = H2_1 enabled to toggle)	1
1 bit	HLG_1_ Enable (0 = HLG_1 at Idle State, 1 = HLG_1 enabled to toggle)	0
1 bit	SHP_1_Enable (0 = SHP_1 at Idle State, 1 = SHP_1 enabled to toggle)	1
1 bit	SHD_1_Enable (0 = SHD_1 at Idle State, 1 = SHD_1 enabled to toggle)	1
1 bit	ADCLK_Enable (0 = ADCLK at Idle State, 1 = ADCLK enabled to toggle)	1
1 bit	DATACLK_Enable (0 = DATACLK at Idle State, 1 = DATACLK enabled to toggle)	0
1 bit	PIXCLK_Enable (0 = PIXCLK de-asserted, 1 = PIXCLK on)	1
1 bit	H1_2_Enable (0 = H1_2 at Idle State, 1 = H1_2 enabled to toggle)	0
1 bit	H2_2_Enable (0 = H2_2 at Idle State, 1 = H2_2 enabled to toggle)	0
1 bit	HLG_2_Enable (0 = HLG_2 at Idle State, 1 = HLG_2 enabled to toggle)	0
1 bit	SHP_2_Enable (0 = SHP_2 at Idle State, 1 = SHP_2 enabled to toggle)	0
1 bit	SHD_2_Enable (0 = SHD_2 at Idle State, 1 = SHD_2 enabled to toggle)	0
1 bit	H1_1 24mAoutput enable (0 = 12mA, 1 = 24mA)	0
1 bit	H2_1 24mA output enable (0 = 12mA, 1 = 24mA)	0
1 bit	HLG_1 24mA output enable (0 = 12mA, 1 = 24mA)	0
1 bit	SHP_1 24mA output enable (0 = 12mA, 1 = 24mA)	0
1 bit	SHD_1 24mA output enable (0 = 12mA, 1 = 24mA)	0
1 bit	ADCLK 24mA output enable (0 = 12mA, 1 = 24mA)	0
1 bit	DATACLK 24mA output enable (0 = 12mA, 1 = 24mA)	0
1 bit	PIXCLK 24mA output enable (0 = 12mA, 1 = 24mA)	0

1 bit	H1_2 24mA output enable (0 = 12mA, 1 = 24mA)	0
1 bit	H2_2 24mA output enable (0 = 12mA, 1 = 24mA)	0
1 bit	HLG_2 24mA output enable (0 = 12mA, 1 = 24mA)	0
1 bit	SHP_2 24mA output enable (0 = 12mA, 1 = 24mA)	0
1 bit	SHD_2 24mA output enable (0 = 12mA, 1 = 24mA)	0
4 bits	DLL Frequency Range Select 0000 Invalid 0001 Invalid 0010 Invalid 0011 Invalid 0100 4.13MHz to 5.94MHz 0101 5.94MHz to 8.53MHz 0110 8.53MHz to 13.52MHz 0111 13.52MHz to 17.55MHz 1000 17.55MHz to 26.04MHz 1001 26.04MHz to 31.88MHz 1010 31.88MHz to 42.22MHz 1011 42.22MHz to 60.0MHz 1100 Invalid 1101 Invalid 1110 Invalid 1111 Invalid	9

Table 12 General Setup Register Map

Line Valid Pixel Quadrature Start	Description
00	Assert LINE_VALID signal coincident with PIXCLK leading edge (DLL core_clk_0)
01	LINE_VALID signal assertion delayed 90 degrees from PIXCLK leading edge (DLL core_clk_90)
10	LINE_VALID signal assertion delayed 180 degrees from PIXCLK leading edge (DLL core_clk_180)
11	LINE_VALID signal assertion delayed 270 degrees from PIXCLK leading edge (DLL core_clk_270)

Table 13 Line Valid Quadrature Start Descriptor Table

General Control Register

The General Control Register controls the following functions:

- Power Management
- Operation state

The Low Power Enable bit is used to place the KSC-1000 in its low power mode. In this mode the DLL and other clocks except PIXCLK are shut down. Serial programming is enabled in the low power mode. The RAM tables and all registers retain their settings.

Memory table reprogramming is allowed at any time. However, to prevent unexpected operation, it is recommended that the user halt execution of the current frame and line tables prior to reprogramming. De-asserting the Memory Table Mode bit halts execution at the completion of the current line table. Asserting this bit will initiate execution of the frame table pointed to by the Frame Table Pointer Register. The memory tables can also be programmed in the low power mode.

Register 2	General Control Register	Default
Data Length	Register Field	Decimal
1 bit	Low Power Enable (0 = Full Power, 1 = Low Power)	1
1 bit	Memory Table Mode (0 = Programming Mode, 1 = Execution Mode)	0

Table 14 General Control Register Map

INTG_STRT Setup Register

Electronic shuttering is used with the Kodak family of interline sensors. The figure below illustrates the electronic shutter timing with respect to the image sensor horizontal and vertical clocks. t_{essu}, the electronic shutter setup time, is the time from the end of the horizontal clocks to the start of the electronic shutter pulse. t_{es} is the electronic shutter pulse width. t_{esh}, the electronic shutter hold time, is the time from the trailing edge of the electronic shutter pulse to the start of the vertical clocking interval. Note that the line time on which the integrate start pulse is generated is extended by the setup time, shutter pulse width and hold time.

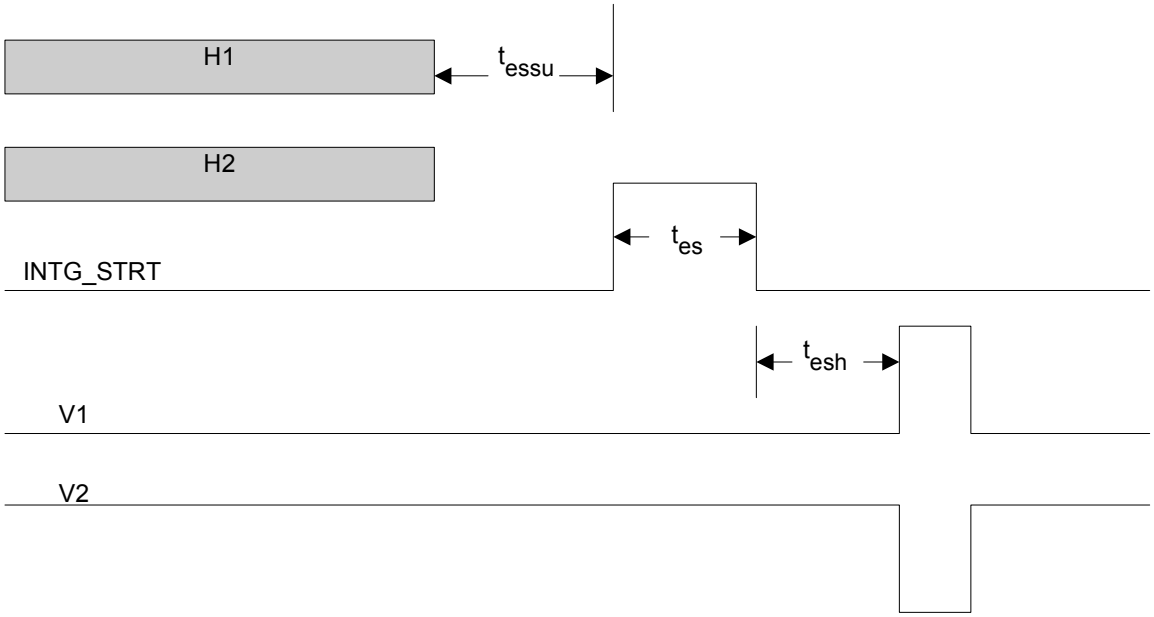


Figure 12 INTG_STRT Timing

Register 3	INTG_STRT Setup Register	Default
Data Length	Register Field	(Decimal)
10 bits	Electronic Shutter Setup Clocks (Pixel clock period counts)	0
10 bits	Electronic Shutter Pulse Width (Pixel clock period counts)	0
10 bits	Electronic Shutter Hold Clocks (Pixel clock period counts)	0

Table 15 INTG_STRT Setup Register Map

INTG_STRT Line Register

The value in this register generates the INTG_STRT clock sequence described in the Integrate Start Setup Register at the start of the programmed line number. The vertical line counter starts at count 0 and counts up. Note that the Check and Increment Line Counter bit in the frame table must be set to allow INTG_STRT pulse generation. Also the Vertical Line Counter must be set to zero at the appropriate time by the Clear Line Counter bit in the frame table.

Register 4	INTG_STRT Line Register	Default
Data Length	Register Field	(Decimal)
13 bits	Integrate Start Pulse Line Number	0

Table 16 INTG_STRT Line Register Map

Signal Polarity Register

Each of the outputs associated with this table have an XOR in their logic path to control the polarity of the output signal. A '0' in the following register means that the output will be '0' when it is inactive. A '1' in the following register inverts the polarity defined in the line table for the V1_1, V1_2, V2_1, V2_2,V_DISCGH, and FAST_DUMP signals, and means that the output will be '1' when it is inactive for the other signals. For example, an H clock's idle value is the level it is held at during vertical clocking. For PBLK, CLPOB, and CLDPM, the idle value is the level it is held at during horizontal clocking in readout mode.

Register 5	Signal Polarity Register	Default
Data Length	Register Field	(Decimal)
1 bit	H1_1_IDLE_VAL (level held during vertical clocking)	0
1 bit	H1_2_IDLE_VAL (level held during vertical clocking)	0
1 bit	H2_1_IDLE_VAL (level held during vertical clocking)	1
1 bit	H2_2_IDLE_VAL (level held during vertical clocking)	1
1 bit	HLG_1_IDLE_VAL (level held during vertical clocking)	0
1 bit	HLG_2_IDLE_VAL (level held during vertical clocking)	0
1 bit	RG_IDLE_VAL (level held during de-asserted state)	0
1 bit	SHP_1_IDLE_VAL (level held during de-asserted state)	1
1 bit	SHP_2_IDLE_VAL (level held during de-asserted state)	1
1 bit	SHD_1_IDLE_VAL (level held during de-asserted state)	1
1 bit	SHD_2_IDLE_VAL (level held during de-asserted state)	1
1 bit	ADCLK_IDLE_VAL (level held when signal is disabled)	0
1 bit	DATA_CLK_IDLE_VAL (level held when signal is disabled)	0
1 bit	CLPOB_IDLE_VAL (level held during de-asserted state)	1
1 bit	CLPDM_IDLE_VAL (level held during de-asserted state)	1
1 bit	AMP_ENABLE_IDLE_VAL (level held during de-asserted state)	0
1 bit	FRAME_VALID_IDLE_VAL (level held during de-asserted state)	0
1 bit	LINE_VALID_IDLE_VAL (level held during de-asserted state)	0
1 bit	INTEGRATE_START_IDLE_VAL (level held during de-asserted state)	0
1 bit	V1_1_IDLE_VAL (used in conjunction with V1_2 to define non-clocking state of KSC-2000 clock driver ASIC)	1
1 bit	V1_2_IDLE_VAL (used in conjunction with V1_1 to define non-clocking state of KSC-2000 clock driver ASIC)	0
1 bit	V2_1_IDLE_VAL (used in conjunction with V2_2 to define non-clocking state of KSC-2000 clock driver ASIC)	1
1 bit	V2_2_IDLE_VAL (used in conjunction with V2_1 to define non-clocking state of KSC-2000 clock driver ASIC)	0
1 bit	V_DISCHG_IDLE_VAL (level held during de-asserted state)	0
1 bit	FAST_DUMP_IDLE_VAL (level held during de-asserted state)	0

Table 17 Signal Polarity Register Map

Offset Register

This register controls the offset of the leading edge of the signals listed below relative to the DLL clk(0) signal for given output.

The offset is defined in units of 1/64th the pixel period. Each entry is 6 bits in length.

Register 6	Offset Register	Default
Data Length	Register Field	(Decimal)
6 bits	H1_1_OFFSET	0
6 bits	H1_2_OFFSET	0
6 bits	H2_1_OFFSET	0
6 bits	H2_2_OFFSET	0
6 bits	HLG_1_OFFSET	0
6 bits	HLG_2_OFFSET	0
6 bits	RG_OFFSET	0
6 bits	SHP_1_OFFSET	0
6 bits	SHP_2_OFFSET	0
6 bits	SHD_1_OFFSET	32
6 bits	SHD_2_OFFSET	32
6 bits	ADCLK_OFFSET	0
6 bits	DATA_CLK_OFFSET	0

Table 18 Offset Register Map

Width Register

This register controls the width of the signals listed below. The width is defined in units of 1/64th the pixel period. Each entry is 5 bits in length, providing a maximum width of ½ the pixel period. The Offset Register Setting positions the leading edge of these signals. The trailing edge of these signals is positioned by setting of this register relative to the setting of the Offset Register. The H1, H2, HLG, ADCLK, and DATACLK outputs are adjustable from 1/4 duty cycle to 47/64 duty cycle. The SHP, SHD, and RG outputs are adjustable from 1/64 duty cycle to ½ duty cycle.

Register 7	Width Register	Default
Data Length	Register Field	(Decimal)
5 bits	H1_1 WIDTH (0 = ¼ duty cycle, 16 = ½ duty cycle, 31 = 47/64 duty cycle)	16
5 bits	H1_2 WIDTH (0 = ¼ duty cycle, 16 = ½ duty cycle, 31 = 47/64 duty cycle)	16
5 bits	H2_1 WIDTH (0 = ¼ duty cycle, 16 = ½ duty cycle, 31 = 47/64 duty cycle)	16
5 bits	H2_2 WIDTH (0 = ¼ duty cycle, 16 = ½ duty cycle, 31 = 47/64 duty cycle)	16
5 bits	HLG_1 WIDTH (0 = ¼ duty cycle, 16 = ½ duty cycle, 31 = 47/64 duty cycle)	16
5 bits	HLG_2 WIDTH (0 = ¼ duty cycle, 16 = ½ duty cycle, 31 = 47/64 duty cycle)	16
5 bits	RG_WIDTH (0 = ½ duty cycle, 1 = 1/64 duty cycle, 31 = 31/64 duty cycle)	7
5 bits	SHP_1_WIDTH (0 = ½ duty cycle, 1 = 1/64 duty cycle, 31 = 31/64 duty cycle)	14
5 bits	SHP_2_WIDTH (0 = ½ duty cycle, 1 = 1/64 duty cycle, 31 = 31/64 duty cycle)	14
5 bits	SHD_1_WIDTH (0 = ½ duty cycle, 1 = 1/64 duty cycle, 31 = 31/64 duty cycle)	14
5 bits	SHD_2_WIDTH (0 = ½ duty cycle, 1 = 1/64 duty cycle, 31 = 31/64 duty cycle)	14
5 bits	ADCLK_WIDTH (0 = ¼ duty cycle, 16 = ½ duty cycle, 31 = 47/64 duty cycle)	16
5 bits	DATA_CLK_WIDTH (0 = ¼ duty cycle, 16 = ½ duty cycle, 31 = 47/64 duty cycle)	16

Table 19 Width Register Map

Frame Table Access Register

The Frame Table Access Register is used to program the Frame Tables. The Frame Tables can only be programmed in low power mode or when the Memory Table Mode bit of the General Purpose Control Register is set to Programming Mode. There are 8 unique Frame Tables. Each Frame Table can contain up to 16 entries. Frame tables can be concatenated together to form very complex sensor clocking patterns. The Count and Flag fields together with VD signal control the sequencing from Frame Table to Frame Table as well as looping within a frame table

The frame table address needs to be written only once during programming. Each subsequent group of 34 bits programs a row in the frame table. Programming automatically sequences to the next Frame Table number.

Register 8	Frame Table Access Register	Default
Data Length	Register Field	(Decimal)
7 bits	Frame Table Address	0
34 bits	Frame Table Data	0

Table 20 Frame Table Access Register Map

Frame Table Address Descriptor

Bit Location	Name	Description
0:3	Entry Numbe	One of 16 possible entries (15:0). Each entry points to a line table to define the vertical clocking interval.
4:6	Table Numbe	One of 8 possible frame tables (7:0). Any given sensor operational mode has 1 or more frame tables associated with it.

Table 21 Frame Table Address Descriptor

Frame Table Data Descriptor

Bit Location	Name	Description
0	Check and Increment Line Counter	0 = do not increment the line counter or enable comparison to the Integrate Start Line Register, 1 = increment the line counter and enable comparison to the Integrate Start Line Register. The comparison occurs prior to the increment.
1	Clear Line Counter	0 = do not clear the line counter, 1 = clear the line counter
2	Force Shutter	0 = SHUTTER assertion occurs only if the Check and Increment Line Counter bit is set AND the Line Counter value matches the value programmed in the Shutter Start Line Register. 1 = Assert SHUTTER as defined in the Shutter Start Setup Register at the beginning of the line, regardless of the Line Counter Value and the state of the Check Increment Line Counter bit
3:4	Horizontal Binnin Factor	00 = No Binning, 1 RG clock and A/D clock per horizontal clock 01 = 1 RG clock and A/D clock per every 2 horizontal clocks 10 = 1 RG clock and AD clock per every 3 horizontal clocks 11 = 1 RG clock and AD clock per every 4 horizontal clocks
5	HCLK_V Enable	0 = Disable HCLCK generation during VCLK interval 1 = Allow HCLK generation during VCLK interval
6	LINE_VALID Enable	0 = De-assert LINE_VALID 1 = Allow LINE_VALID to run as specified in the General Setup Register
7	FRAME_VALID Enable	0 = De-assert FRAME_VALID 1 = Assert FRAME_VALID; directly controls output pin
8	Video Amplifier	0 = De-assert AMP_ENABLE,

	Enable	1 = Assert AMP_ENABLE; directly controls the output pin
9	AFE Clock Enable	0 = De-assert ADCLK, DATACLK, SHP_1, SHP_2, SHD_1, SHD_2 1 = Allow clocks to run
10	CLPDM2 Enable	0 = De-assert CLPDM 1 = Allow CLPDM to run as specified in General Setup Register
11	CLPDM1 Enable	0 = De-assert CLPDM 1 = Allow CLPDM to run as specified in General Setup Register
12	CLPOB2 Enable	0 = De-assert CLPOB 1 = Allow CLPOB to run as specified in General Setup Register
13	CLPOB1 Enable	0 = De-assert CLPOB 1 = Allow CLPOB to run as specified in General Setup Register
14	PBLK Enable	0 = De-assert PBLK 1 = Allow PBLK to run as specified in General Setup Register
15	Pblk_Idle_Val	Level held during de-asserted state
16	Flag	Refer to Frame Table Event Descriptor for details
17:29	Count	Refer to Frame Table Event Descriptor for details
30:32	Address 2:0	Refer to Frame Table Event Descriptor for details
33	Address 3	Refer to Frame Table Event Descriptor for details

Table 22 Frame Table Data Descriptor

Frame Table Sequence Control

Frame tables can be coded such that no external intervention is required for sequencing within a frame table or sequencing between frame tables. However, there may be instances where external intervention is desired. In a typical camera system, an external controller may be monitoring the state of the shutter button. Detecting a button press would start a camera system integrate and readout operation.

An external controller can use the VD signal to control frame table sequencing. In the above example the frame table could be coded in such a way that the camera system is performing a decimated preview image readout indefinitely until the VD signal is asserted. Upon detecting the VD signal assertion, execution of the current line table sequence is completed and the frame table execution continues at the instruction destination address.

VD is asserted by driving to a logic high. The state of the VD line is ignored for those frame table instructions listed in Table 23 that have the state of VD event listed as don't care (X). Frame table instructions are described in Table 23.

Frame Table Event Descriptor

Count	Flag	VD Event	Address(3)	Address(2:0)	Mnemonic	Action
0	0	X	0	Frame Table Address	JMPFT	Jump to entry 0 of the frame table indicated in the Address(2:0)field.
0	0	0	1	Frame Table Address	INC	Go to next line in the current frame table.
0	0	1	1	Frame Table Address	BRVD	Jump to entry 0 of the frame table indicated in the Address(2:0)field.
0	1	0	Line Table Address (3)	Line Table Address (2:0)	WVD	Execute line table indicated in the Address(3;0) field indefinitely until a VD event occurs.
0	1	1	Line Table Address (3)	Line Table Address (2:0)	INCVD	Complete execution of the Line Table indicated in the Address(3:0) field. Go to the next frame table entry when completed.
>0	0	X	Line Table Address (3)	Line Table Address (2:0)	ELT	Execute the Line Table indicated in the Address(3:0) field the number of times indicated in the Count field. Jump to the next frame table entry when completed.
>0	1	X	Frame Table Entry (3)	Frame Table Entry (2:0)	INCZ	Store Count as a variable. Jump to frame table entry pointed to by the Address field. Decrement the count variable. If the count variable > 0 jump to frame table entry pointed to by the Address field. Go to the next frame table entry when Count variable count = 0. Note: Nesting of INCZ instructions is not supported.

Table 23 Frame Table Event Descriptor

Horizontal Binning Factor	Description
00	No Binning, 1 RG clock and A/D clock per horizontal clock
01	1 RG clock and A/D clock per every 2 horizontal clocks
10	1 RG clock and AD clock per every 3 horizontal clocks
11	1 RG clock and AD clock per every 4 horizontal clocks

Table 24 Horizontal Binning Factor Descriptor

Line Table Access Register

The Line Table Access Register is used to program the Line Tables. Programming of the Line Tables is permitted only in low power mode or when the Memory Table Mode bit of the General Purpose Control Register is set to Programming Mode. There are 16 unique Line Tables. Each Line Table can contain up to 16 entries. Line Table sequencing is controlled by the Frame Tables.

Register 9	Line Table Access Register	Default
Data Length	Register Field	Decimal
8 bits	Line Table Address	0
20 bits	Line Table Data	0

Table 25 Line Table Access Register Map

Line Table Address Descriptor

Bit Location	Name	Description
0:3	Entry Numbe	One of 16 possible entries (15:0). Each entry describes a portion of a complete Vertical Clock Sequence
4:7	Table Numbe	One of 16 possible line tables (15:0). Any given sensor operational mode has 1 or more line tables associated with it.

Table 26 Line Table Address Descriptor

Line Table Data Descriptor

Bit Location	Name	Description
0:12	Count	Number of pixel clock counts to execute this line table entry
13	HCLK_H Enable	0 = do not allow HCLKS to run during or after completion of this entry, 1 = allow HCLCKS to run
14	Fast Dump	0 = Fast Dump de-asserted, 1 = Fast Dump asserted, polarity depends upon Signal Polarity Register setting
15	VDISCHG	0 = Disable HCLCK generation during VCLK interval 1 = Allow HCLK generation during VCLK interval
16	V2_2	0 = V2_2 de-asserted, 1 = V2_2 asserted, polarity depends upon Signal Polarity Register setting;
17	V2_1	0 = V2_1 de-asserted, 1 = V2_1 asserted, polarity depends upon Signal Polarity Register setting;
18	V1_2	0 = V1_2 de-asserted, 1 = V1_2 asserted, polarity depends upon Signal Polarity Register setting;
19	V1_1	0 = V1_1 de-asserted, 1 = V1_1 asserted, polarity depends upon Signal Polarity Register setting

Table 27 Line Table Data Descriptor

Status Register

The Status Register is a read only register which provides DLL, Frame Table, Line Table, and VD status.

Register 10	Status Register	Default
Data Length	Description	Decimal
1 bit	DLL Locked, 0 = DLL not locked, 1 = DLL locked	NA
7 bits	Current Frame Table Address	NA
8 bits	Current Line Table Address	NA
1 bit	VD Registered, 0 = VD not registered, 1 = VD registered	NA
1bit	VD Wait 0 = not currently waiting for VD, 1 = waiting for VD	NA
13 bits	Line Counter Value	NA

Table 28 Status Register Map

MECHANICAL DRAWINGS

Package

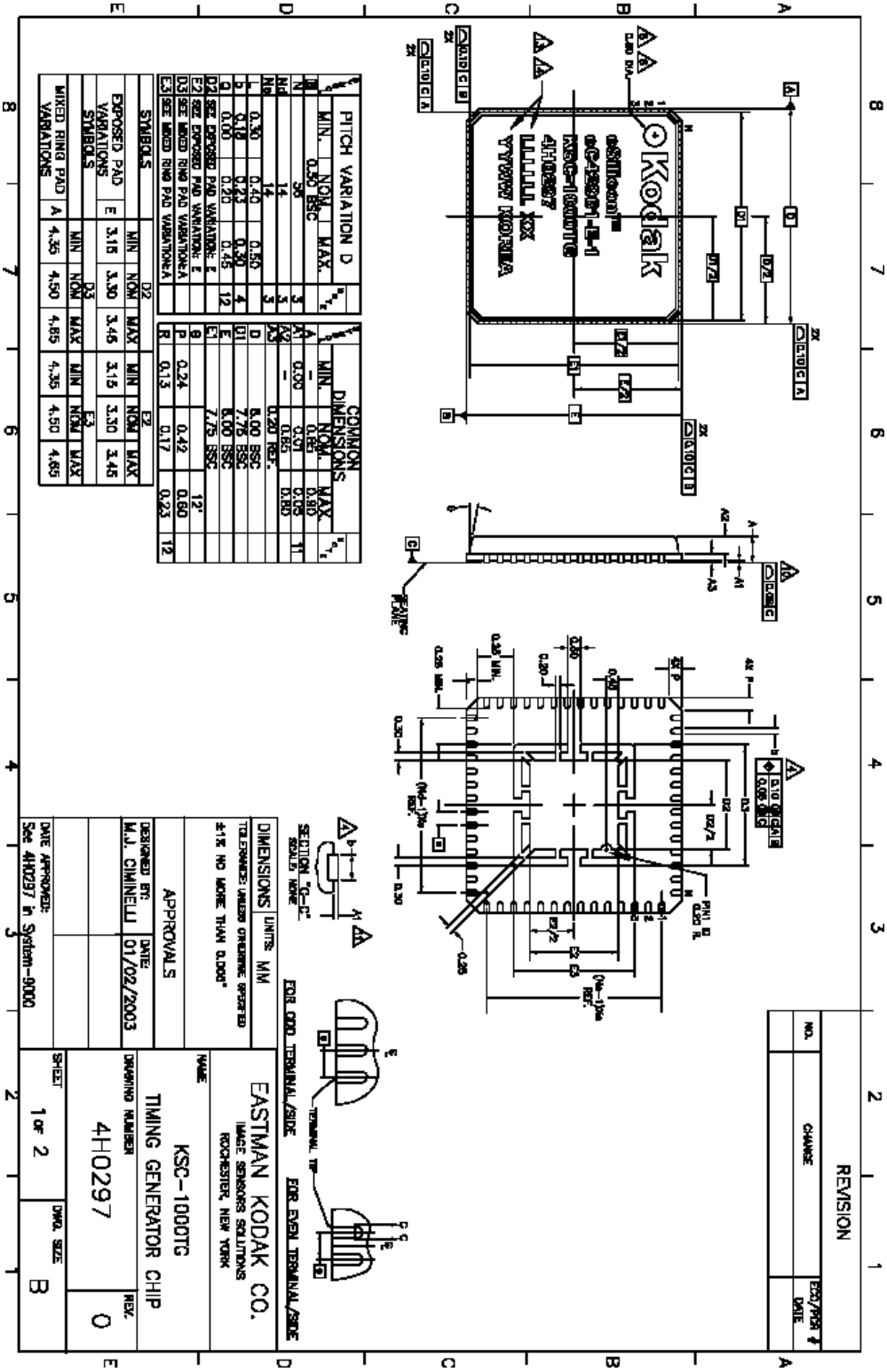
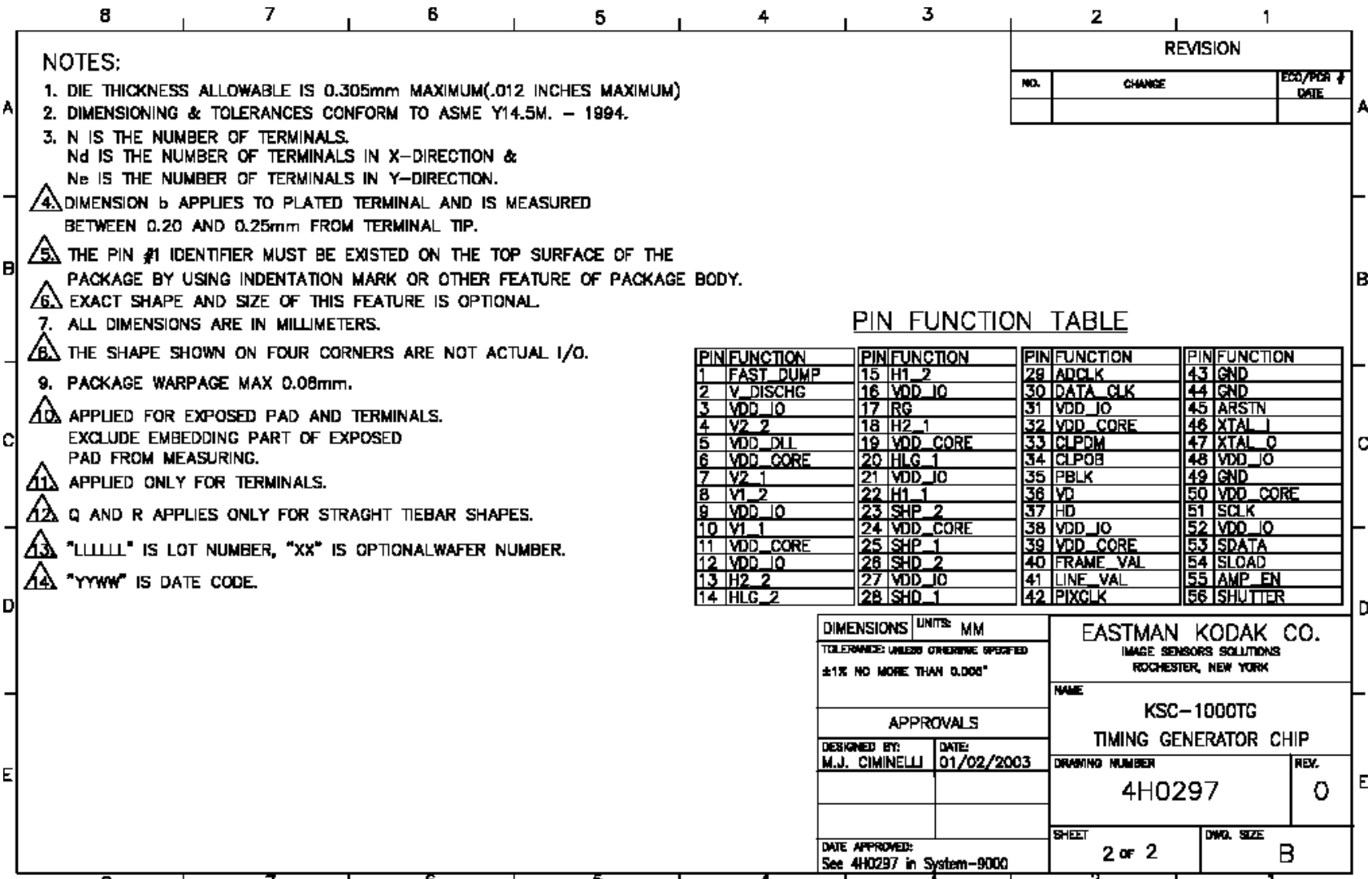


Figure 13 KSC-1000 Package Drawing Page 1



NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM(.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.
9. PACKAGE WARPAGE MAX 0.08mm.
10. APPLIED FOR EXPOSED PAD AND TERMINALS.
    EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
11. APPLIED ONLY FOR TERMINALS.
12. Q AND R APPLIES ONLY FOR STRAGHT TIEBAR SHAPES.
13. "LLLLLL" IS LOT NUMBER, "XX" IS OPTIONALWAFER NUMBER.
14. "YYWW" IS DATE CODE.

REVISION

NO.	CHANGE	ECO/PCR # DATE

PIN FUNCTION TABLE

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	FAST_DUMP	15	H1_2	29	ADCLK	43	GND
2	V_DISCHG	16	VDD_IO	30	DATA_CLK	44	GND
3	VDD_IO	17	RG	31	VDD_IO	45	ARSTN
4	V2_2	18	H2_1	32	VDD_CORE	46	XTAL_I
5	VDD_DLL	19	VDD_CORE	33	CLPDM	47	XTAL_O
6	VDD_CORE	20	HLG_1	34	CLPOB	48	VDD_IO
7	V2_1	21	VDD_IO	35	PBLK	49	GND
8	V1_2	22	H1_1	36	VD	50	VDD_CORE
9	VDD_IO	23	SHP_2	37	HD	51	SCLK
10	V1_1	24	VDD_CORE	38	VDD_IO	52	VDD_IO
11	VDD_CORE	25	SHP_1	39	VDD_CORE	53	SDATA
12	VDD_IO	26	SHD_2	40	FRAME_VAL	54	SLOAD
13	H2_2	27	VDD_IO	41	LINE_VAL	55	AMP_EN
14	HLG_2	28	SHD_1	42	PIXCLK	56	SHUTTER

DIMENSIONS UNITS: MM
TOLERANCE: UNLESS OTHERWISE SPECIFIED
±1% NO MORE THAN 0.005"

APPROVALS

DESIGNED BY:	DATE:
M.J. CIMINELLI	01/02/2003

DATE APPROVED: See 4H0297 in System–9000

EASTMAN KODAK CO.
IMAGE SENSORS SOLUTIONS
ROCHESTER, NEW YORK

NAME
KSC–1000TG
TIMING GENERATOR CHIP

DRAWING NUMBER 4H0297
REV. 0
SHEET 2 OF 2
DWG. SIZE B

Figure 14 KSC-1000 Package Drawing Page 2

PC Board Geometry and Attachment

The package is a 8mm x 8mm Micro leadframe (MLF) package. The package itself is Lead (Pb) free, with a Cu-alloy lead frame and pure tin plating. The package has been qualified for both 240°C and 260°C peak temperature soldering profiles. These higher temperature profiles are usually associated lead (Pb) free soldering conditions.

The package features a large exposed metal pad on to which the silicon ASIC is attached. This provides a low impedance ground connection when soldered directly to a printed circuit board. Numerous ASIC ground connections are made between the silicon die and the exposed center pad, therefore a good solder connection to the back of the package is imperative for the specified performance.

The PC board geometry specified includes a large metallization on to which the die will be soldered. This metallization needs to be connected to the ground plane of the PC board. This is done by a 4 x 4 array of vias between the top metallization and the ground plane. Each of the vias is covered with solder mask to prevent solder from flowing into it. If the solder flows into the via, the uniformity of the solder bond is compromised and voids will form.

The solder connection that provides the ground should contact the inner large exposed pad. **It is not necessary or recommended to attach the outer ring pad to the ground plane**. The solder stencil pattern is used to define the areas where the package is soldered to the PC board. A solder stencil thickness of 0.125 mm is recommended for parts with 0.5mm pitch, such as this one. Since not enough space is available underneath the part after reflow, the package manufacturer recommends that a “No Clean”, Type 3 paste be used for mounting MLF packages.

In the following figures, the solder mask is not defined for the perimeter pads. At this pad pitch and size, manufacturers differ on whether they prefer to mask each perimeter pad individually or to open all the perimeter pads collectively within one large rectangle. The solder mask that is shown in the figures is to “tent” the via holes in the center ground pad. The tenting of the via holes is not critical. The size of the solder mask should, at the minimum, be the larger than the via holes by the PC board manufacturing alignment tolerance. There will also be solder mask between the large center ground connection and the I/O pads but this is not explicitly shown.

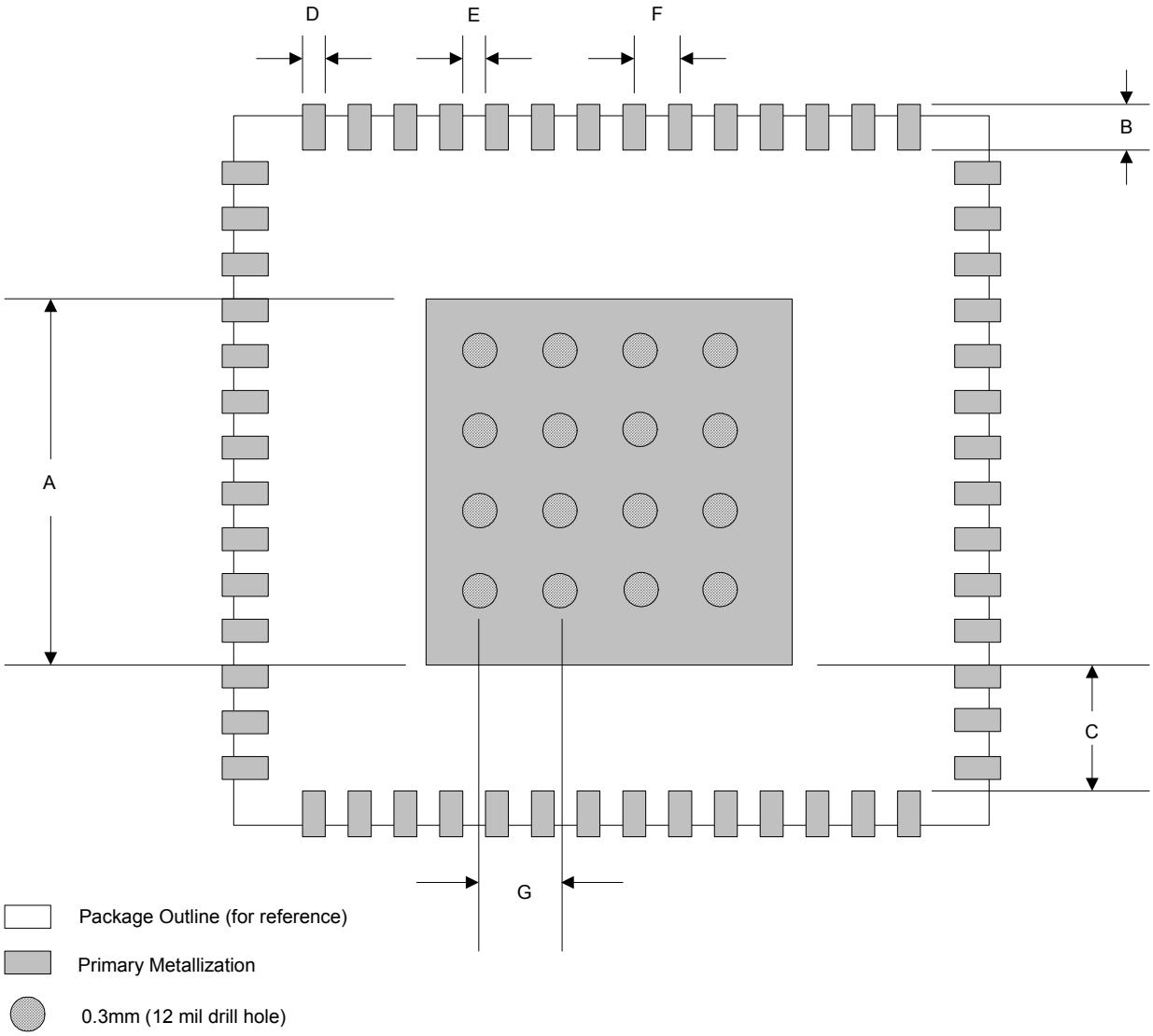


Figure 15 KSC-1000 PC Board Geometry

Label	Description	Distance (mm)	Distance (mils)
A	Ground Pad Dimension	3.5	137.78
B	I/O Pad Length	0.69	27.16
C	Ground Pad to IO Pad Spacing	1.74	68.49
D	IO Pad Width	0.28	11.10
E	IO Pad Space	0.22	8.66
F	IO Pad Center to Center	0.5	19.68
G	Via Hole Spacing	0.8	31.49

Table 29 KSC-1000 PC Board Geometry Dimensions

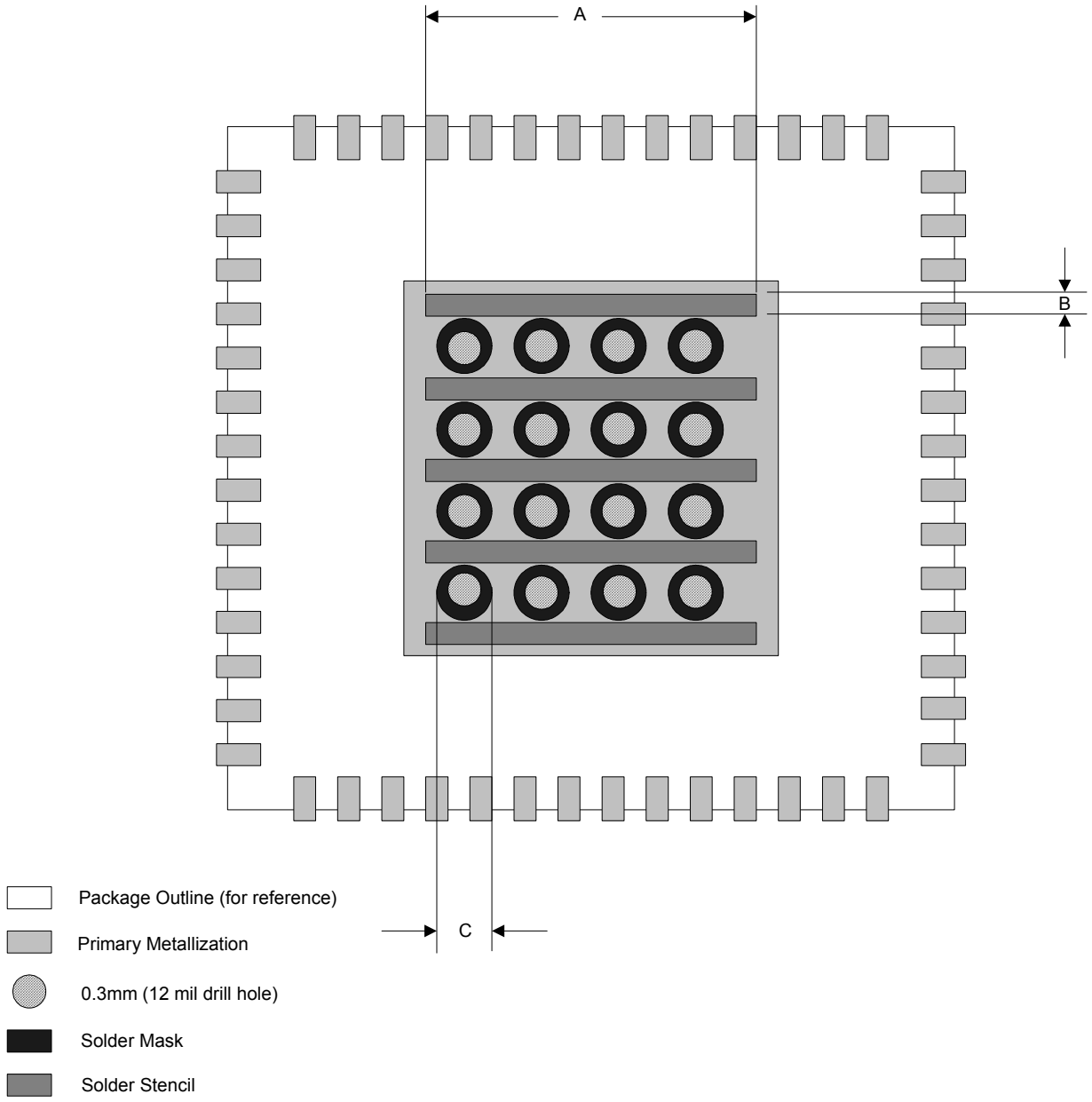


Figure 16 KSC-1000 Ground Paddle Solder Stencil and Solder Mask

Label	Description	Distance (mm)	Distance (mils)
A	Solder Pattern Length (Solder Stencil Defined)	3.4	133.84
B	Solder Pattern Width(Solder Stencil Defined)	0.35	13.78
C	Solder Mask Via “tent” diameter	0.4	15.75

Table 30 KSC-1000 Ground Paddle Solder Stencil and Solder Mask Dimensions

Package Moisture Sensitivity Level

The KSC-1000 MLF package has Moisture Sensitivity Level (MSL) rating of 3. The devices are shipped in a vacuum-sealed bag. The shelf life in the bag is 12 months when stored at a temperature of less than 40˚C and a relative humidity level of less than 90%. After the bag is opened, the devices must be stored at a temperature of less than 30˚C and a relative humidity level of less than 60% for a maximum of 1 week. If any of these conditions are exceeded, the devices will require baking for 8 hours at 125˚C for 8 hours per JEDEC J-STD-033.

QUALITY ASSURANCE AND RELIABILITY

Quality Strategy: All CCD timing generators will conform to the specifications stated in this document. This will be accomplished through a combination of statistical process control and inspection at key points of the production process. Typical specification limits are not guaranteed but provided as a design target. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

Replacement: All devices are warranted against failure in accordance with the terms of Terms of Sale. This does not include failure due to mechanical and electrical causes defined as the liability of the customer below.

Liability of the Supplier: A reject is defined as an CCD timing generator that does not meet all of the specifications in this document upon receipt by the customer.

Liability of the Customer: Damage from mechanical, electrostatic discharge (ESD) damage, or other electrical misuse of the device beyond the stated absolute maximum ratings, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

ESD Precautions: Devices are shipped in static-safe containers and should only be handled at static-safe workstations. See ISS Application Note MTD/PS-0224 for handling recommendations.

Reliability: Reliability results are available from the Image Sensor Solutions and can be supplied upon request. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

Mechanical: The device assembly drawing is provided as a reference. The device will conform to the published package tolerances.

ORDERING INFORMATION

Available Part Configurations

Type	Description
KSC-1000	CCD Timing Generator

Please contact Image Sensor Solutions for available part numbers.

Address all inquiries and purchase orders to:

Image Sensor Solutions
Eastman Kodak Company
Rochester, New York 14650-2010
Phone: (585) 722-4385
Fax: (585) 477-4947
E-mail: imagers@kodak.com

WARNING: LIFE SUPPORT APPLICATIONS POLICY

Kodak image sensors and support ASICS are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury or property or other consequential damages.

REVISION CHANGES

Revision Number	Description of Changes
1.0	Initial release