STRUCTURE Silicon Monolithic Integrated Circuit

TYPE 2channel Step-Down Switching Regulator Controller

(Channel 2 : Synchronous Rectification Configuration)

PRODUCT SERIES **BD9775FV**

FEATURES
- 2channel Power MOS FET driver
- Synchronous rectification for channel 2
- Able to synchronize to an external clock signal
- Over Current Protection (OCP) by monitoring VDS of P channel FET
- Short Circuit Protection (SCP) by delay time and latch method
- Under Voltage Lock Out (UVLO)
- Thermal Shut Down (TSD)
- Stand-by / Active control for each channel
- Package : SSOP-B28

○Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Limits	Units
Supply Voltage (VCC to GND)	Vcc	36	V
VREF to GND Voltage	Vref	7	V
VREGA to GND Voltage	Vrega	7	V
VREGB to VCC Voltage	Vregb	7	V
OUT1, OUT2H to VCC Voltage	Vouth	7	V
OUT2L to GND Voltage	Voutl	7	V
Power Dissipation	Pd	640(*1)	MW
Operating Temperature Range	Topr	-40～+85	℃
Storage Temperature Range	Tstg	-55～+125	℃
Junction Temperature	Tjmax	+125	℃

(*1) Without heat sink, reduce to 6.4mW when Ta=25℃ or above

Pd is 850mW mounted on 70x70x1.6mm, and reduce to 8.5mW/℃ above 25℃.

○Recommended operating conditions

Parameter	Symbol	Limits			Units
		MIN	TYP	MAX	
Supply Voltage	Vcc	6.0	-	30.0	V
Oscillating Frequency	Fosc	30	100	300	KHz
Timing Resistance	RT	10	27	56	kΩ
Timing Capacitance	CT	100	470	4700	pF

Status of this document

The Japanese language version of this document shall be the official specification.

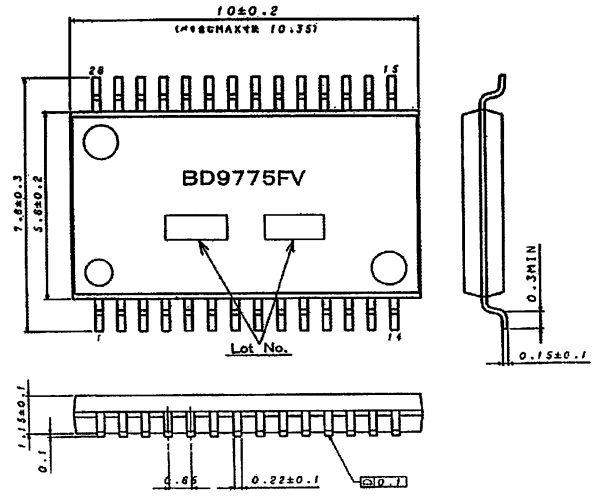
Any translation of this document shall be for reference only.

○Electrical characteristics(Ta=25℃, VCC=13.2V, fosc=100kHz, CTL1=3V, CTL2=3V)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
【Whole Device】						
Stand-by Current	Iccst	—	—	5	μA	CTL1,CTL2=0V
Cirvuit Current	Icc	2.5	4.2	7	mA	FB1,FB2=0V
【Reference Voltage】						
VREF Output Voltage	Vref	2.97	3.00	3.03	V	Io=-1mA
Line Regulation	DVli	—	—	10	mV	Vcc=7～18V,Io=-1mA
Load Regulation	DVlo	—	—	10	mV	Io=-0.1mA～-2mA
Short Output Current	Ios	-60	-22	-5	mA	
【Internal Voltage Regulator】						
VREGA Output Voltage	Vrega	4.5	5.0	5.5	V	Switching with COUT=5000pF
VREGB Output Voltage	Vregb	VCC -5.5	VCC -5.0	VCC -4.5	V	Switching with COUT=5000pF
VREGB Dropout Voltage	Vdregb	—	1.8	2.2	V	VREGB to GND Voltage
【Oscillator】						
Oscillating Frequency	fosc	90	100	110	kHz	RT=27kΩ,CT=470pF
Frequency Tolerance	Dfosc	—	—	2	%	Vcc=7～18V
【Synchronized Frequency】						
Synchronized Frequency	fosc2	—	120	—	kHz	FIN=120kHz
FIN Threshold Voltage	Vthfin	1.2	1.4	1.6	V	
FIN Input Current	Ifin	-1	—	1	μA	VFIN=1.4V
【Error Amplifier】						
Threshold Voltage	Vthea	0.98	1.00	1.02	V	
INV Input Bias Current	Ibias	-1	—	1	μA	
Voltage Gain	Av	—	70	—	dB	DC
Band Width	Bw	—	2.0	—	MHz	Av=0dB
Maximum Output Voltage	Vfbh	2.2	2.4	2.6	V	INV=0.5V
Minimum Output Voltage	Vfbl	—	—	0.1	V	INV=1.5V
Output Sink Current	Isink	0.5	2	5.2	mA	FB1,2 Terminal
Output Source Current	Isource1	-170	-110	-70	μA	FB1 Terminal
	Isource2	-200	-130	-85	μA	FB2 Terminal
【PWM Comparator】						
Threshold Voltage at 0%	Vth0	0.88	0.98	1.08	V	FB Voltage
Threshold Voltage at 100%	Vth100	1.88	1.98	2.08	V	FB Voltage
DTC Input Bias Current	Idtc	-1	—	1	μA	
【FET Driver】						
Sink Current	Isink	20	36	58	mA	VDS=0.4V
Source Current	Isource	-510	-320	-180	mA	VDS=0.4V
ON Resistance	RonN	7.0	11.0	17.8	Ω	OUT1,2H,2L : L
	RonP	0.7	1.4	2.2	Ω	OUT1,2H,2L : H
Rise Time	Tr	—	20	—	nsec	Switching with COUT=5000pF
Fall Time	Tf	—	100	—	nsec	Switching with COUT=5000pF
Driver's Duty Cycle of Synchronous Rectification	Δ Duty	42	45	48	%	RSYNC=30KΩ, 50% of main driver's duty cycle
SYNC Terminal Voltage	Vsync	1.45	1.55	1.65	V	RSYNC=30KΩ, FB=1.5V
【Over Current Protection (OCP)】						
VS Threshold Voltage	Vths	VCC -0.24	VCC -0.21	VCC -0.18	V	RCL=21kΩ, the output tern off after detected 8 cycle
VS Input Current	IVSH	-1	—	1	μA	VS1,VS2=VCC
	IVSL	-1	—	1	μA	VS1,VS2=0V
CL Input Current	Icl	9	10	11	μA	
【Stand-by】						
Threshold Voltage	Vctl	1.0	1.5	2.0	V	
CTL Input Current	Ictl	6	15	30	μA	CTL1,CTL2=3V
【Short Circuit Protection (SCP)】						
Timer Start Voltage	Vtime	0.6	0.7	0.8	V	INV Voltage
Threshold Voltage	Vthscp	1.92	2.00	2.08	V	SCP Voltage
Stand-by Voltage	Vstscp	—	10	100	mV	SCP Voltage
Source current	Isoscp	-4.0	-2.5	-1.5	μA	SCP=1.0V
【Under Voltage Lock Out (UVLO)】						
Threshold Voltage	Vuvlo	5.6	5.7	5.8	V	Vcc sweep down
Hysteresis Voltage Range	DVuvlo	0.05	0.1	0.15	V	

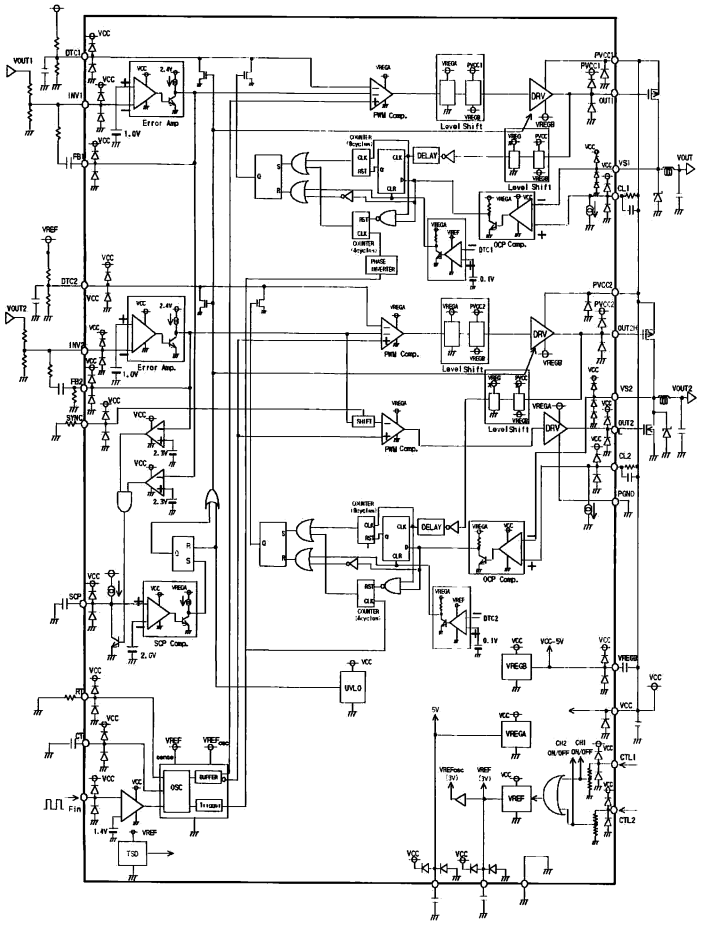
Note : This Product is not designed for normal operation within a radioactive environment.

○Package Dimensions



SSOP-B28 (Unit:mm)

○Block Diagram



○Pin Description

Pin No.	Pin Name	Description
1	FB1	Error amplifier output pin (Channel 1)
2	INV1	Error amplifier negative input pin (Channel 1)
3	RT	Oscillator frequency adjustment pin connected resistor
4	CT	Oscillator frequency adjustment pin connected capacitor
5	FIN	Oscillator synchronization pulse signal input pin
6	GND	Low-noise ground
7	VREF	Reference voltage output pin
8	DTC1	Maximum duty and soft start adjustment pin (Channel 1)
9	DTC2	Maximum duty and soft start adjustment pin (Channel 2)
10	INV2	Error amplifier negative input pin (Channel 2)
11	FB2	Error amplifier output pin (Channel 2)
12	CTL1	Enable/stand-by control input (Channel 1)
13	CTL2	Enable/stand-by control input (Channel 2)
14	VCC	Main power supply pin
15	SYNC	Synchronous rectification timing adjustable pin
16	PGND	Power ground (connected low-side gate driver and digital ground)
17	OUT2L	Low-side (synchronous rectifier) gate driver output pin (Channel 2)
18	VREGA	Connected capacitor for internal regulator
19	SCP	Delay time of short circuit protection adjustment pin connected capacitor
20	VS2	Over current detection voltage monitor pin (connected FET drain, Channel 2)
21	CL2	Over current detection voltage adjustment pin connected capacitor and resistor (Channel 2)
22	PVCC2	High-side gate driver power supply input (Channel 2)
23	OUT2H	High-side gate driver output pin (Channel 2)
24	VREGB	Connected capacitor for internal regulator
25	OUT1	High-side gate driver output pin (Channel 1)
26	PVCC1	High-side gate driver power supply input (Channel 1)
27	CL1	Over current detection voltage adjustment pin connected capacitor and resistor (Channel 1)
28	VS1	Over current detection voltage monitor pin (connected FET drain, Channel 1)

○Operation Notes

1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC deterioration or damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2) GND potential

Ensure a minimum GND pin potential in all operating conditions. In addition, ensure that no pins other than the GND pin carry a voltage lower than or equal to the GND pin, including during actual transient phenomena.

3) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4) Inter-pin shorts and mounting errors

Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pin caused by the presence of a foreign object may result in damage to the IC.

5) Operation in a strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

6) Thermal shutdown circuit (TSD circuit)

This IC incorporates a built-in thermal shutdown circuit (TSD circuit). The TSD circuit is designed only to shut the IC off to prevent runaway thermal operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of the thermal shutdown circuit is assumed.

7) Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.

8) Common impedance

Power supply and ground wiring should reflect consideration of the need to lower common impedance and minimize ripple as much as possible (by making wiring as short and thick as possible or rejecting ripple by incorporating inductance and capacitance).

9) Applications with modes that reverse VCC and pin potentials may cause damage to internal IC circuits.

For example, such damage might occur when VCC is shorted with the GND pin while an external capacitor is charged. It is recommended to insert a diode for preventing back current flow in series with VCC or bypass diodes between VCC and each pin.

10) Timing resistor and capacitor

Timing resistor(capacitor) connected between RT(CT) and GND, has to be placed near RT(CT) terminal 3pin(4pin). And pattern has to be short enough.

11) The Dead time input voltage has to be set more than 1.1V. Also, the resistance between DTC and VREF is used more than 30kΩ to work OCP function reliably.

12) The energy on DTC1 (8pin) and DTC2 (9pin) is discharged when CTL1 (12pin) and CTL2 (13pin) are OFF, respectively, or VCC (14pin) is OFF (UVLO activation). However, it is considerable to occur overshoot when CTL and VCC are turned on with remaining more than 1V on the DTC.

13) If Gate capacitance of P-channel MOSFET or resistance placed on

Gate is large, and the time from beginning of Gate switching to the end of Drain's (tsw), is long, it may not start up due to the OCP malfunction.

To avoid it, select MOSFET or adjust resistance as tsw becomes less than 270nsec.

14) In Synchronous Recification, insert $R_{FB2\text{-}GND}$ ($R_{FB2\text{-}GND} \fallingdotseq 3 \times R_{sync}$) between FB2 and GND, because it is possible to reduce overshoot

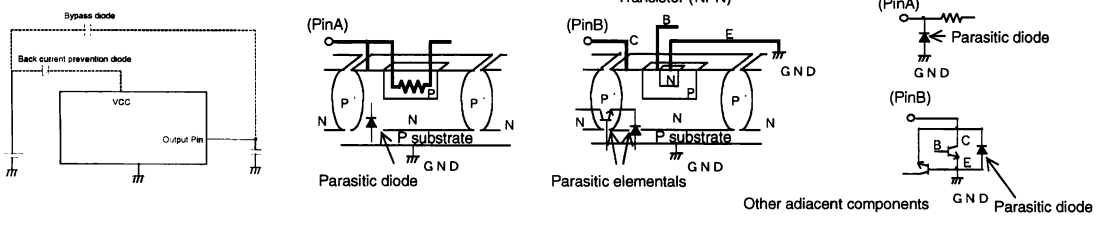
(In Without Synchronous Rectification, don't insert $R_{FB2\text{-}GND}$).

15) IC pin input

This monolithic IC contains P+ isolation and PCB layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements. For example, when a resistor and transistor are connected to pins as shown in following chart,

- O the P/N junction functions as a parasitic diode when GND > (Pin A) for the resistor or GND > (Pin B) for the transistor (NPN).
- O Similarly, when GND > (Pin B) for the transistor (NPN), the parasitic diode described above combines with the N layer of other adjacent elements to operate as a parasitic NPN transistor.

The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as by the application of voltages lower than the GND (PCB) voltage to input and output pins.



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