Complementary Power Transistors

DPAK For Surface Mount Applications

NPN
MJD41C*
PNP
MJD42C*

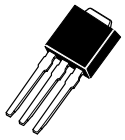
*ON Semiconductor Preferred Device

SILICON
POWER TRANSISTORS
6 AMPERES
100 VOLTS
20 WATTS

Designed for general purpose amplifier and low speed switching applications.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("–1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel ("T4" Suffix)
- Electrically Similar to Popular TIP41 and TIP42 Series
- Monolithic Construction With Built–in Base–Emitter Resistors

CASE 369A–13



CASE 369–07

MAXIMUM RATINGS

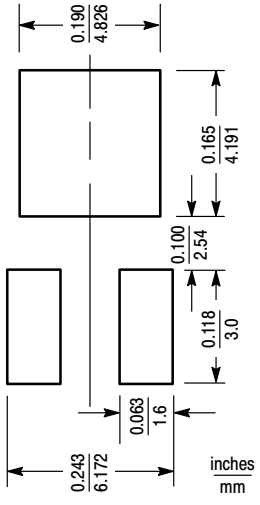
Rating	Symbol	MJD41C MJD42C	Unit
Collector–Emitter Voltage	V_{CEO}	100	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Emitter–Base Voltage	V_{EB}	5	Vdc
Collector Current — Continuous Peak	I_C	6 10	Adc
Base Current	I_B	2	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Total Power Dissipation* @ T_A = 25°C Derate above 25°C	P_D	1.75 0.014	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction to Ambient*	$R_{\theta JA}$	71.4	°C/W

*These ratings are applicable when surface mounted on the minimum pad size recommended.

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0)	I_{CEO}	—	50	μAdc
Collector Cutoff Current (V_{CE} = 100 Vdc, V_{EB} = 0)	I_{CES}	—	10	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	—	0.5	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 4 Vdc) (I_C = 3 Adc, V_{CE} = 4 Vdc)	h_{FE}	 30 15	 — 75	—
Collector–Emitter Saturation Voltage (I_C = 6 Adc, I_B = 600 mAdc)	$V_{CE(sat)}$	—	1.5	Vdc
Base–Emitter On Voltage (I_C = 6 Adc, V_{CE} = 4 Vdc)	$V_{BE(on)}$	—	2	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)	f_T	3	—	MHz
Small–Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 kHz)	h_{fe}	20	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) $f_T = |h_{fe}| \bullet f_{test}$.

TYPICAL CHARACTERISTICS

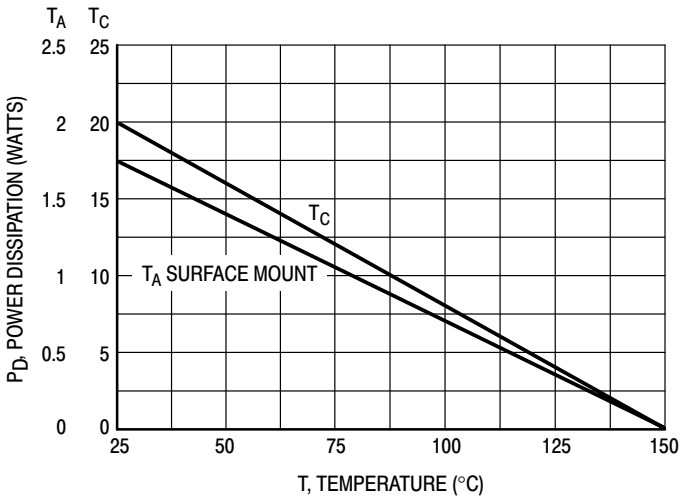


Figure 1. Power Derating

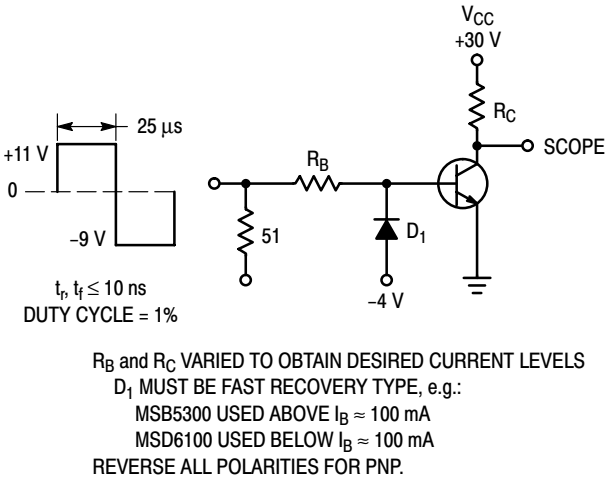


Figure 2. Switching Time Test Circuit

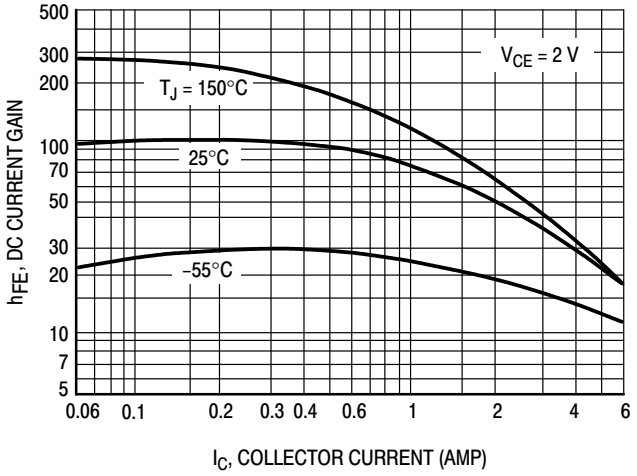


Figure 3. DC Current Gain

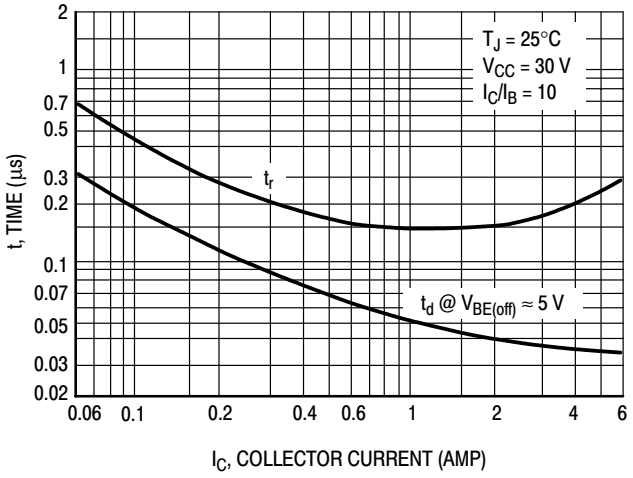


Figure 4. Turn−On Time

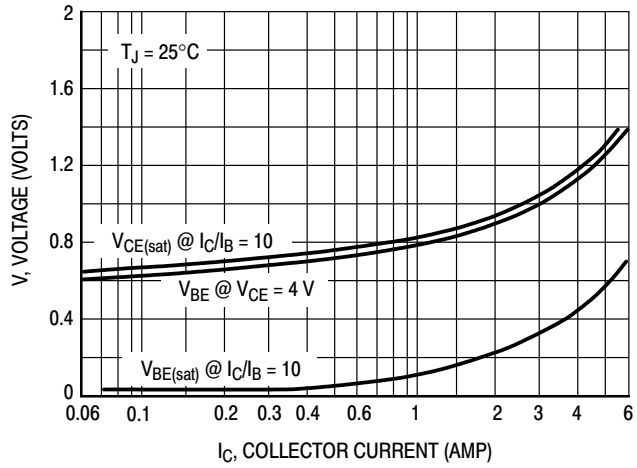


Figure 5. “On” Voltages

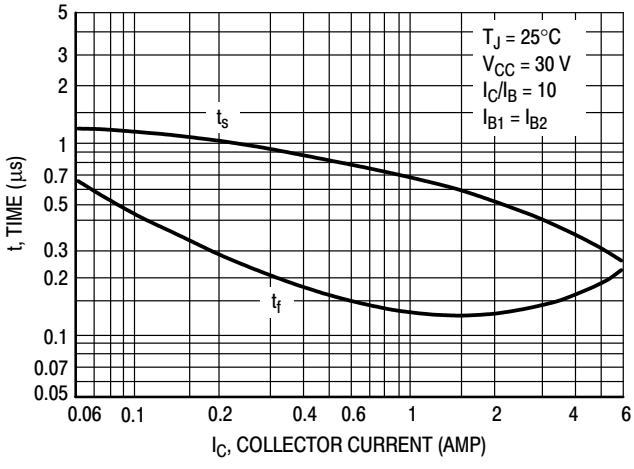


Figure 6. Turn−Off Time

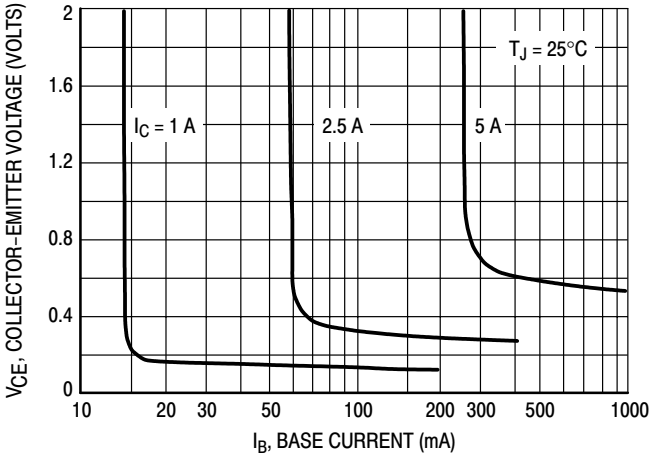


Figure 7. Collector Saturation Region

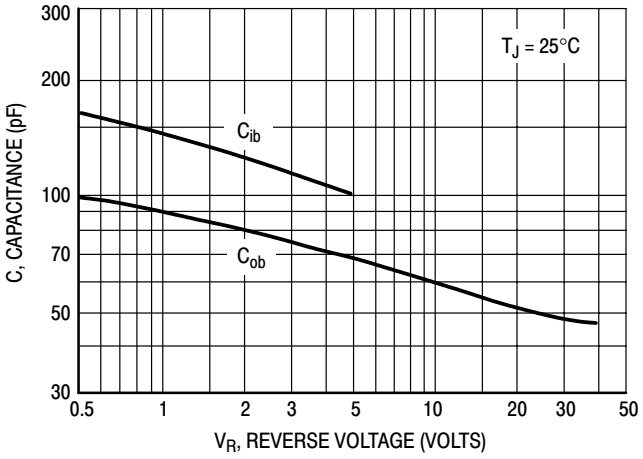


Figure 8. Capacitance

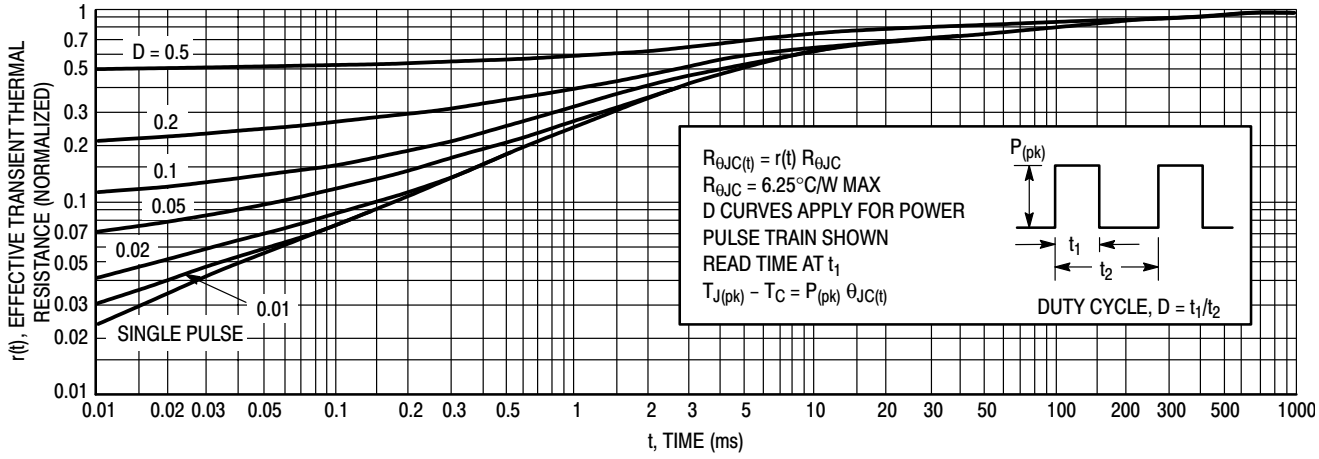


Figure 9. Thermal Response

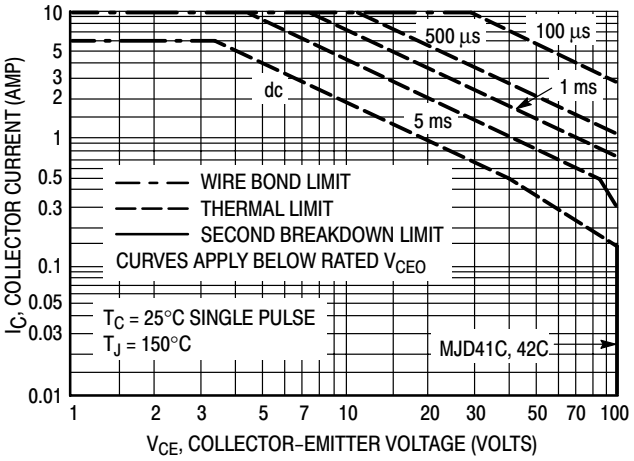


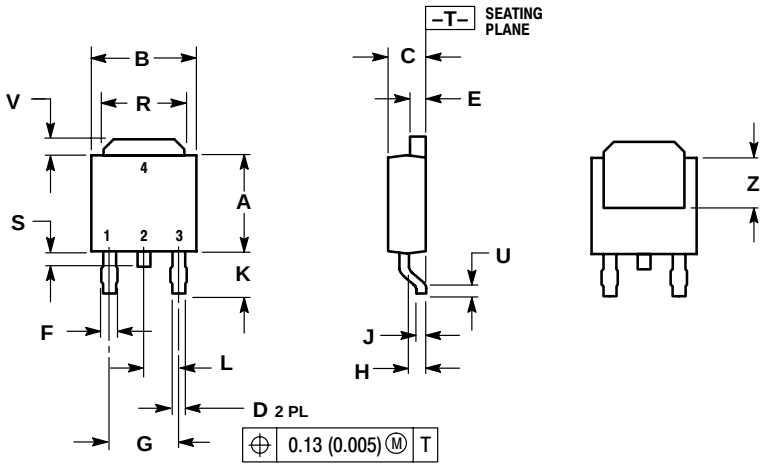
Figure 10. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 9. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

PACKAGE DIMENSIONS

DPAK
CASE 369A–13
ISSUE AA

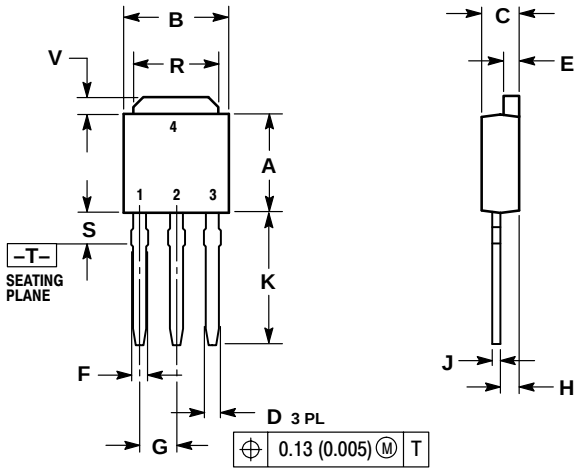


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020	---	0.51	---
V	0.030	0.050	0.77	1.27
Z	0.138	---	3.51	---

PACKAGE DIMENSIONS

DPAK
CASE 369–07
ISSUE M



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.175	0.215	4.45	5.46
S	0.050	0.090	1.27	2.28
V	0.030	0.050	0.77	1.27

Notes

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

N. American Technical Support: 800–282–9855 Toll Free USA/Canada

JAPAN: ON Semiconductor, Japan Customer Focus Center
4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–0031
Phone: 81–3–5740–2700
Email: r14525@onsemi.com

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local
Sales Representative.