

STRUCTURE Silicon Monolithic Integrated Circuit

PRODUCT NAME Main Power Supply For TFT-LCD Display Module

TYPE **BD8160EFV**

PACKAGE Fig.1 HTSSOP-B28 (Plastic mold)

BLOCK DIAGRAM Fig.2

FEATURE Boost and Buck DC/DC converter  
Built-in +/- charge pump driver

● ABSOLUTE MAXIMUM RATING (Ta=25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage	SUP, VIN	20	V
Power Dissipation	Pd	1450*	mW
Operating Temperature Range	Topr	-40~+85	°C
Storage Temperature Range	Tstg	-55~+150	°C
Junction Temperature	Tjmax	150	°C
SW Voltage	VSW	21	V
SWB Voltage	VSWB	19	V
EN1, EN2, FREQ Voltage	VEN1, VEN2, VFREQ	19	V

\* Derating is done 11.6mW/°C for operating above Ta≥25°C (On 70.0mm×70.0mm×1.6mm board)

● OPERATION RANGE (Ta=-40~85°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	SUP, VIN	8	12	18	V
Vs Voltage	Vs	VIN+2	15	18	V
Switch current for SW	ISW	—	—	2.6**	A
Switch current for SWB	ISWB	—	—	2.0**	A
EN1, EN2, FREQ Voltage	VEN1, VEN2, VFREQ	—	—	18	V

\*\* Pd, ASO should not be exceeded

Status of this document

The English version of this document is the formal specification.

A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document, formal version takes priority.

● Electrical characteristics (unless otherwise specified VIN=12V and Ta=25°C)

1. DC/DC converter controller block

PARAMETER	SYMBOL	LIMITS			UNIT	CONDITIONS
		MIN	TYP	MAX		
<b>Soft start – SS</b>						
SS source current	I <sub>SS</sub>	6	10	14	μA	V <sub>SS</sub> =0.5V
<b>Error amplifier block – FB and FBB</b>						
FB and FBB input bias current	I <sub>FB12</sub>	-	0.1	2	μA	
Feedback voltage for boost converter	V <sub>FB</sub>	1.150	1.162	1.174	V	Voltage follower
Feedback voltage for buck converter	V <sub>FBB</sub>	1.188	1.213	1.238	V	
<b>SW block – SW</b>						
On resistance N-channel	R <sub>ONN</sub>	-	0.2	0.3	Ω	I <sub>O</sub> =0.8A
Leak current N-channel	I <sub>LEAKN1</sub>	-	0	10	μA	V <sub>SW</sub> =18V
Maximum duty cycle	M <sub>DUTY</sub>	75	90	97	%	FB= 0V
<b>SW block – SWB</b>						
Leak current N-channel	I <sub>LEAKN2</sub>	-	0	10	μA	V <sub>INB</sub> =18V , V <sub>SWB</sub> =0V
<b>Protections</b>						
Over Voltage Protection for SW	V <sub>SWOVP</sub>	18.5	19	19.5	V	

2. Charge pump driver block

PARAMETER	SYMBOL	LIMITS			UNIT	CONDITIONS
		MIN	TYP	MAX		
<b>Error amplifier block – FBP and FBN</b>						
FBP, FBN input bias current	I <sub>FBP, FBN</sub>	-	0.1	1	μA	
Feedback voltage for VGH	V <sub>FBP</sub>	1.188	1.213	1.238	V	
Feedback voltage for VGL	V <sub>FBN</sub>	0.18	0.2	0.22	V	
<b>Delay start block</b>						
DLY1, DLY2 source current	I <sub>DLY1, DLY2</sub>	2	5	9	μA	V <sub>DLY</sub> =0.5V

3. General

PARAMETER	SYMBOL	LIMITS			UNIT	CONDITIONS
		MIN	TYP	MAX		
<b>Supply current</b>						
Average supply current	I <sub>CC</sub>	-	5	8	mA	
<b>Oscillator</b>						
Oscillation frequency1	F <sub>OSC1</sub>	600	750	900	kHz	FREQ = High
Oscillation frequency2	F <sub>OSC2</sub>	400	500	600	kHz	FREQ = Low
<b>Protections</b>						
Under voltage lockout threshold1	V <sub>UML01</sub>	6.9	7.4	7.9	V	V <sub>IN</sub> rising
Under voltage lockout threshold2	V <sub>UML02</sub>	6.5	7.0	7.5	V	V <sub>IN</sub> falling
<b>Reference Voltage</b>						
Reference Voltage	V <sub>REF</sub>	1.188	1.213	1.238	V	
<b>Gate Drive</b>						
Gate drive threshold	V <sub>GD</sub>	0.985	1.065	1.145	V	
GD output low voltage	V <sub>OL</sub>	-	0.7	1.4	V	I = 1mA
GD output leakage current	I <sub>LK</sub>	-	0	10	μA	
<b>Logic signals EN1, EN2, FREQ</b>						
High level input voltage	V <sub>IH</sub>	2.0	-	-	V	
Low level input voltage	V <sub>IL</sub>	-	-	0.8	V	

This product is not designed for protection against radioactive rays.

### ● PHYSICAL DIMENSION

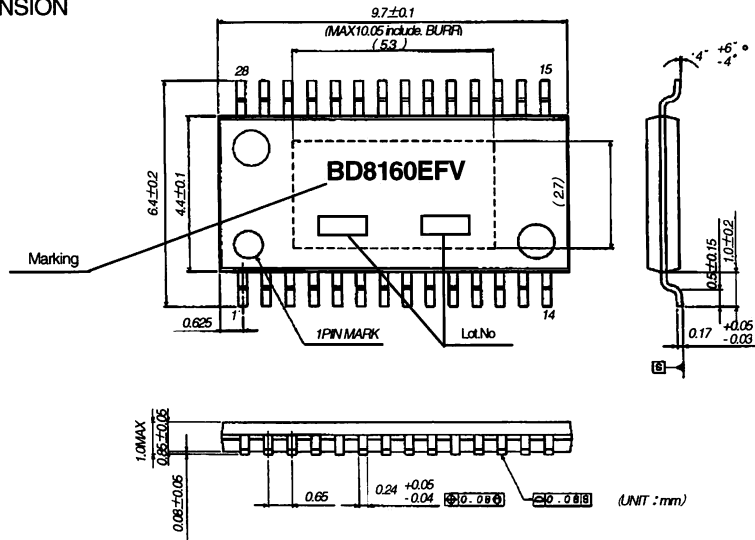
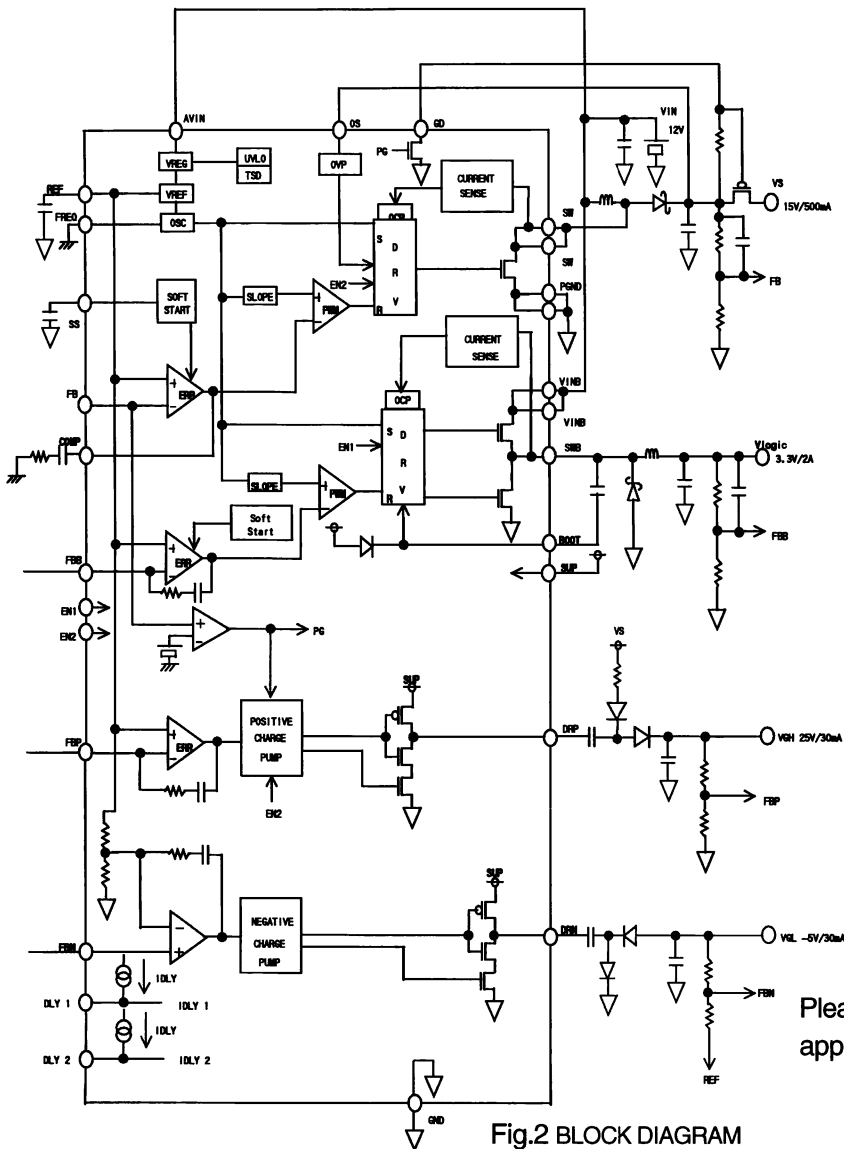


Fig.1 PHYSICAL DIMENSION (PLASTIC MOLD) (UNIT: mm)

### ● BLOCK DIAGRAM



PIN NO.	PIN NAME	PIN NO.	PIN NAME
1	FB	15	FBB
2	COMP	16	EN1
3	OS	17	BOOT
4	SW	18	SWB
5	SW	19	N.C.
6	PGND	20	VINB
7	PGND	21	VINB
8	SUP	22	AVIN
9	EN2	23	GND
10	DRP	24	REF
11	DRN	25	DLY1
12	FREQ	26	DLY2
13	FBN	27	GD
14	FBP	28	SS

Please refer to Technical note concerning application circuit, etc.

Fig.2 BLOCK DIAGRAM

● OPERATION NOTES

1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2) GND potential

Ensure a minimum GND pin potential in all operating conditions.

3) Setting of heat

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4) Pin short and mistake fitting

Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pins caused by the presence of a foreign object may result in damage to the IC.

5) Actions in strong magnetic field

Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.

6) Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.

7) Ground wiring patterns

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring patterns of any external components.

8) Regarding input pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements.

For example, when the resistors and transistors are connected to the pins as shown in Fig. , a parasitic diode or a transistor operates by inverting the pin voltage and GND voltage.

The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements such as by the application of voltages lower than the GND (P substrate) voltage to input and output pins.

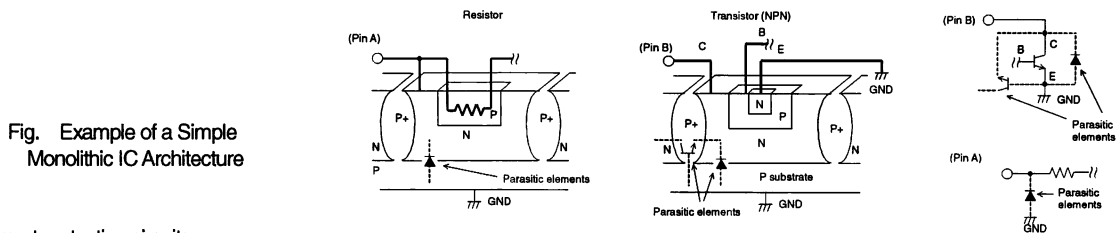


Fig. Example of a Simple Monolithic IC Architecture

9) Overcurrent protection circuits

An overcurrent protection circuit designed according to the output current is incorporated for the prevention of IC damage that may result in the event of load shorting. This protection circuit is effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits. At the time of thermal designing, keep in mind that the current capacity has negative characteristics to temperatures.

10) Thermal shutdown circuit (TSD)

This IC incorporates a built-in TSD circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power dissipation limits, the attendant rise in the chip's junction temperature  $T_J$  will trigger the TSD circuit to turn off all output power elements. Operation of the TSD circuit presumes that the IC's absolute maximum ratings have been exceeded. Application designs should never make use of the TSD circuit.

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