MOSPEC

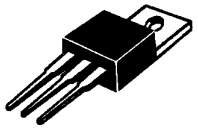
NPN SILICON POWER TRANSISTORS

...designed for the output stage of 25W to 35W AF power amplifier

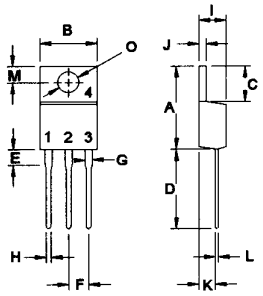
FEATURES:
* Low Collector-Emitter Saturation Voltage
  $V_{CE(sat)}$= 2.0V(Max) @I_C=4.0A,I_B=0.4A
* DC Current Gain
  hFE= 40-320@I_C= 1.0A
* Complementary to NPN 2SB633

NPN
2SD613

6 AMPERE
POWER
TRANASISTORS
85 VOLTS
40 WATTS



TO-220



PIN 1.BASE
2.COLLECTOR
3.EMITTER
4.COLLECTOR(CASE)

DIM	MILLIMETERS	
	MIN	MAX
A	14.68	15.31
B	9.78	10.42
C	5.01	6.52
D	13.06	14.62
E	3.57	4.07
F	2.42	3.66
G	1.12	1.36
H	0.72	0.96
I	4.22	4.98
J	1.14	1.38
K	2.20	2.97
L	0.33	0.55
M	2.48	2.98
O	3.70	3.90

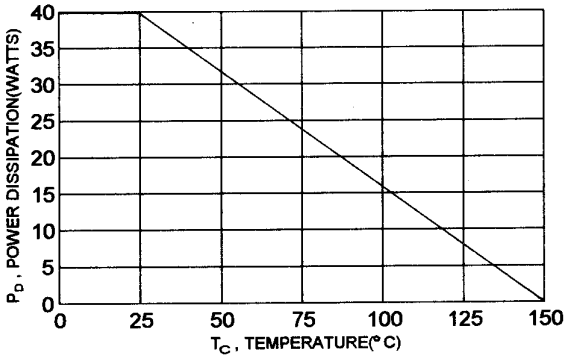
MAXIMUM RATINGS

Characteristic	Symbol	2SD613	Unit
Collector-Emitter Voltage	V_{CEO}	85	V
Collector-Base Voltage	V_{CBO}	100	V
Emitter-Base Voltage	V_{EBO}	6.0	V
Collector Current - Continuous - Peak	I_C I_{CM}	6.0 10	A
Base current	I_B	3.0	A
Total Power Dissipation @T_C = 25°C Derate above 25°C	P_D	40 0.32	W W/°C
Operating and Storage Junction Temperature Range	T_J , T_{STG}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction to Case	Rθjc	3.125	°C/W

FIGURE -1 POWER DERATING



ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

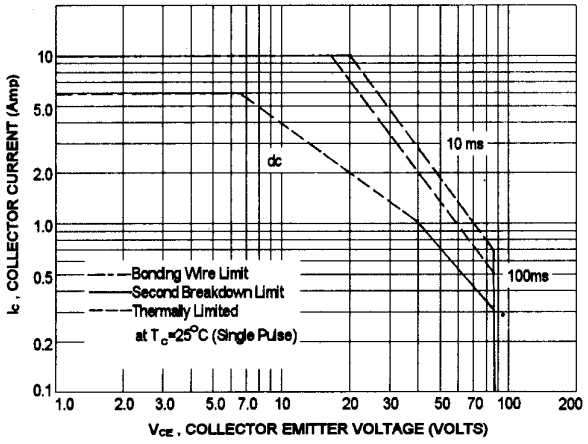
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C= 50 mA, I_B= 0)	$V_{(BR)CEO}$	85		V
Collector-Base Breakdown Voltage (I_C= 5.0 mA, I_E= 0)	$V_{(BR)CBO}$	100		V
Emitter-Base Breakdown Voltage (I_E= 5.0 mA, I_C= 0)	$V_{(BR)EBO}$	6.0		V
Collector Cutoff Current (V_{CB}= 40 V, I_E= 0)	I_{CBO}		100	uA
Emitter Cutoff Current (V_{EB}= 4.0 V, I_C= 0)	I_{EBO}		100	uA
ON CHARACTERISTICS (1)				
DC Current Gain (I_C= 1.0 A, V_{CE}= 5.0 V) * (I_C= 3.0 A, V_{CE}= 5.0 V)	hFE(2) hFE	40 20	320	
Collector-Emitter Saturation Voltage (I_C= 4.0 A, I_B= 400 mA)	$V_{CE(sat)}$		2.0	V
Base-Emitter On Voltage (I_C= 1.0 A, V_{CE}=5.0 V)	$V_{BE(on)}$		1.5	V
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product (I_C = 1.0 A, V_{CE} = 5.0 V, f = 1.0 MHz)	f_T	5.0		MHz

(1) Pulse Test: Pulse Width =300 us, Duty Cycle ≦ 2.0%

* hFE(2) Classification :

40	C	80	60	D	120	100	E	200	160	F	320

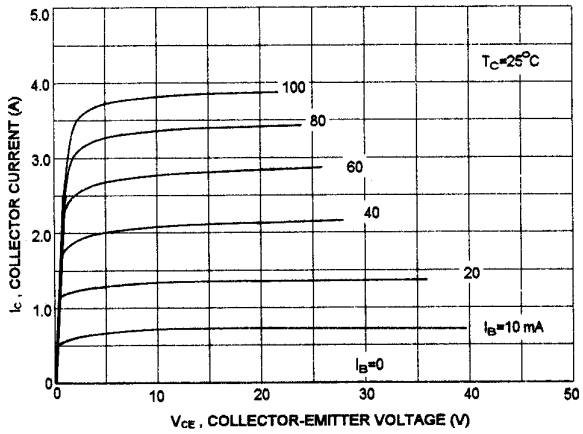
ACTIVE-REGION SAFE OPERATING AREA (SOA)



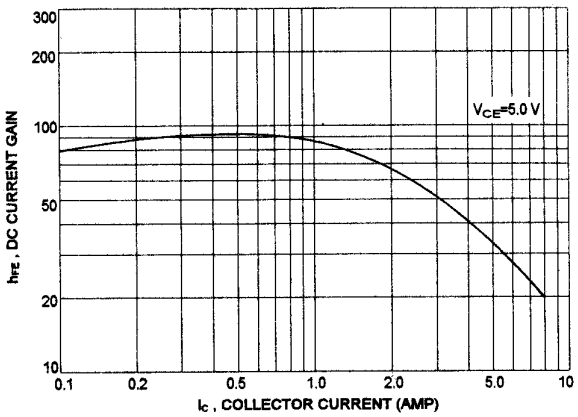
There are two limitation on the power handling ability of a transistor:average junction temperature and second breakdown safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than curves indicate.

The data of SOA is base on $T_{J(PK)}$=150 °C;T_C is variable depending on conditions.second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(PK)}$≤150°C, At high case temperatures, thermal limita tion will reduce the power that can be handled to value less than the limi-tations imposed by second breakdown.

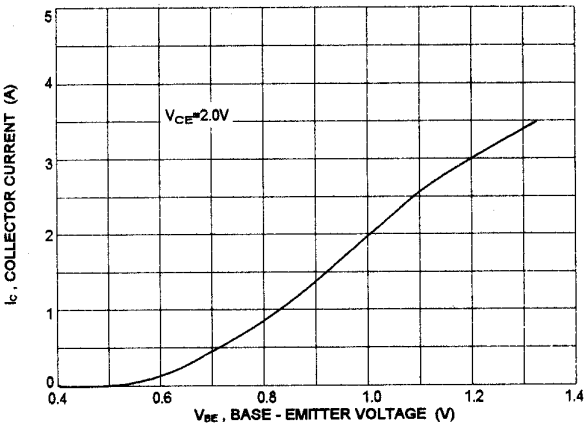
Ic - Vce



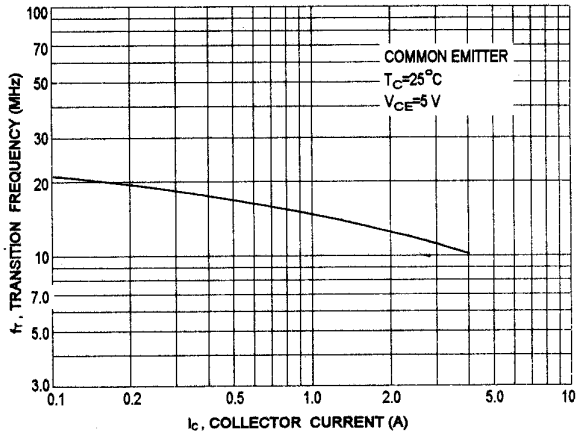
DC CURRENT GAIN



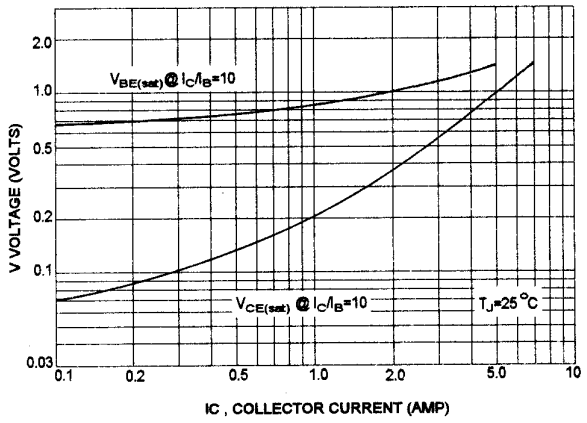
Ic - Vbe



f_T - Ic



"ON" VOLTAGES



CAPACITANCES