PCS CDMA Upconverter/Driver 1710 - 1910 MHz

V 200

MD59-0062

Features

- Highly integrated upconverter and driver
- Operates with supply voltages from 2.7 V to 5 V
- +7 dBm output power at 56 dBc ACPR
- Low current mode for power saving at low output power
- Balanced IF input (265 ohms)
- Low LO drive level, -10 dBm
- Operates in the US and Korean PCS bands
- Miniature 4-mm plastic FQFP-N package

Description

M/A-COM's MD59-0062 is a fully integrated upconverter / driver IC that includes an IF amplifier, upconverting mixer, two stage driver amplifier and LO buffer in a miniature 4 mm plastic FQFP-N package.

The MD59-0062 is ideally suited for CDMA handset transmitters that require high linearity and low power consumption.

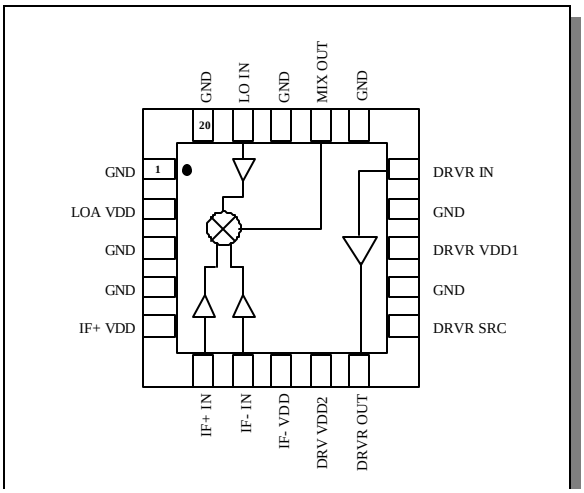
M/A-COM fabricates the MD59-0062 using an 0.5 micron low noise GaAs MESFET process. The process features full passivation for performance and reliability.

Absolute Maximum Ratings [1]

Parameter	Absolute Maximum
VDD	6 Volts
IF Input Level	0 dBm
LO in Power	0 dBm
Operating Temperature	-55°C to +100°C
Storage Temperature	-65°C to +150°C

1. Exceeding any one or combination of these limits may cause per-

Functional Schematic



Pin Configuration

Pin No.	PIN Name	Description
1	GND	DC and RF Ground
2	LOA V_{DD}	LO amplifier supply voltage. Bypassing required.
3	GND	DC and RF Ground
4	GND	DC and RF Ground
5	IF+ V_{DD}	IF+ supply voltage. Off chip inductor and IF bypassing required.
6	IF+ IN	IF+ input port. Off chip matching elements required.
7	IF– IN	IF– input port. Off chip matching elements required.
8	IF- V_{DD}	IF- supply voltage. Off chip inductor and IF bypassing required.
9	DFVR V_{DD2}	Driver amplifier second stage supply votlage. Must be RF bypassed.
10	DRVR OUT	50 ohms output of driver amplifier
11	DRVR SRC	Source bias voltage of driver output stage. Requires RF bypassing and may be used to control output stage current.
12	GND	DC and RF Ground
13	DFVR V_{DD1}	Driver Amplifier first stage supply voltage. Must be RF bypass.
14	GND	DC and RF Ground
15	DRVR IN	50 ohms input to driver amplifier
16	GND	DC and RF Ground
17	MIX OUT	50 ohms output of mixer
18	GND	DC and RF Ground
19	LO IN	Local oscillator input (-10 to +5 dBm)
20	GND	DC and RF Ground

Electrical Specifications[1]: V_{dd} = 3.0V, T_a = 25°C

Parameter	Test Conditions	Units	Min	Typ	Max
Complete Upconverter[2]/High Power Mode					
Conversion Gain	V_{CTRL} = Logic High (V_{DD})	dB	23	25	27
CDMA Linear Output Power[3]	RF Frequency = 1710 - 1910 MHz	dBm		7	
Noise Figure	LO Frequency = 1580 - 1780 MHz			10	
I_{DD}	LO Power = -10 dBm	mA		66	
V_{SWR} (All Ports)	IF = 130 MHz			1.5:1	
IF Input Impedance		Ohms		265	
LO-to-RF Port Leakage		dBm		-18	
Complete Upconverter[2]/High Power Mode					
Conversion Gain	V_{CTRL} = Logic Low (0 Volts)	dB		22	
CDMA Linear Output Power	RF Frequency = 1710 - 1910 MHz	dBm		0	
Noise Figure	LO Frequency = 1580 - 1780 MHz	dB		10	
I_{DD}	LO Power = -10 dBm	mA		46	
V_{SWR} (All Ports)	IF = 130 MHz			1.5:1	
IF Input Impedance		Ohms		265	
LO-to-RF Port Leakage		dBm		-18	

1. All specifications are optimized for K_PCS.
2. Complete Upconverter/driver measurements taken with a surface mount SAW filter between mixer output and driver input.
3. CDMA linear power is defined as 56 dBc ACPR at a 1.228 MHz offset from the carrier frequency.

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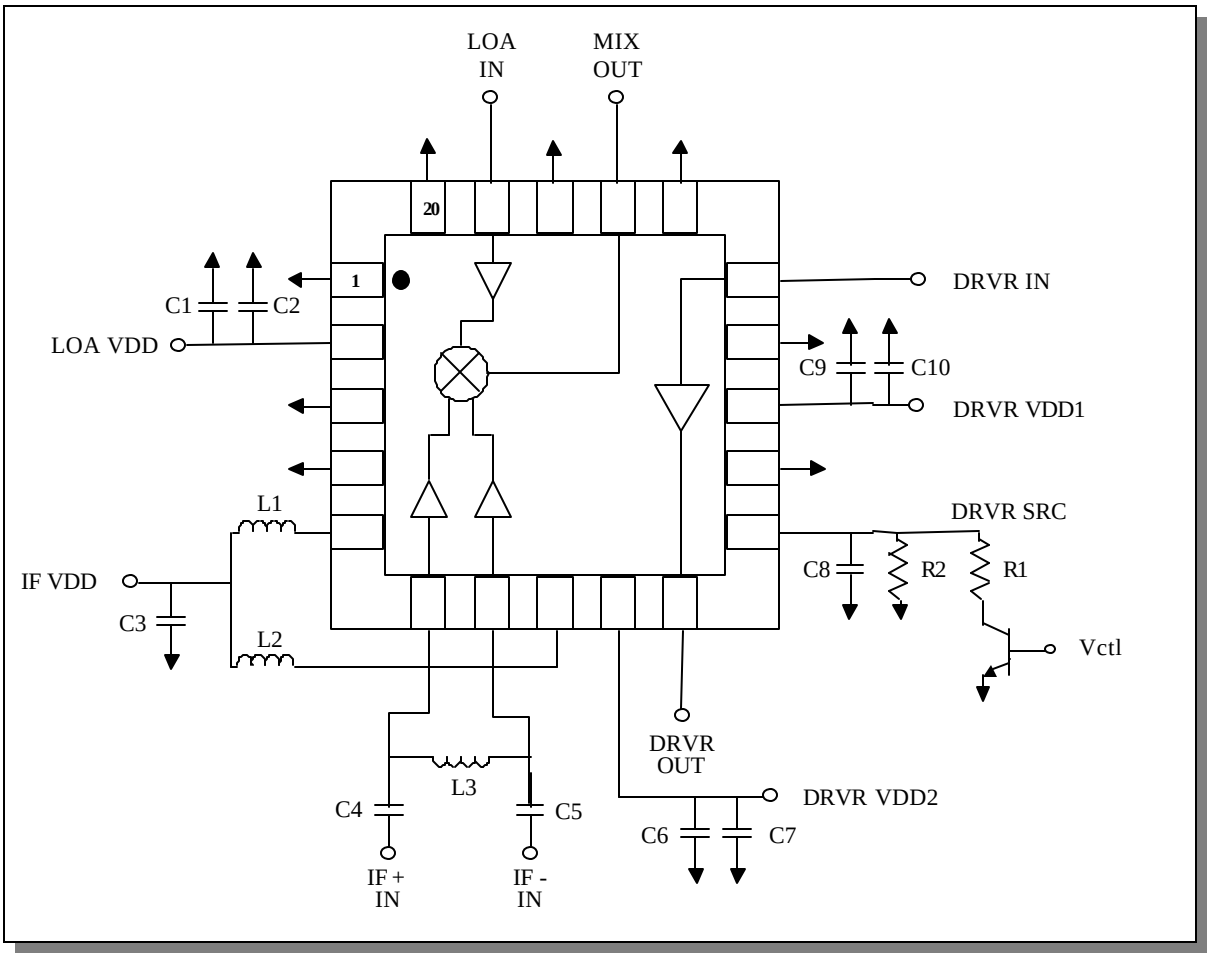
Sample Board Schematic



External Circuitry Parts List

Ref. Designation	Value	Purpose
C2, C6, C9	33 pF	RF bypass
C1, C3, C7, C10	1000 pF	RF/IF bypass
C4, C5	10 pF	IF matching
C8	10 pF	RF bypass
L3	270 nH	IF matching
L1, L2	82 nH	RF choke
R[1]	18 ohms	Adjustable source bias resistor
R[2]	68 ohms	Source bias resistor

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Operating Instructions

The MD59-0062 is a highly integrated MMIC upconverter / driver for the 1710 - 1910 MHz PCS band. The upconverter / driver provides exceptional RF performance while consuming low DC current and is packaged in a low cost plastic package. It is ideal for lightweight battery operated portable radio systems.

The transmit chain consists of a balanced IF amplifier, balanced mixer with single-ended RF output, and a two stage RF driver amplifier as shown in the block diagram. The user must add surface mount resistors, inductors and capacitors in conjunction with the IC to optimize the trade-offs among performance, tunability and ease of use. A schematic on page 4 shows the IC and required off-chip components.

An off-chip self-bias resistor R1 with an RF bypass capacitor allows the current in the driver amplifier to be varied to obtain the required linear output power. By placing a bipolar transistor in series with the self-bias resistor, you can dynamically switch the current draw in the driver to provide high and low power operating modes. In high power mode, the bipolar transistor is on and the driver output stage is self-biased through R1 to provide +7 dBm of linear output power. By switching off the bipolar transistor, the output stage is biased through the higher resistance R2 thus reducing the current by ~25 mA to give 0 dBm of linear output power.

An external filter is required between the mixer output and driver amplifier input to reduce the amplitude of the image and local oscillator signals coming out of the mixer. This filter should have a 50 Ω input and output impedance.

The mixer is a balanced resistive FET mixer that provides exceptional linearity and isolation with low loss and no DC current.

The IFA input ports are externally matched to 265 ohm differential impedance using two off-chip capacitors and an off chip inductor. This allows maximum flexibility of intermediate frequency and IF filter. The IFA output ports are matched to the mixer using off chip inductors, which are also used for DC bias injection. A matching network such as that shown below can be used to match both the input and output of the IFA at the required frequency. The inductor also acts as a choke for the DC supply line.

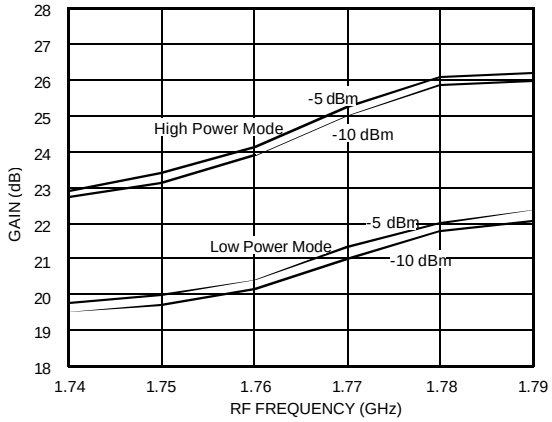
The LO input port is matched on-chip to 50 ohms. An LO buffer amplifier boosts the -10 dBm input signal to the level required to drive the mixer. The converter reaches optimum performance with a drive level of -5 dBm.

All DC supply lines must be properly bypassed at RF frequencies to obtain optimum performance and at lower frequency to maintain unconditional stability. Capacitors C1, C3, C8 are RF bypass capacitors for the LO amplifier and the driver amplifier. The value and placement of these capacitors is critical in determining the frequency response of these amplifiers. Capacitor C10 is a source bypass capacitor for the second stage of the driver amplifier. The placement of this capacitor will affect the gain of the amplifier. For best performance, place all the RF bypass capacitors as shown in the PCB drawing on the previous page. Capacitors C2, C4, C5 and C9 are 1000 pF low frequency DC supply bypass capacitors. Their values and placement are less critical than the other capacitors. However, for best results, place these capacitor as close to the package leads as possible.

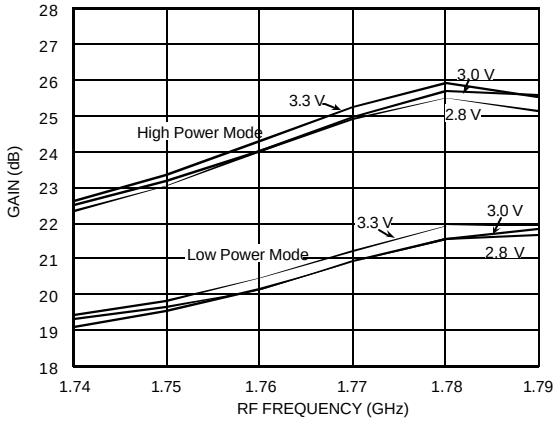
Typical Performance Curves

Korean PCS Band

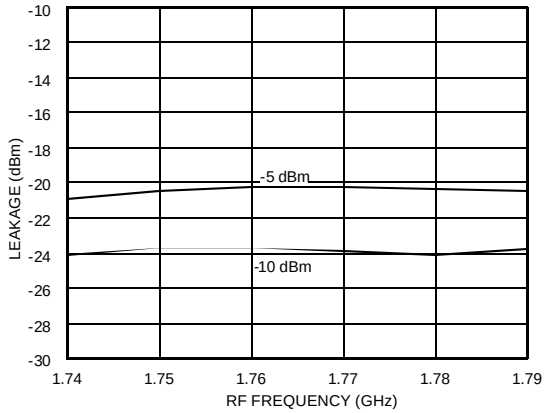
Conversion Gain vs. Frequency
LO = 10 dBm, -5 dBm, V_{DD} = 3.0V



Conversion Gain vs. Frequency
V_{DD} = 2.8V, 3.0V, 3.3V, LO = 10 dBm

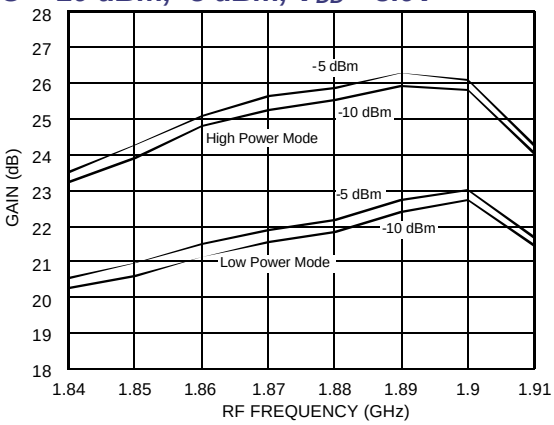


LO-to-RF Leakage vs. Frequency
LO = 10 dBm, -5 dBm, V_{DD} = 3.0V

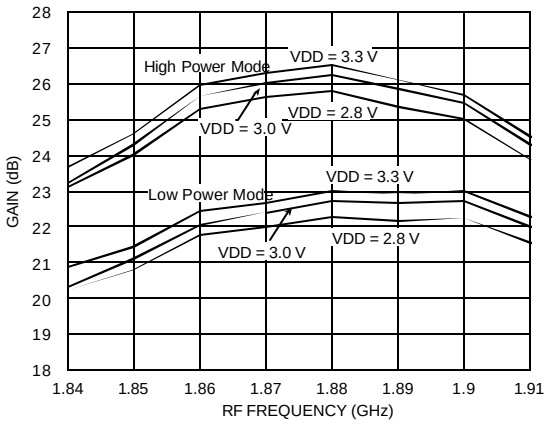


US PCS Band

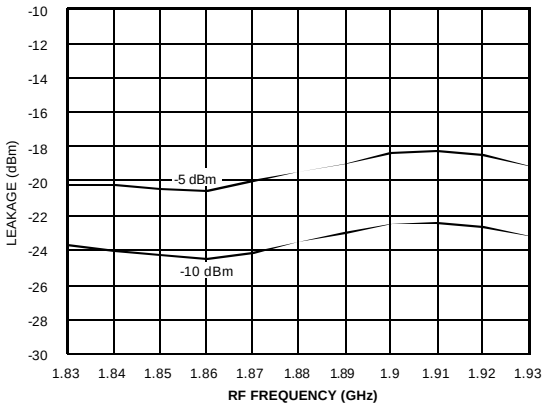
Conversion Gain vs. Frequency
LO = 10 dBm, -5 dBm, V_{DD} = 3.0V



Conversion Gain vs. Frequency
V_{DD} = 2.8V, 3.0V, 3.3V, LO = 10 dBm



LO-to-RF Leakage vs. Frequency
LO = 10 dBm, -5 dBm, V_{DD} = 3.0V



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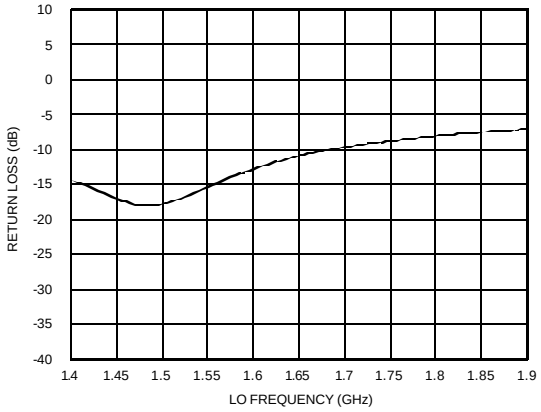
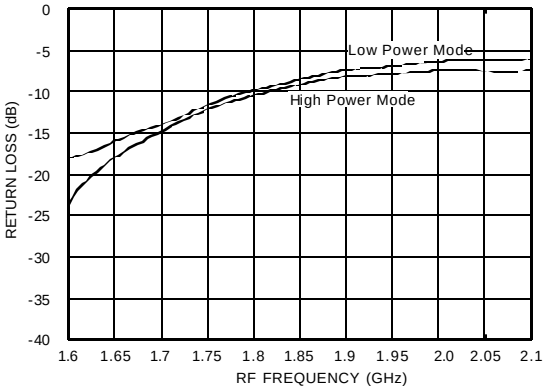
Typical Performance Curves (Cont'd)

Korean PCS Band

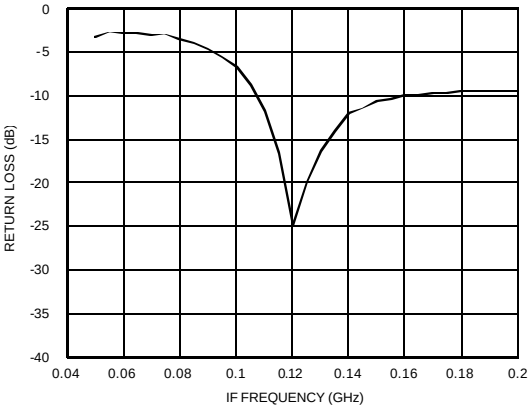
LO Input Return Loss vs. Frequency
LO = 10 dBm, V_{DD} = 3.0V



Driver Output Return Loss vs. Frequency
High and Low Power Mode, V_{DD} = 3.0V

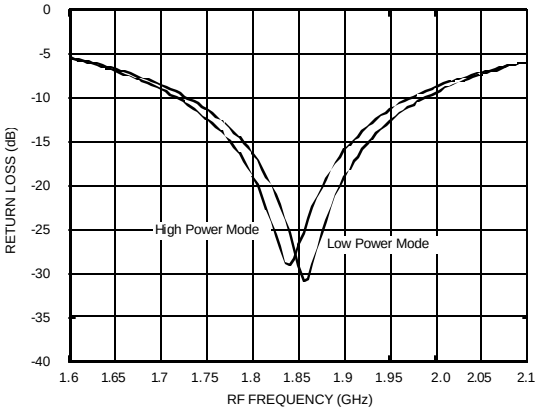


IF Input Return Loss vs. Frequency
LO = -5 dBm, V_{DD} = 3.0V

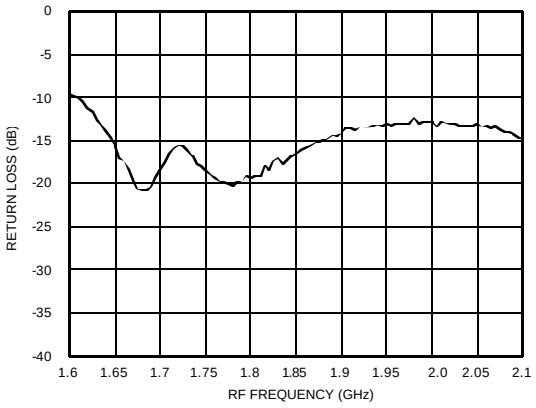


US PCS Band

LO Input Return Loss vs. Frequency
LO = 10 dBm, V_{DD} = 3.0V



Driver Output Return Loss vs. Frequency
High and Low Power Mode, V_{DD} = 3.0V



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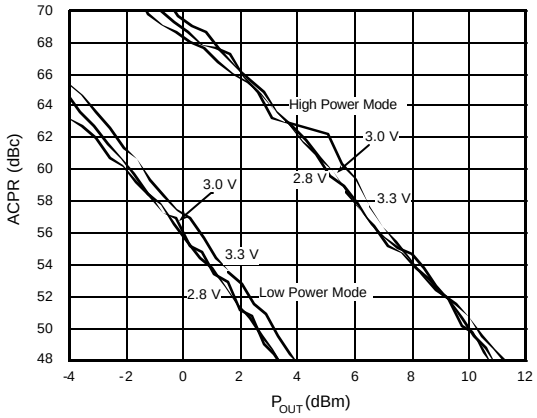
Typical Performance Curves (Cont'd)

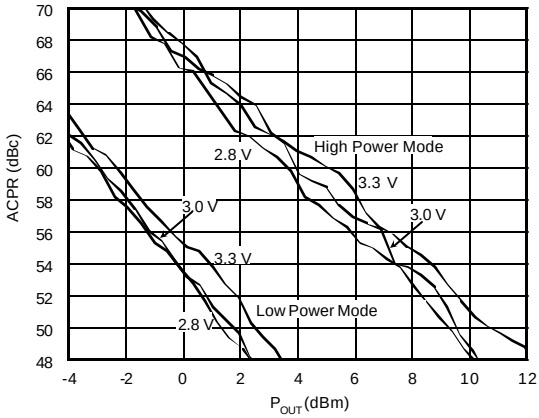
Korean PCS Band

ACPR vs. Output Power
F_{RF} = 1760 MHz
LO = -10 dBm, V_{DD} = 2.8 V, 3.0V, 3.3V

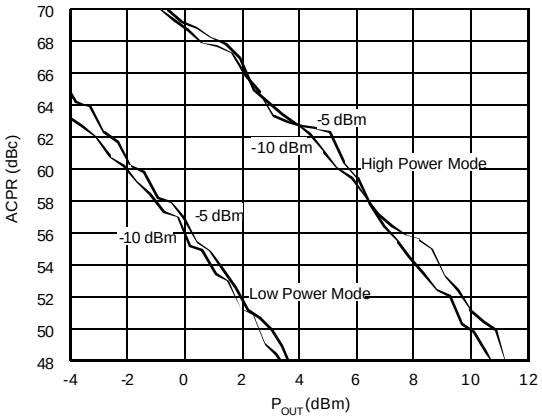


US PCS Band

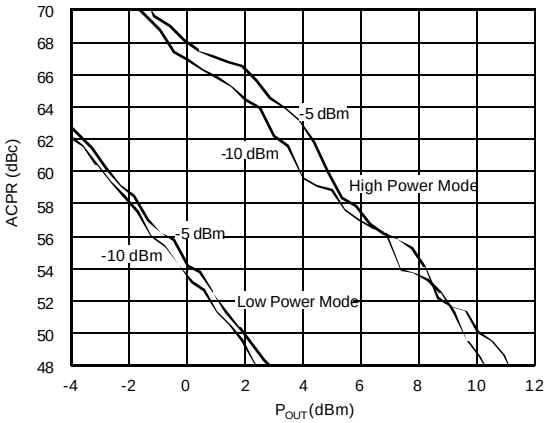
ACPR vs. Output Power
F_{RF} = 1760 MHz
LO = -10 dBm, V_{DD} = 2.8 V, 3.0V, 3.3V



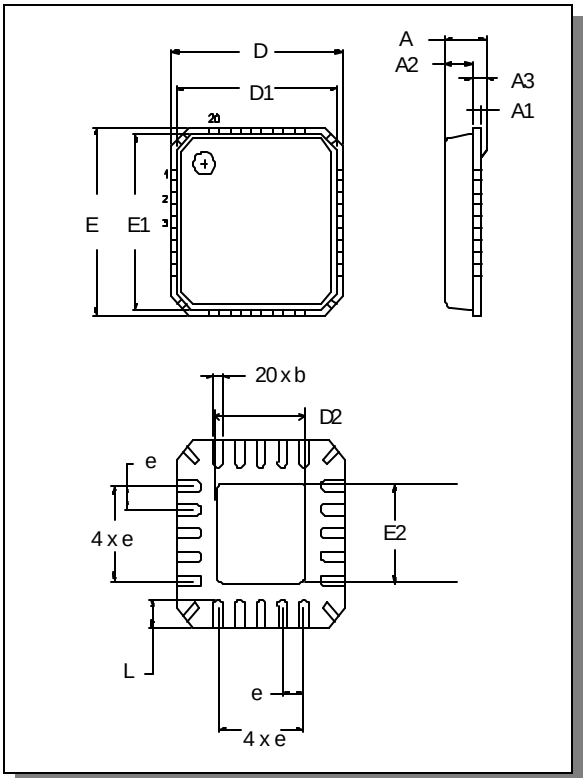
ACPR vs. Output Power
F_{RF} = 1760 MHz
LO = -10 dBm, -5 dBm, V_{DD} = 3.0V



ACPR vs. Output Power
F_{RF} = 1760 MHz
LO = -10 dBm, -5 dBm, V_{DD} = 3.0V



4 mm FQFP-N-20[1]



1. See JEDEC MO-220A VGGD-1 for additional dimensional and tolerance information.

4 mm FQFP-N-20

Dim.	Measurement (mm)		
	Min.	Nom.	Max.
A	0.80	0.90	1.00
A1	0	0.02	0.05
A2	0	0.65	1.00
A3		0.25 ref.	
b	0.18	0.23	0.30
D		4.00 basic	
D1		3.75 basic	
D2	0.75	1.70	2.25
e		0.50 basic	
E		4.00 basic	
E1		3.75 basic	
E2	0.75	1.70	2.25
L	0.35	0.55	0.75

Ordering Information

Part Number	Package
AM59-0062	4-mm Plastic FQFP-N Package
AM59-0062TR	Forward Tape and Reel[1]

1. If specific reel size is required, consult factory for part number assignment.