

Features

- Highly integrated upconverter / driver IC
- High linear output power with low current
- Variable gain control
- Low LO drive level, -10 dBm
- Single 3.0 V supply
- Miniature 4-mm plastic FQFP-N package
- CDMA, JCDMA + TDMA Applications

Description

M/A-COM's MD59-0054 is a fully integrated upconverter IC with a driver amplifier, a RF amplifier, a mixer, an IF amplifier and a LO buffer in a miniature 4-mm plastic FQFP-N package with exposed backside for improved high frequency grounding.

M/A-COM designed the MD59-0054 for use in applications with RF frequencies in the range of 800 – 900 MHz, including CDMA, JCDMA and TDMA wireless standards.. The device features balanced IF inputs and a single-ended RF output. The maximum conversion gain is 28 dB with a minimum 10 dB of gain range. The MD59-0054 is capable of producing +4 dBm of linear output power with an associated ACPR level of -56 dBc. The MD59-0054 includes a power-down mode to reduce current draw when it is powered but not in use. An internal LO buffer amplifier allows low LO input levels to the device.

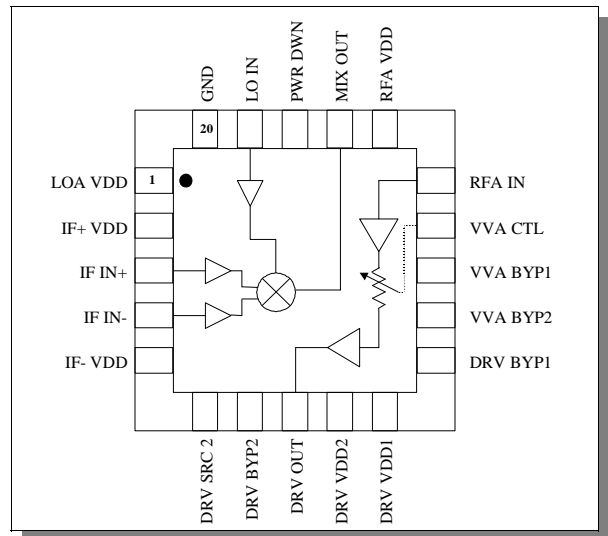
M/A-COM fabricates the MD59-0054 using an 0.5 micron low noise E/D GaAs MESFET process. The process features full passivation for performance and reliability.

Absolute Maximum Ratings ¹

Parameter	Absolute Maximum
VDD	6 Volts
IF Input Level	0 dBm
LO In Power	0 dBm
Operating Temperature	-55 °C to +100 °C
Storage Temperature	-65 °C to +150 °C

1. Exceeding any one or combination of these limits may cause permanent damage.

Functional Schematic



Pin Configuration

PIN No.	PIN Name	Description
1	LOA V _{DD}	LO amplifier supply voltage - Bypassing required.
2	IF+ V _{DD}	IF positive supply voltage. Off-chip inductor and IF bypassing required.
3	IF+ IN	IF plus input port. Off-chip matching elements required.
4	IF- IN	IF minus input port. Off-chip matching elements required.
5	IF- V _{DD}	IF negative supply voltage. Off-chip inductor and IF bypassing required.
6	DRV SRC2	Source bias voltage of driver output stage. Requires Driver output stage bias resistor which you can adjust to increase or decrease linear output power..
7	DRV BYP2	Driver second stage bypass cap.
8	DRV OUT	50 Ω output of driver amplifier
9	DRV V _{DD2}	Driver amplifier second stage supply voltage. RF bypassing required.
10	DRV V _{DD1}	Driver amplifier first stage supply voltage.
11	DRV BYP1	Driver first stage bypass cap.
12	VVA BP2	VVA bypass cap.
13	VVA BP1	VVA bypass cap
14	VVA CTL	VVA control voltage
15	RFA IN	50 Ω input to RF amplifier.
16	RFA V _{DD}	RF amplifier first stage supply voltage. RF bypassing required
17	MIX OUT	50 Ω output of mixer
18	PWR DWN	Power down control voltage
19	LO IN	Local oscillator (input -10 to +5 dBm), 50Ω
20	GND	DC and RF ground

Electrical Specifications: $V_{DD} = 3.0\text{ V}$, $T_A = +25\text{ }^\circ\text{C}$, VVA CTL = 2.7 V, PD = 2.7 V

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Cascaded Performance					
RF Frequency Range		MHz		824-849	
Conversion Gan	Frequency = 836 MHz	dB	25	28	32
Linear Output Power @ -56 dBc ACPR	Frequency = 836 MHz, $P_{IN} = -14\text{ dBm}$	dBm	+2.0	+4.0	
Gain Range	VVA CTL = 0.7 V \rightarrow 2.7 V		10	25	
Gain Variation vs. Frequency		dB	2		
Port Matches	All Ports	dB	10		
LO-to-Mixer Out Leakage		dBm	-15	-25	
LO-to-IF Isolation		dB	25	35	
Mixer Out to RFA In		dB	30	40	
I_{DD}		mA		50	
IF Input					
IF Frequency		MHz		130	
IF Input Level		dBm			-12
IF Impedance	Balanced	Ohms		265	
LO Input					
LO-to-RF Port Leakage		MHz		954-979	
LO Input Level		dBm	-12	-10	-5

1. Complete upconverter / driver measurements taken with a surface mount SAW filter between mixer output and driver input.
2. CDMA linear power is defined as 56 dBc ACPR at a 1.228 MHz offset from the carrier frequency

Specifications subject to change without notice.

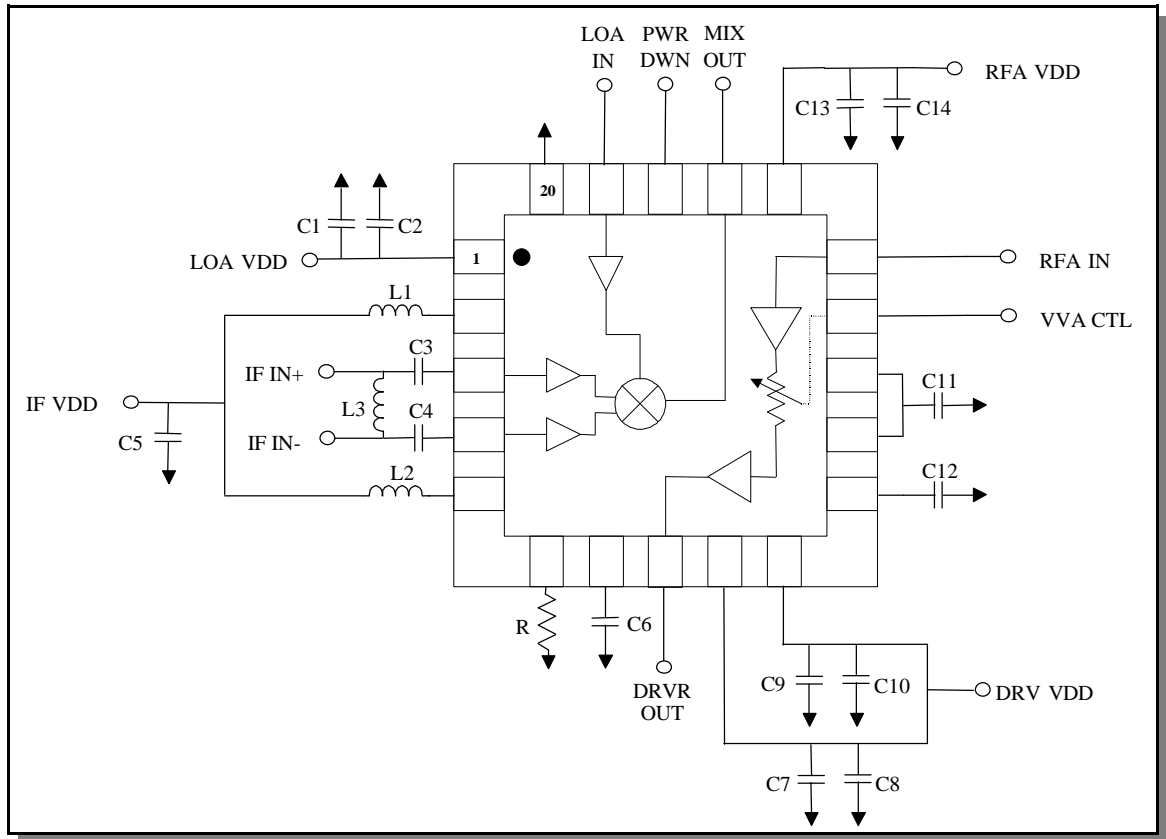
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- **Europe:** Tel. +44 (1344) 869 595, Fax+44 (1344) 300 020

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Sample Board Schematic



External Circuitry Parts List¹

Ref. Designation	Value	Purpose
C2,C6,C8,C10,C11,C14	47 pF	RF bypass
C1,C5,C7,C9,C13	1000 pF	RF/ IF bypass
C3,C4	68 pF	IF matching
C6,C12	0.1 μF	RF bypass
L3	220 nH	IF matching
L1, L2	82 nH	RF choke
R	12 Ω	Adjustable source bias resistor

1. Values of external elements are not final.

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Operating Instructions

The MD59-0054 is a fully integrated upconverter / driver IC for the 824 – 849 MHz cellular frequency band. It includes a differential IF amplifier, a balanced mixer, an LO buffer amplifier, a RF amplifier, a voltage variable attenuator, and a driver amplifier. It also has a power down mode that turns off the current to the part to conserve power when the part is not in use. The part is set in a miniature 4-mm plastic FQFP-N 20-lead package where the backside of the lead frame is exposed to facilitate excellent RF grounding and thermal transfer. The user must add surface mount resistors, inductors and capacitors are used in conjunction with the IC to optimize the trade-offs among performance, tunability and ease of use. The test board schematic provided shows the MMIC and required off-chip component values.

The IFA is a differential pair of single-stage, common source DFET amplifiers. An internal self-biasing resistor in the source is used to set a nominal current of 10 mA (5 mA per amplifier). The input impedance of the IFA is matched externally to 50 ohms at the desired IF frequency with L3, C3 and C4. In addition, C3 and C4 also act as DC blocking capacitors for the differential IF inputs. An external 4:1 transformer can be used to test the device in a single ended 50-ohm system. Inductors L1 and L2 help match the output of the differential IF amplifier to the differential input of the mixer, as well as providing RF chokes for the DC supply lines. The capacitor C5 is a low frequency bypass capacitor for the DC supply line and should be placed as close to the device as is practical.

The LOA is an EFET / DFET cascode amplifier that provides the voltage gain required to drive the gate of the mixer FET while drawing only 3 mA of current nominally. The input port is matched on chip to 50 ohms. Place components C1 and C2, RF and low frequency bypass capacitors for the DC supply line, as close to the device as practical.

The mixer is a balanced floating FET mixer that provides exceptional linearity and isolation with low loss and consumes no DC current. The mixer uses a high-side LO frequency. An external image reject filter is required between the mixer output and driver input to prevent upconversion noise at the image frequency leaking onto the RF. The filter used should have a 50-ohm input and output impedance.

The RFA is a single stage, common source EFET amplifier. The topology of both the input and output matching networks for the RF amplifier provides internal DC blocking capacitors to prevent unwanted DC leakage.

Place components C13 and C14, RF and low frequency bypass capacitors for the DC supply line as close to the device as practical.

The voltage variable attenuator (VVA) has a double-T topology and provides better than 30 dB of attenuation range. Use the VVA_Ctrl input to set the desired attenuation. Capacitor C11 is a bypass capacitor used to provide RF ground to the shunt legs of the attenuator.

The driver amplifier is a two-stage, common source DFET amplifier. Both stages use a self-biasing resistor in their source path to set their bias point. The self-biasing resistor for the first stage is internal and has been chosen for a nominal current of 5 mA. Select the external, self-biasing resistor for the second stage, R1, for a nominal current of 25 mA. You can also select the value of R1 can to adjust the bias current of the second stage, thereby adjusting the driver's linear output power. Components C7, C8, C9 and C10 are RF and low frequency bypass capacitors for the DC supply. Components C12 and C6 are the source bypass capacitors for the first and second stages of the driver respectively. Place these capacitors as close to the device as practical.

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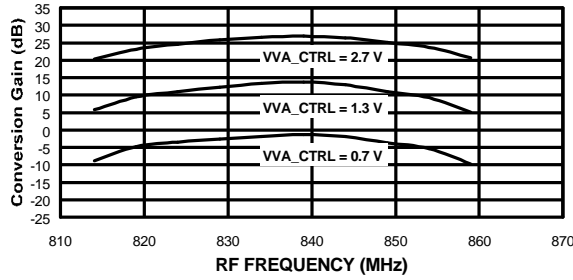
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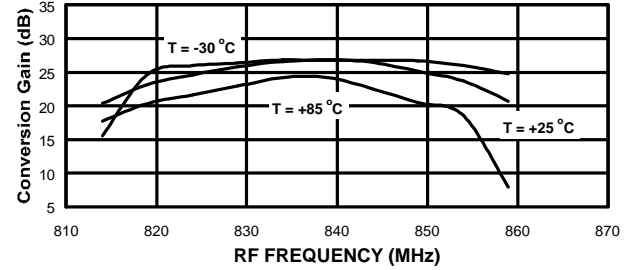
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Typical Performance Curves

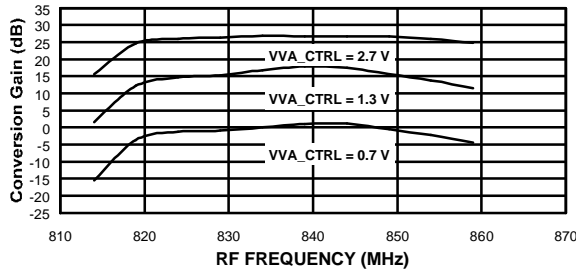
Conversion Gain vs. VVA Control
T = +25 °C, LO = -10 dBm, IF = -12 dBm, V_{DD} = 3.0 V, PD = 2.7 V



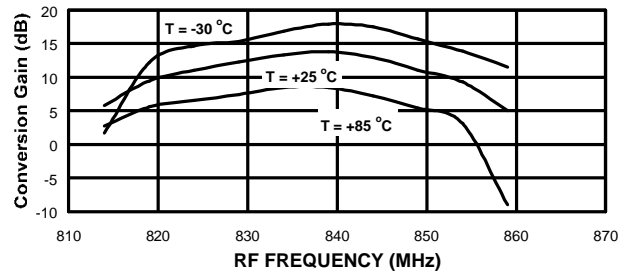
Conversion Gain vs. Temperature
VVA_CTRL = 2.7 V, LO = -10 dBm, IF = -12 dBm, V_{DD} = 3.0 V, PD = 2.7 V



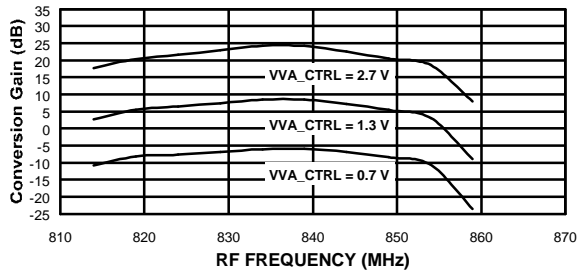
Conversion Gain vs. VVA Control
T = -30 °C, LO = -10 dBm, IF = -12 dBm, V_{DD} = 3.0 V, PD = 2.7 V



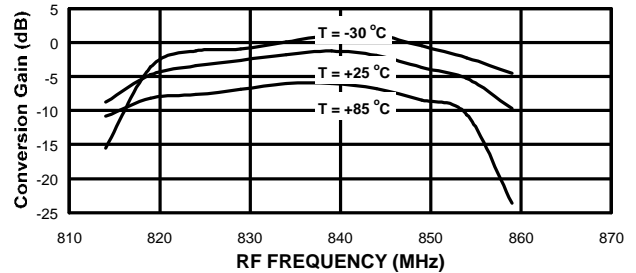
Conversion Gain vs. Temperature
VVA_CTRL = 1.3 V, LO = -10 dBm, IF = -12 dBm, V_{DD} = 3.0 V, PD = 2.7 V



Conversion Gain vs. VVA Control
T = +85 °C, LO = -10 dBm, IF = -12 dBm, V_{DD} = 3.0 V, PD = 2.7 V



Conversion Gain vs. Temperature
VVA_CTRL = 0.7 V, LO = -10 dBm, IF = -12 dBm, V_{DD} = 3.0 V, PD = 2.7 V



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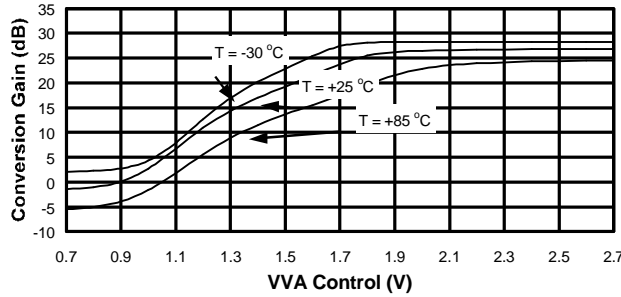
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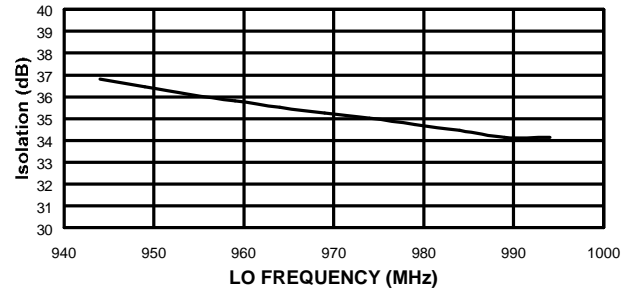


Typical Performance Curves (Cont'd)

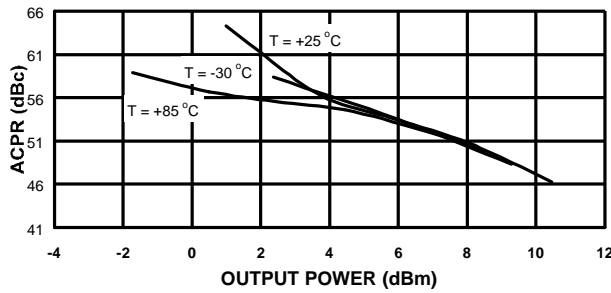
Conversion Gain vs. VVA_CTRL
Over Temperature, LO = -10 dBm,
IF = -12 dBm, V_{DD} = 3.0 V, PD = 2.7 V



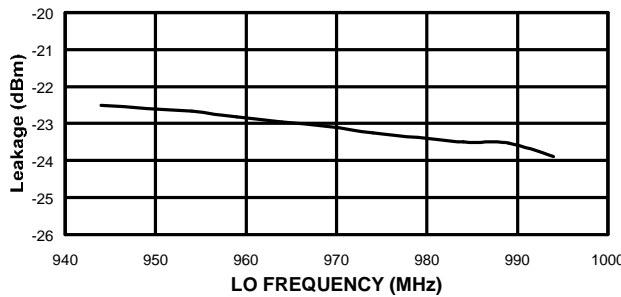
LO-to-IF Isolation, T = +25 °C
IF_Power = -12 dBm,
LO_Power = -10 dBm
V_{DD} = 3.0 V, PD = 2.7 V



ACPR vs. Output Power
Over Temperature, RF = 836.5 MHz
LO = -10 dBm, IF = -12 dBm,
V_{DD} = 3.0 V, PD = 2.7 V



LO-to-MIX_Out Leakage, T = +25 °C
IF_Power = -12 dBm,
LO_Power = -10 dBm
V_{DD} = 3.0 V, PD = 2.7 V



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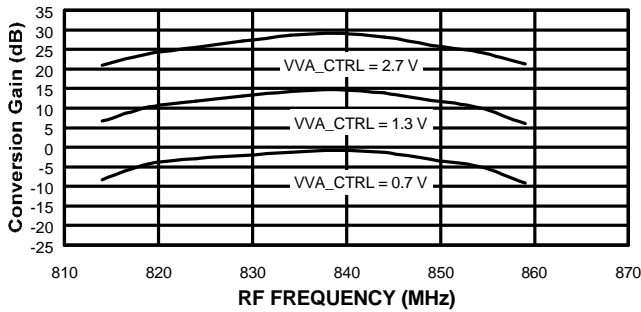
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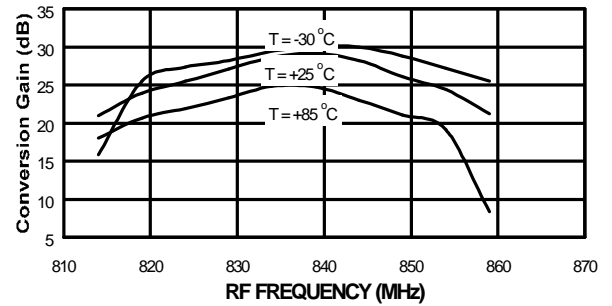


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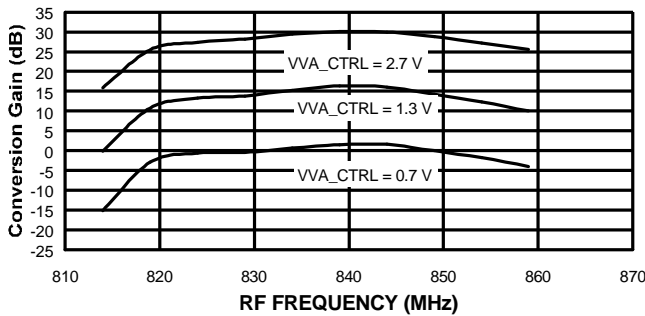
Conversion Gain vs. VVA Control
T = +25 °C, LO = -10 dBm, IF = -15 dBm,
V_{DD} = 3.0 V, PD = 2.7 V



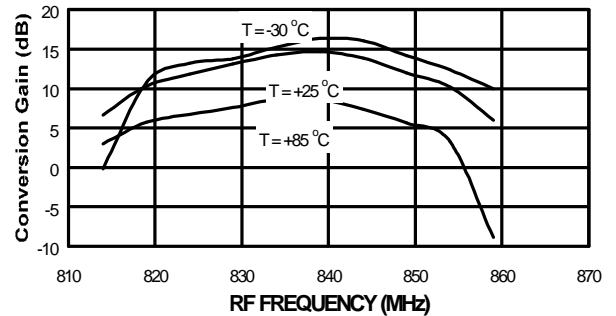
Conversion Gain vs. Temperature
VVA_CTRL = 2.7 V, LO = -10 dBm,
IF = -15 dBm, V_{DD} = 3.0 V, PD = 2.7 V



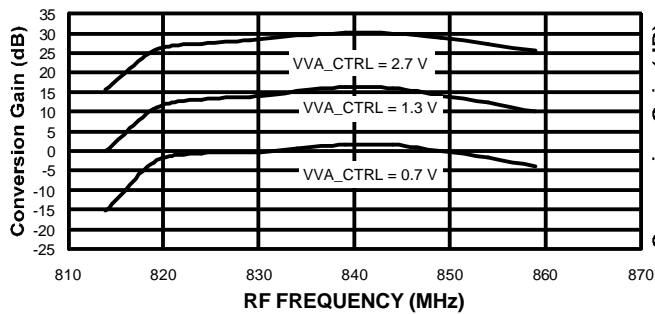
Conversion Gain vs. VVA Control
T = -30 °C, LO = -10 dBm, IF = -15 dBm,
V_{DD} = 3.0 V, PD = 2.7 V



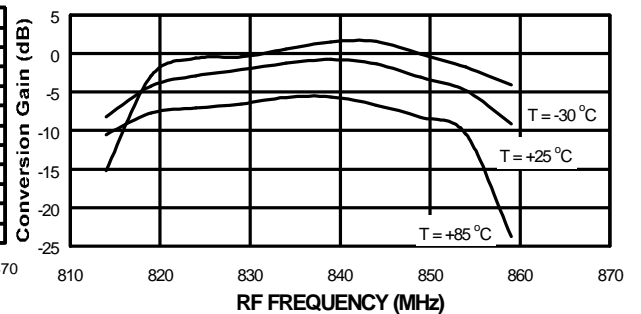
Conversion Gain vs. Temperature
VVA_CTRL = 1.3 V, LO = -10 dBm,
IF = -15 dBm, V_{DD} = 3.0 V, PD = 2.7 V



Conversion Gain vs. VVA Control,
T = +85 °C, LO = -10 dBm, IF = -15 dBm,
V_{DD} = 3.0 V, PD = 2.7 V



Conversion Gain vs. Temperature
VVA_CTRL = 0.7 V, LO = -10 dBm,
IF = -15 dBm, V_{DD} = 3.0 V, PD = 2.7 V



Specifications subject to change without notice.

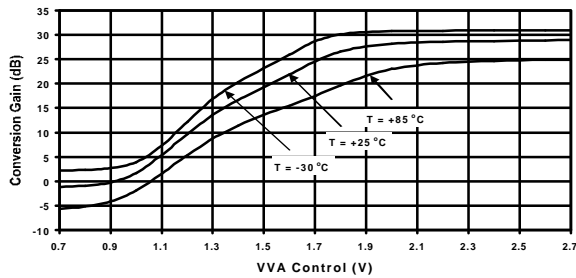
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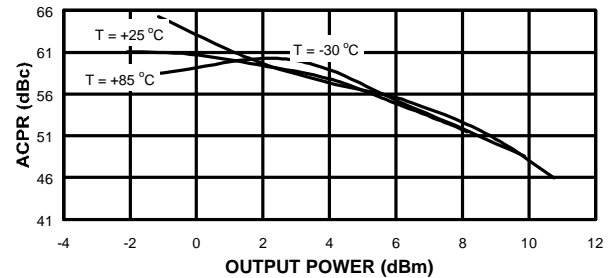


Typical Performance Curves (Cont'd)

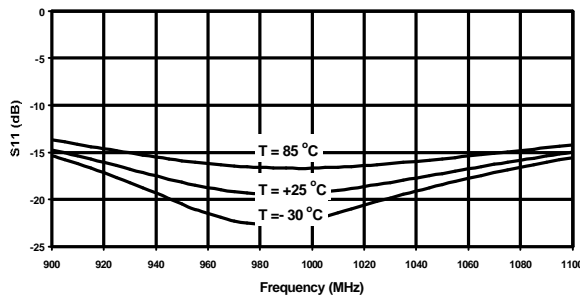
Conversion Gain vs. VVA_CTRL Over Temperature, LO = -10 dBm, IF = -15 dBm, V_{DD} = 3.0 V, PD = 2.7 V Freq = 836.5 MHz



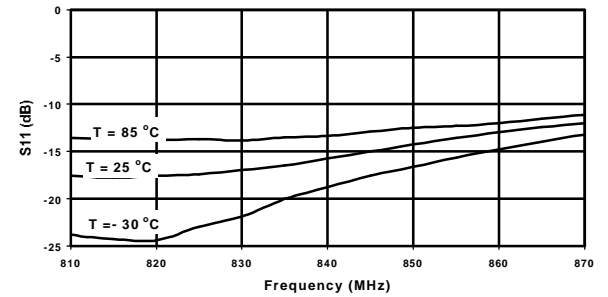
ACPR vs. Output Power Over Temperature, RF = 836.5 MHz, LO = -10 dBm, IF = -15 dBm, V_{DD} = 3.0 V, PD 2.7 V



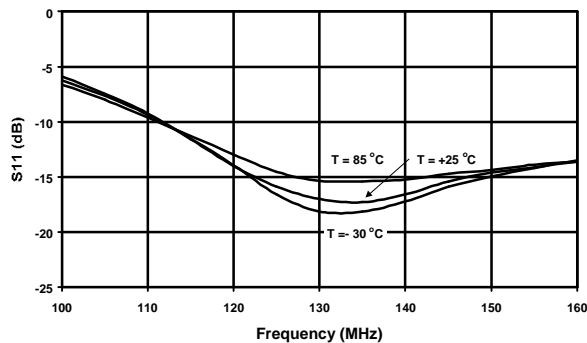
LO Input Port Match Over Temperature V_{DD} = 3.0 V, PD = 2.7 V



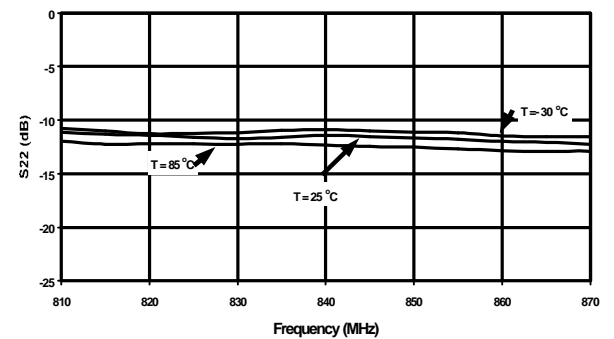
VGA Input Port Match Over Temperature VVA_CTRL = 2.7 V, V_{DD} = 3.0 V, PD = 2.7 V



IF Input Port Match Over Temperature V_{DD} = 3.0 V, PD = 2.7 V



VGA Output Port Match Over Temperature, VVA_CTRL = 2.7 V, V_{DD} = 3.0 V, PD = 2.7 V



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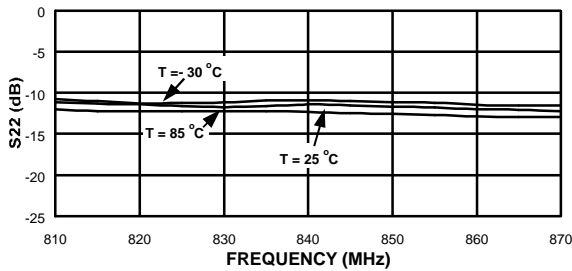
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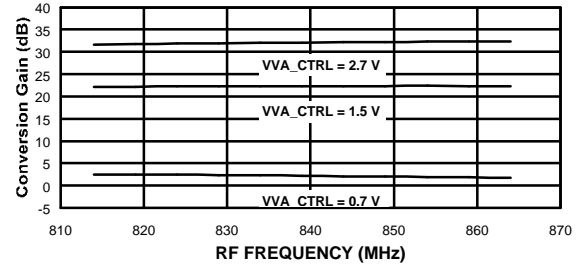


Typical Performance Curves (Cont'd)

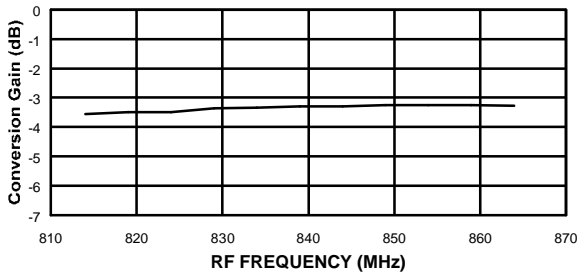
Mixer Output Port Match Over Temperature
 $V_{DD} = 3.0\text{ V}$, $PD = 2.7\text{ V}$



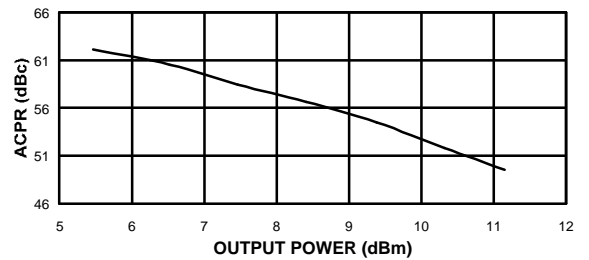
Driver Section Gain vs. VVA Control
 $T = +25\text{ °C}$, $Input\ Power = -25\text{ dBm}$,
 $V_{DD} = 3.0\text{ V}$, $PD = 2.7\text{ V}$



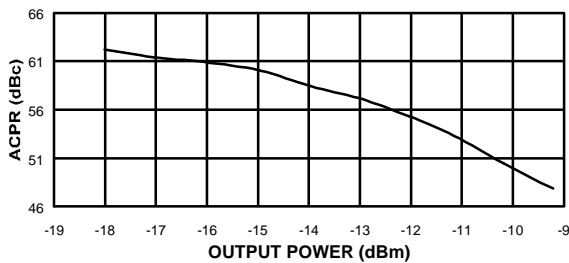
Upconverter Conversion Gain
 $T = +25\text{ °C}$, $LO = -10\text{ dBm}$, $IF = -12\text{ dBm}$,
 $V_{DD} = 3.0\text{ V}$, $PD = 2.7\text{ V}$



Driver Section ACPR vs. Output Power
 $T = +25\text{ °C}$, $RF = 836.5\text{ MHz}$,
 $VVA_CTRL = 2.7\text{ V}$, $V_{DD} = 3.0\text{ V}$, $PD = 2.7\text{ V}$



Upconverter ACPR vs. Output Power
 $T = +25\text{ °C}$, $RF = 836.5\text{ MHz}$,
 $LO = -10\text{ dBm}$, $V_{DD} = 3.0\text{ V}$, $PD = 2.7\text{ V}$



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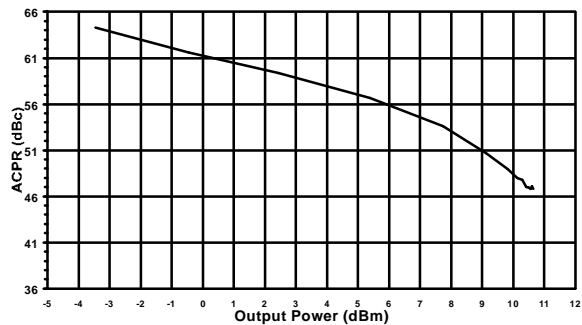
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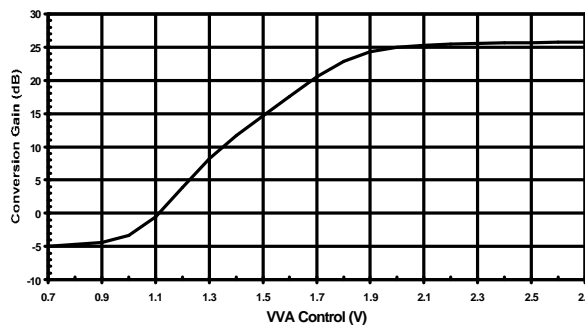


CDMA-One Performance

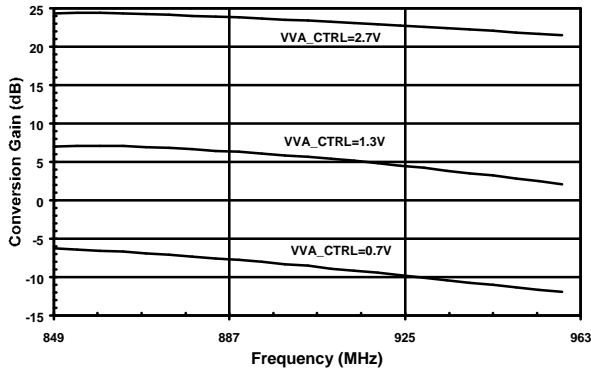
CDMA-One ACPR vs Output Power at 25 °C, RF Freq = 906 MHz, IF Freq = 167 MHz, LO Power = -10 dBm, IF Power = -15 dBm, V_{DD} = 3.0 V, PD = 2.7 V



CDMA-One Conversion Gain vs VVA Control Voltage at 25 °C, RF Freq = 906 MHz, IF Freq = 167 MHz, LO Power = -10 dBm, IF Power = -15 dBm, V_{DD} = 3.0 V, PD = 2.7 V



CDMA-One Conversion Gain vs VVA Control Voltage at 25 °C, RF Freq = 906 MHz, IF Freq = 167 MHz, Lowside LO, LO Power = -10 dBm, IF Power = -15 dBm, V_{DD} = 3.0 V, PD = 2.7 V

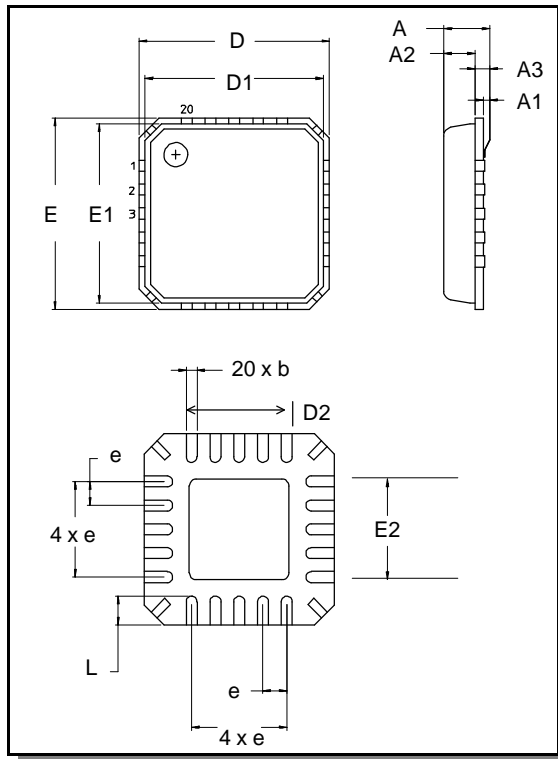


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4 mm FQFP-N-20¹

1. See JEDEC MO-220A VGGD-1 for additional dimensional and tolerance information.

4 mm FQFP-N-20

Dim.	Measurement (mm)		
	Min.	Nom.	Max.
A	0.80	0.90	1.00
A1	0	0.02	0.05
A2	0	0.65	1.00
A3		0.25 ref.	
b	0.18	0.23	0.30
D		4.00 basic	
D1		3.75 basic	
D2	0.75	1.70	2.25
e		0.50 basic	
E		4.00 basic	
E1		3.75 basic	
E2	0.75	1.70	2.25
L	0.35	0.55	0.75

Ordering Information

Part Number	Package
MD59-0054	4-mm Plastic FQFP-N Package
MD59-0054TR	Forward Tape and Reel ¹

1. If specific reel size is required, consult factory for part number assignment.

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