MD59-0043

Highly Linear LNA / Downconverter 800 - 900 MHz

Features

- Highly integrated LNA and downconverter
- Operates with supply voltage from 2.7V to 5V
- Low noise figure, 2.3 dB Typical
- Ultra-low current consumption
- High input intercept point
- Stepped gain control
- Low LO drive level, -6 dBm
- Miniature 4mm MLF plastic package

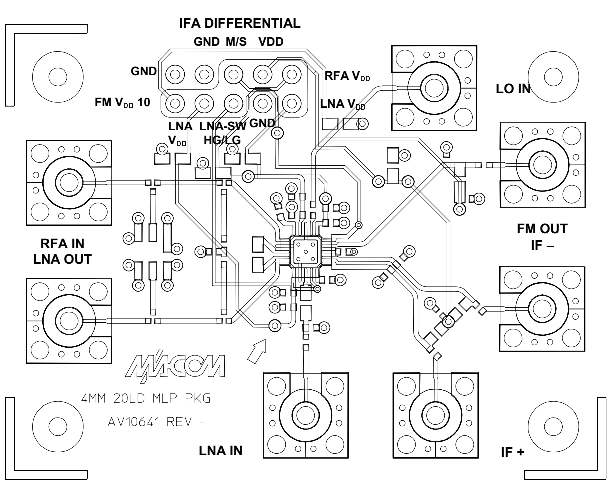
Description

M/A-COM's MD59-0043 integrated downconverter combines a low noise amplifier, RF amplifier, mixer, IF amplifier, and LO buffer in a miniature 4 millimeter plastic MLF package that has an exposed paddle for improved high frequency grounding.

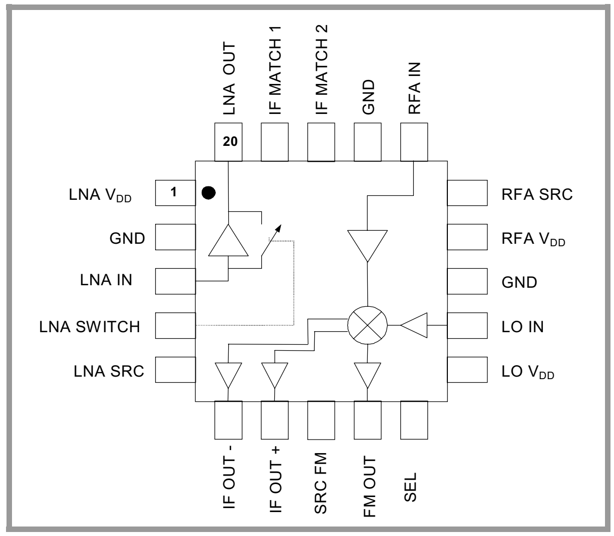
M/A-COM designed the MD59-0043 for CDMA handsets requiring wide dynamic range and low power consumption. The LNA features stepped gain control for use in wide dynamic range receivers.

M/A-COM fabricates the MD59-0043 using a 0.5 micron low noise E/D GaAs MESFET process. The process features full passivation for increased performance and reliability.

Recommended PCB Configuration



Functional Schematic



Pin Configuration

PIN No.	PIN Name	Description
1	LNA V_{DD}	LNA V_{DD} line (DC Current to the LNA)
2	GND	DC Ground
3	LNA IN	LNA Input PIN
4	LNA SW	LNA switch used to set LNA in High (2.7V) or Low (0V) gain mode
5	LNA	LNA Source RF Bypass
6	IF– OUT	Differential IF Amplifier Output
7	IF+ OUT	Differential IF Amplifier Output
8	FM SRC	Single Ended IFA Source RF Bypass
9	FM OUT	Single Ended IFA Output
10	SEL	Selects Differential (2.7V) or Single ended (0V)
11	LO V_{DD}	LO Amplifier V_{DD} (DC Current to the LOA)
12	LO IN	LO Input PIN
13	GND	Ground
14	RFA V_{DD}	RF Amplifier V_{DD} (DC Current to the RFA)
15	RFA	RFA Source RF Bypass
16	RFA IN	RFA Input from a SAW Filter
17	GND	Ground
18	M+	IFA Input Matching PIN 1
19	M-	IFA Input Matching PIN 2
20	LNA	LNA Output to a SAW Filter

Electrical Specifications T_A = +25°C, V_{DD} = 2.7 Volts

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Low Noise Amplifier					
Gain	Frequency = 0.88 GHz	dB		10.5	
Noise Figure		dB		1.2	
V_{SWR} In / Out				2:1	
Input IP_3		dBm		+8.0	
I_{DD}		mA		5	
Low Noise Amplifier Bypass					
Gain	Frequency = 0.88 GHz	dB		-4.5	
Noise Figure		dB		4.5	
V_{SWR} In / Out				2:1	
Input IP_3		dBm		> +23	
I_{DD}		mA		0	
Complete LNA / Downconverter High Gain Mode[1]					
Conversion Gain	RF = 0.88 GHz	dB		28	
Noise Figure	LO = 1.01 GHz, LO Level = -6 dBm	dB		2.3	
Input IP_3	IF = 130 MHz	dBm		-12	
LO-to-RF Isolation		dB		40	
LO-to-IF Isolation		dB		30	
RF-to-IF Isolation		dB		20	
I_{DD}		mA		21	
Complete LNA / Downconverter Low Gain Mode[1]					
Conversion Gain	RF = 0.88 GHz	dB		13	
Noise Figure	LO = 1.01 GHz, LO Level = -6 dBm	dB		11.5	
Input IP_3	IF = 130 MHz	dBm		+3	
LO-to-RF Isolation		dB		35	
LO-to-IF Isolation		dB		30	
RF-to-IF Isolation		dB		30	
I_{DD}		mA		16	
Complete LNA / Downconverter FM Mode[1]					
Conversion Gain	RF = 0.88 GHz	dB		20	
Noise Figure	LO = 1.01 GHz, LO Level = -6 dBm	dB		2.5	
Input IP_3	IF = 130 MHz	dBm		-1	
LO-to-RF Isolation		dB		40	
LO-to-IF Isolation		dB		30	
RF-to-IF Isolation		dB		30	
I_{DD}		mA		17	

1 Complete downconverter measurements taken with 3 dB pad between LNA output and RFA in.

Operating Instructions

The MD59-0043 is a highly integrated MMIC downconverter for the 800 – 900 MHz cellular band. The downconverter provides exceptional RF performance while drawing low DC current and is assembled in a low cost plastic package. The MD59-0043 incorporates both a single ended and differential IF outputs that allow for dual band cellular operation. It is an ideal candidate for light-weight, battery operated, portable handset applications.

The MD59-0043 incorporates an LNA, RFA, LOA, Mixer, differential IF, and single ended IF amplifiers. Surface mount inductors and capacitors are used in conjunction with the MMIC to optimize the trade-offs between performance, tunability and ease of use. The schematic on page 5 shows the MMIC and required off-chip component values.

The LNA is biased at 5 mA nominally. The components L1, C1, and C2, are tuning elements for the input matching network. Capacitor C1 is often just replaced with a short as there is a DC blocking capacitor present on-chip. Capacitor C3 is a RF frequency bypass capacitor for the DC supply line. Capacitor C4 is used to bypass the source of the LNA. The output matching is done all on-chip and includes a DC blocking capacitor. The LNA has two gain states, a high gain state when 2.7V is placed on the 'LNA Switch' pin and a low gain state when 0 Volts is placed on the 'LNA Switch' pin. The circuit has been designed to provide insensitivity to voltage changes on the 'LNA Switch' pin thus the 'high gain' mode requires a voltage from 2.4-3.0 Volts and the 'low gain' mode requires a voltage of 0-0.3 Volts. The position of both C3 and C4 shown in the application circuit may affect the gain of the LNA amplifier and should be placed as close the device as is practical. An off chip SAW (Surface Acoustic Wave) Filter is required between the LNA and the RFA to reject out of band signals at the LNA input from leaking into the downconverter section of the chip.

The matching network topology of both the input and output matching networks for the RF amplifier provides internal DC blocking capacitors, to prevent unwanted DC leakage. Both of these networks are entirely on-chip. Capacitor C5 is a source bypass capacitor for the RF amplifier. C6 is a RF bypass capacitor for the DC supply line. Similar to the LNA, C5 and C6 should be placed as close the device as is practical.

The LO input port is matched on chip to 50 Ω. The LO buffer amplifier provides the voltage gain required to drive the gate of the mixer FET, while drawing a minimal amount of current. The LO buffer amplifies the –10 dBm input signal to the level required to drive the mixer. For optimum performance, it is recommended to use a drive level of –6 dBm. Capacitor C7 provides a DC block on the input of the LOA. C9 is a RF frequency bypass capacitor for the DC supply line. L3 is used tune the output of the LOA for low side operation. When this is the case, C9 is left open and C8 is used as the RF bypass capacitor.

The mixer is a balanced floating FET mixer that provides exceptional linearity and isolation with low loss and requires no DC current.

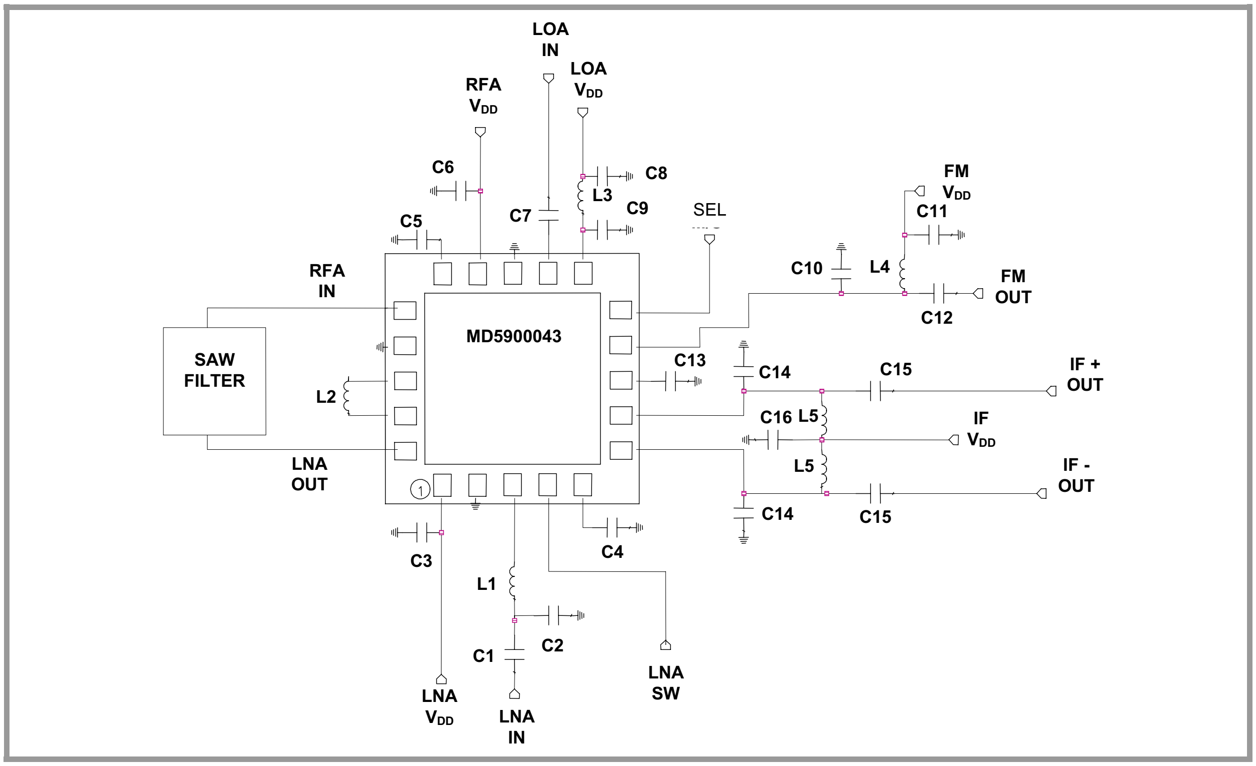
The input to the single and differential IF amplifiers are tuned using the inductor L2. The output impedance of the differential IF amplifier is matched externally to 50 Ω at the desired IF frequency with L5, C14 and C15. The L5 inductors also act as the RF chokes to the DC supply lines. In addition, the C15 capacitors act as a DC block for the differential IF outputs. Similarly, the single ended IF Amplifier output is matched to 50 Ω using L4, C10, and C12. L4 also acts as an RF choke and C12 acts as a DC block. Capacitor C11 and C16 are low frequency bypass capacitors. Switching between the differential IF amplifier and the single ended IF amplifier is done by placing 0-0.3 Volts on the 'Sel' (Mode Select) pin and providing 2.7 Volts to the 'FM OUT' pin. The IF V_{DD} line can remain at 2.7 Volts. Differential mode requires 2.4-3.0 Volts on the 'Sel' pin and 'FM OUT' to be 0 Volts.

It is recommended that all of the DC source lines have a decoupling capacitor of at least 0.1 uF present somewhere on the board. This is a standard operating procedure in many handsets. Omission of these decoupling capacitors may impact the device performance.

Logic Table for All Three Modes of Operation

Gain State	LNA Sw	SEL	FM V_{DD}
High	2.7	2.7	0
Low	0	2.7	0
AMPS	2.7	0	2.7

Sample Board Schematic



External Circuitry Parts List - US CDMA

Ref. Designation	Value	Purpose
L1	22 nH	LNA Input Matching
L2	220 nH	IFA Input Matching
L3	Short	LOA Output Matching
L4	150 nH	FM IFA Output Matcing
L5	120 NH	Differential IFA Output Matching
C1	Short	LNA Input Matching (Series)
C2	Open	LNA Input Matching (Shunt)
C3	1000 pF	LNA V_{DD} RF Bypass
C4	0.1 uF	LNA Source Bypass
C5	0.1 uF	RFA Source Bypass
C6	47 pF	RFA V_{DD} RF Bypass
C7	1000 pF	LOA Input DC Block
C8	Open	LOA V_{DD} RF Bypass 1
C9	1000 pF	LOA V_{DD} RF Bypass 2
C10	Open	FM Output Matching (Shunt)
C11	1000 pF	FM V_{dd} RF Bypass
C12	7 pF	FM Output Matching (Series)
C13	1000 pF	FM Source Bypass
C14	Open	Differential IFA Output Matching (Shunt)
C15	10 pF	Differential IFA Output Matching (Series)
C16	1000 pF	Differential IFA V_{DD} RF Bypass

External Circuitry Parts List - Japanese

Ref. Designation	Value	Purpose
L1	22 nH	LNA Input Matching
L2	270 nH	IFA Input Matching
L3	5.1 nH	LOA Output Matching
L4	150 nH	FM IFA Output Matcing
L5	150 nH	Differential IFA Output Matching
C1	Short	LNA Input Matching (Series)
C2	Open	LNA Input Matching (Shunt)
C3	1000 pF	LNA V_{DD} RF Bypass
C4	0.1 uF	LNA Source Bypass
C5	0.1 uF	RFA Source Bypass
C6	47 pF	RFA V_{DD} RF Bypass
C7	1000 pF	LOA Input DC Block
C8	1000 pF	LOA V_{DD} RF Bypass 1
C9	Open	LOA V_{DD} RF Bypass 2
C10	4 pF	FM Output Matching (Shunt)
C11	1000 pF	FM V_{DD} RF Bypass
C12	8.2 pF	FM Output Matching (Series)
C13	1000 pF	FM Source Bypass
C14	Open	Differential IFA Output Matching (Shunt)
C15	10 pF	Differential IFA Output Matching (Series)
C16	1000 pF	Differential IFA V_{DD} RF Bypass

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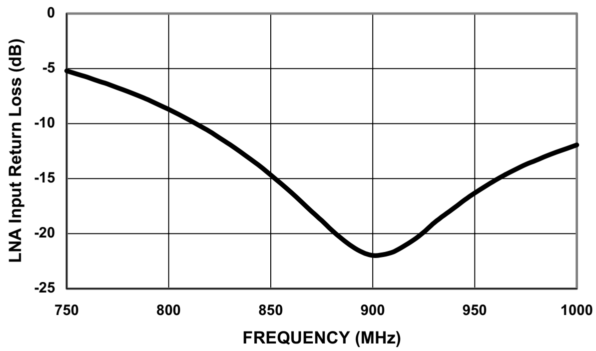
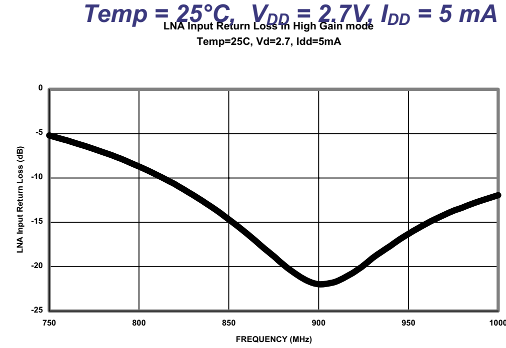
Typical Performance Curves

LNA

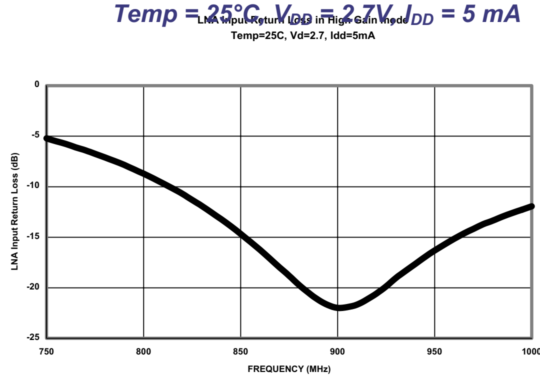
Input Return Loss in High Gain Mode
Temp = 25°C, V_{DD} = 2.7V, I_{DD} = 5 mA



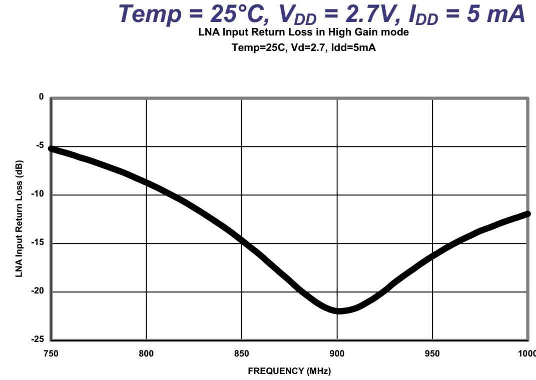
Output Return Loss in High Gain Mode
Temp = 25°C, V_{DD} = 2.7V, I_{DD} = 5 mA



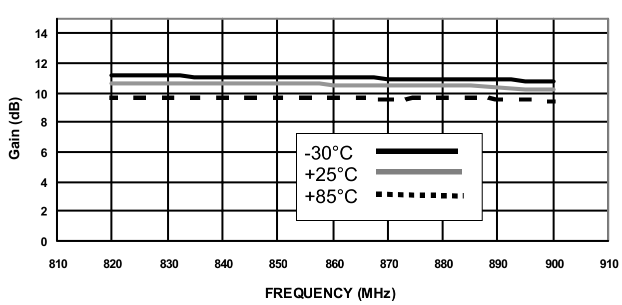
Input Return Loss in Low Gain Mode
Temp = 25°C, V_{DD} = 2.7V, I_{DD} = 5 mA



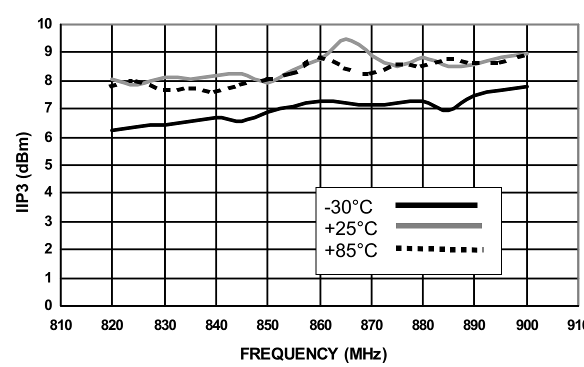
Output Return Loss in Low Gain Mode
Temp = 25°C, V_{DD} = 2.7V, I_{DD} = 5 mA



Gain vs. Temperature in High Gain Mode
V_{DD} = 2.7V, I_{DD} = 5 mA



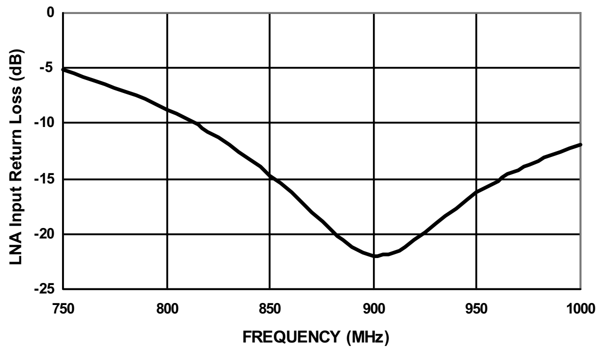
IIP_3 vs. Temperature in High Gain Mode



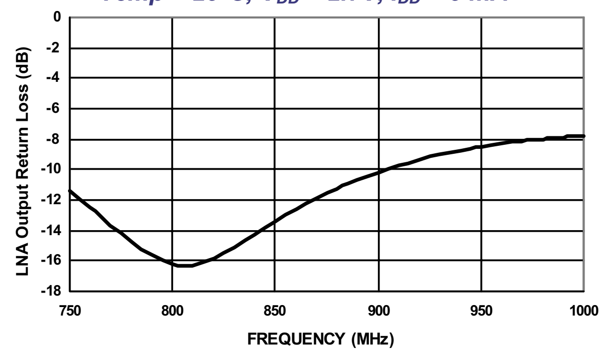
Typical Performance Curves (Cont'd)

LNA (Cont'd)

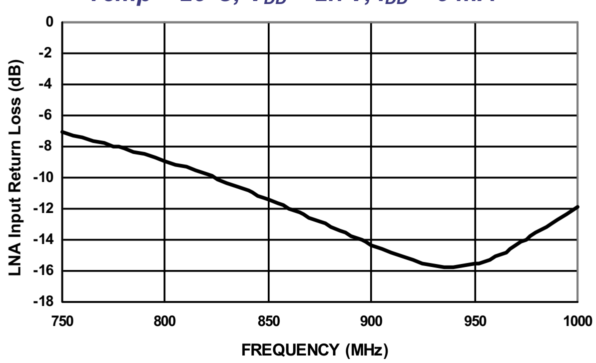
Input Return Loss in High Gain Mode
Temp = 25°C, V_{DD} = 2.7V, I_{DD} = 5 mA



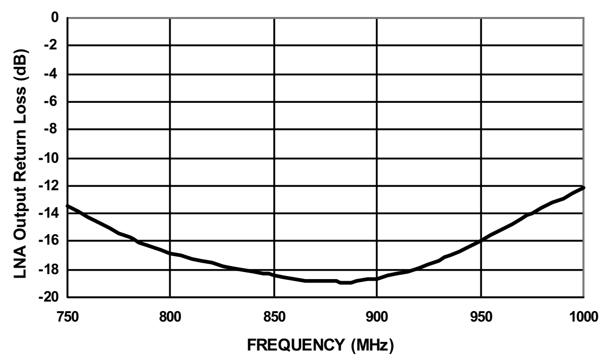
Output Return Loss in High Gain Mode
Temp = 25°C, V_{DD} = 2.7V, I_{DD} = 5 mA



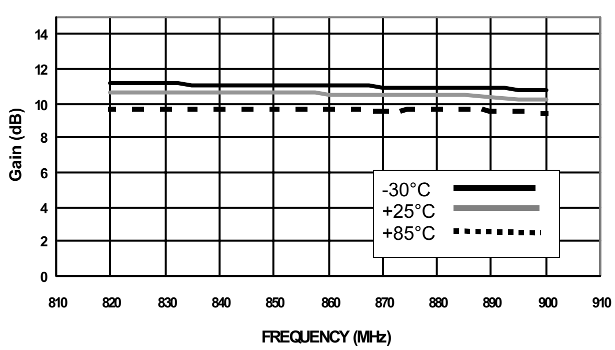
Input Return Loss in Low Gain Mode
Temp = 25°C, V_{DD} = 2.7V, I_{DD} = 5 mA



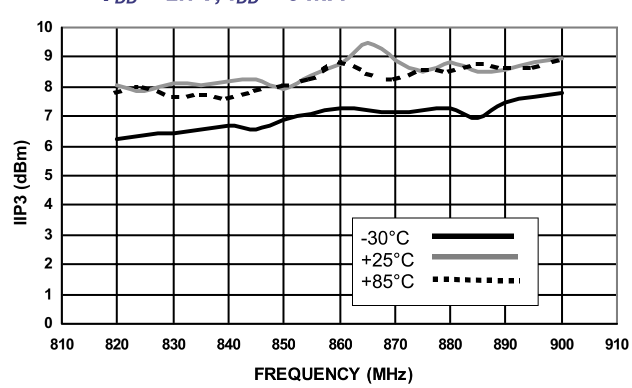
Output Return Loss in Low Gain Mode
Temp = 25°C, V_{DD} = 2.7V, I_{DD} = 5 mA



Gain vs. Temperature in High Gain Mode
V_{DD} = 2.7V, I_{DD} = 5 mA



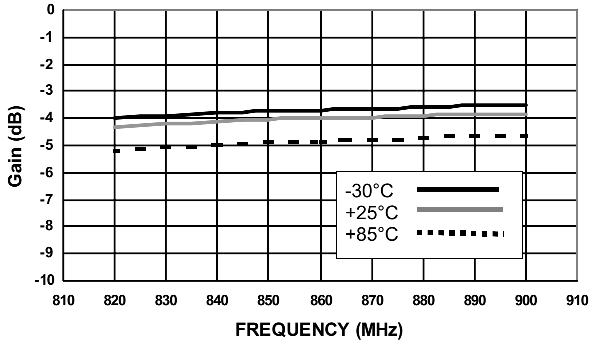
IIP_3 vs. Temperature in High Gain Mode
V_{DD} = 2.7V, I_{DD} = 5 mA



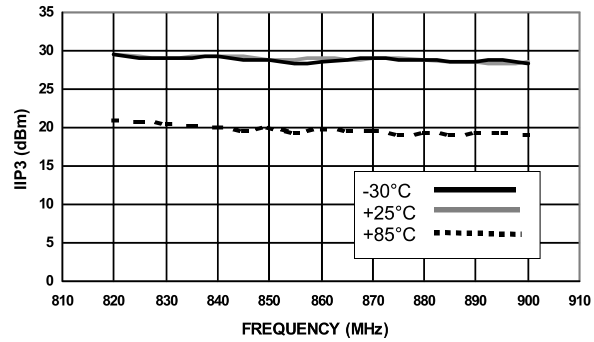
Typical Performance Curves (Cont'd)

LNA (Cont'd)

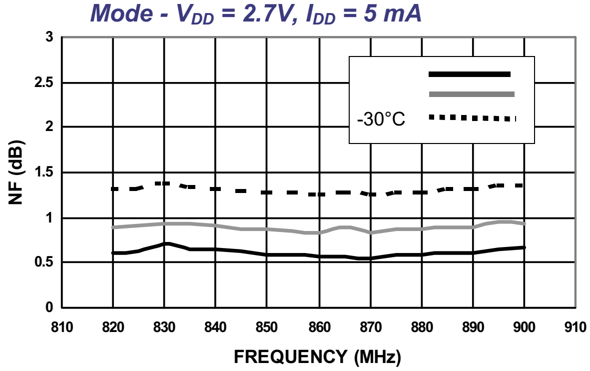
Gain vs. Temperature in Low Gain Mode V_{DD} = 2.7V, I_{DD} = 0 mA



IIP3 vs. Temperature in Low Gain Mode V_{DD} = 2.7V, I_{DD} = 0 mA

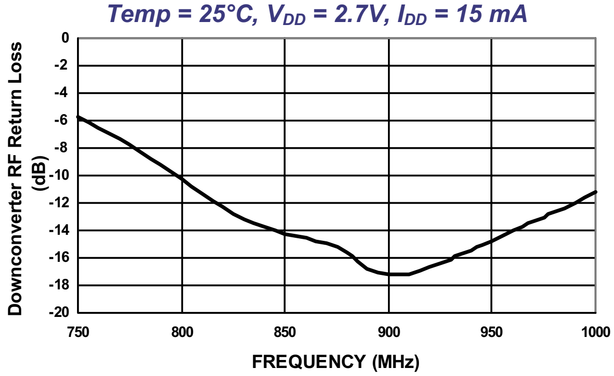


Noise Figure vs. Temperature in High Gain Mode - V_{DD} = 2.7V, I_{DD} = 5 mA

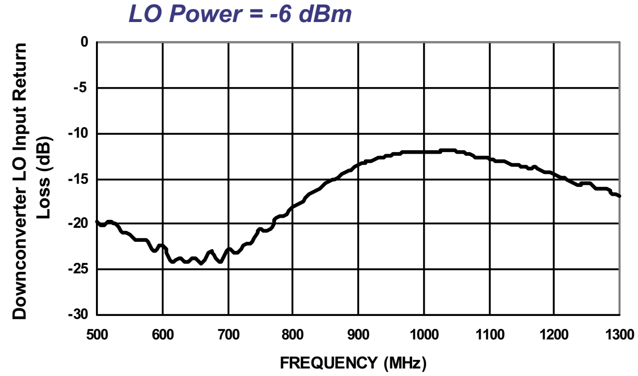


Downconverter

RF Return Loss Temp = 25°C, V_{DD} = 2.7V, I_{DD} = 15 mA



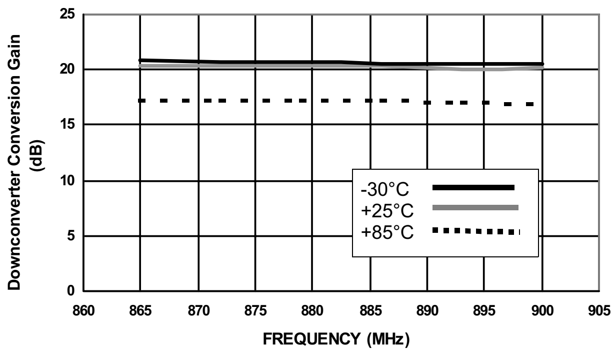
LO Input Return Loss Temp = 25°C, V_{DD} = 2.7V, I_{DD} = 15 mA, LO Power = -6 dBm



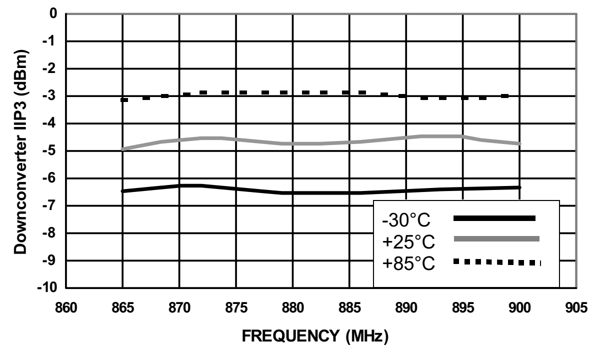
Typical Performance Curves (Cont'd)

Downconverter (Cont'd)

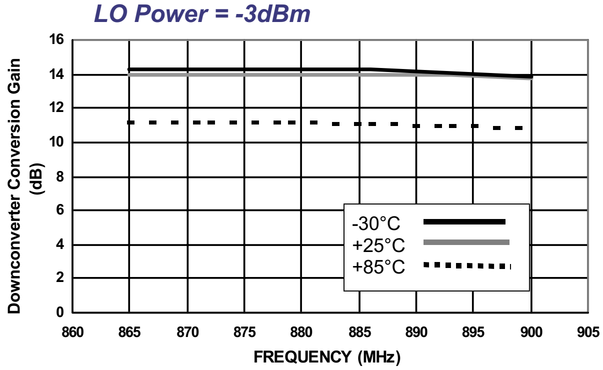
Conversion Gain vs. Temperature in Differential Mode - V_{DD} = 2.7V, I_{DD} = 15 mA, LO Power = -3dBm



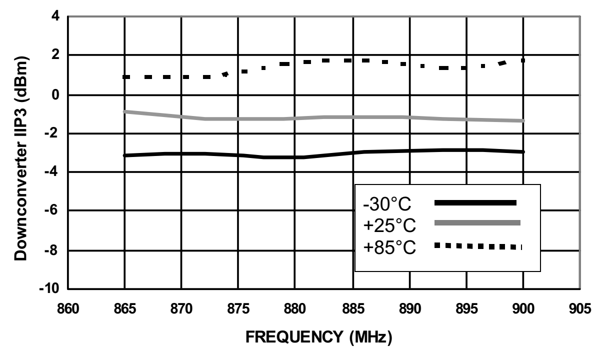
IIP_3 vs. Temperature in Differential Mode V_{DD} = 2.7V, I_{DD} = 15 mA, LO Power = -3 dBm



Conversion Gain vs. Temperature in FM Mode - V_{DD} = 2.7V, I_{DD} = 12 mA, LO Power = -3dBm

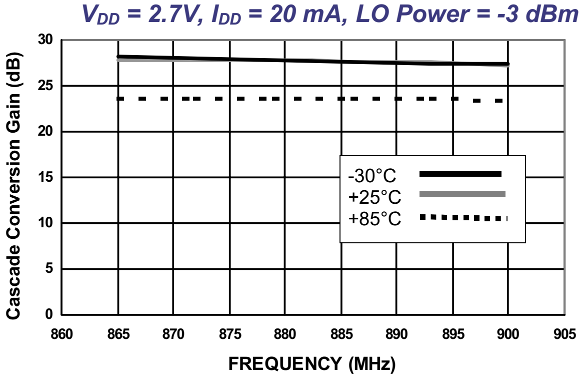


IIP_3 vs. Temperature in FM Mode V_{DD} = 2.7V, I_{DD} = 12 mA, LO Power = -3 dBm

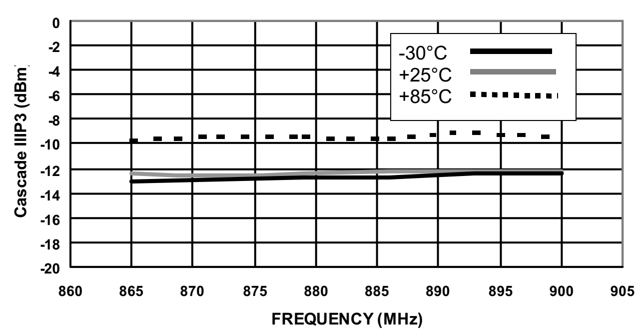


Cascade

Conversion Gain vs. Temperature in Differential High Gain Mode with 3dB Pad V_{DD} = 2.7V, I_{DD} = 20 mA, LO Power = -3 dBm



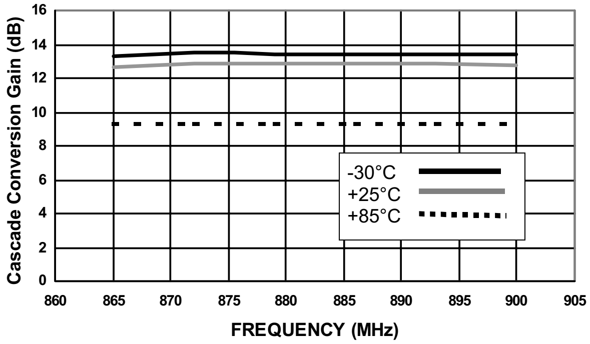
IIP_3 vs. Temperature in Differential High Gain Mode with 3dB Pad V_{DD} = 2.7V, I_{DD} = 20 mA, LO Power = -6 dBm



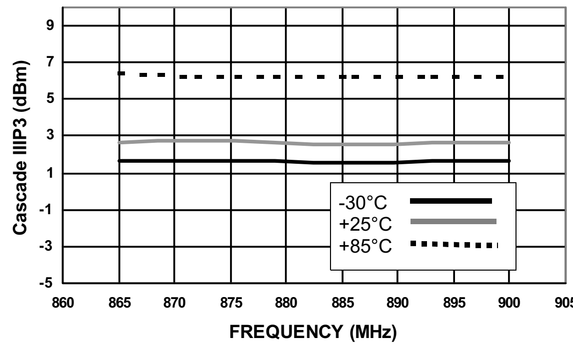
Typical Performance Curves (Cont'd)

Cascade (Cont'd)

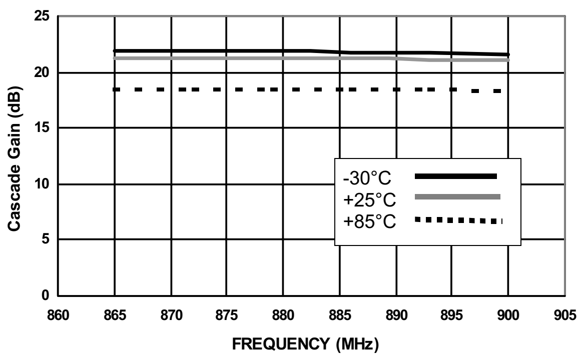
Conversion Gain vs. Temperature in Differential Low Gain Mode with 3dB Pad
V_{DD} = 2.7V, I_{DD} = 15 mA, LO Power = -3dBm



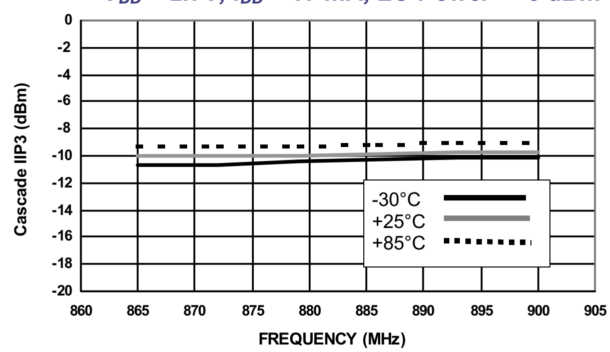
IIP_3 vs. Temperature in Differential Low Gain Mode with 3dB Pad
V_{DD} = 2.7V, I_{DD} = 15 mA, LO Power = -3 dBm



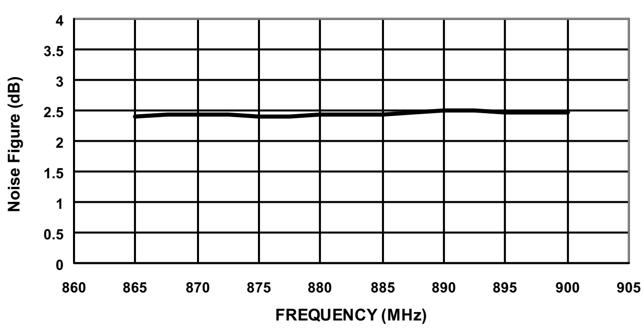
Gain vs. Temperature in FM Mode with 3dB Pad
V_{DD} = 2.7V, I_{DD} = 17 mA, LO Power = -3dBm



IIP_3 vs. Temperature in FM Mode with 3dB Pad
V_{DD} = 2.7V, I_{DD} = 17 mA, LO Power = -3 dBm



Noise Figure in High Gain Differential Mode
Temp = 25°C, V_{DD} = 2.7V, I_{DD} = 20 mA,
LO Power = -6 dBm



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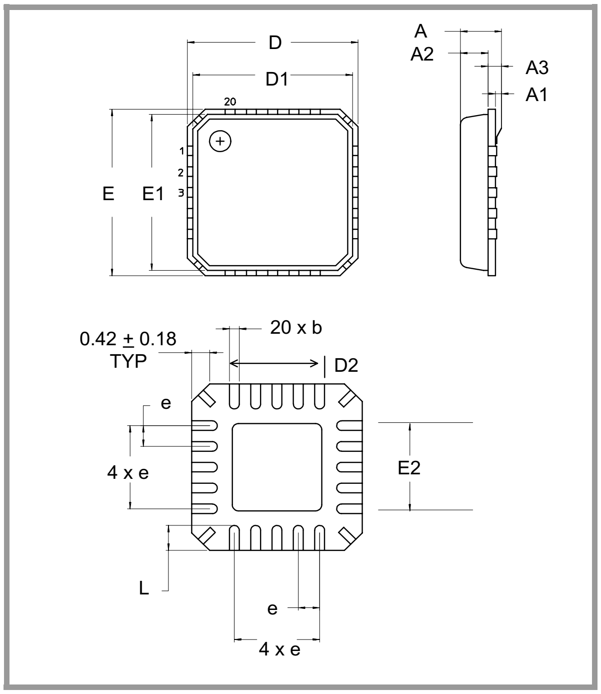
4 mm MLF-20[1]



1 See JEDEC MO-2220A VGGD-1 for additional dimensional and tolerance information.

4 mm MLF-20[1]

Dim.	Measurement (mm)		
	Min.	Nom.	Max.
A	0.80	0.90	1.00
A1	0	0.02	0.05
A2	0	0.65	1.00
A3		0.25 ref.	
b	0.18	0.23	0.30
D		4.00 basic	
D1		3.75 basic	
D2	0.75	1.70	2.25
e		0.50 basic	
E		4.00 basic	
E1		3.75 basic	
E2	0.75	1.70	2.25
L	0.35	0.55	0.75

Ordering Information

Part Number	Package
MD59-0043	MLF-4.0 mm Plastic Package
MD59-0043TR	Forward Tape and Reel[1]
MD59-0043RTR	Reverse Tape and Reel[1]

[1] If specific reel size is required, consult factory for part number assignment.

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