

# High Speed, 200V, Full H-Bridge MOSFET Driver

## Features

- ▶ HVCMOS® technology for high performance
- ▶ All N-MOSFET full-bridge driver
- ▶ Designed for 200V bridge supply voltage
- ▶ Up to 1.0MHz operation frequency
- ▶ Greater than 90% efficiency
- ▶ Designed for low total harmonic distortion
- ▶ Single voltage drive power supply +12V
- ▶ Smart logic voltage threshold
- ▶ Resistor programmable OCP threshold
- ▶ UVP function built-in
- ▶ Accurate and adjustable dead time
- ▶ 32-Lead QFN package

## Applications

- ▶ Class-D audio amplifier
- ▶ High frequency PWM motor control
- ▶ High frequency switching power supply
- ▶ Ultrasound transducer drivers
- ▶ High voltage waveform generator

## General Description

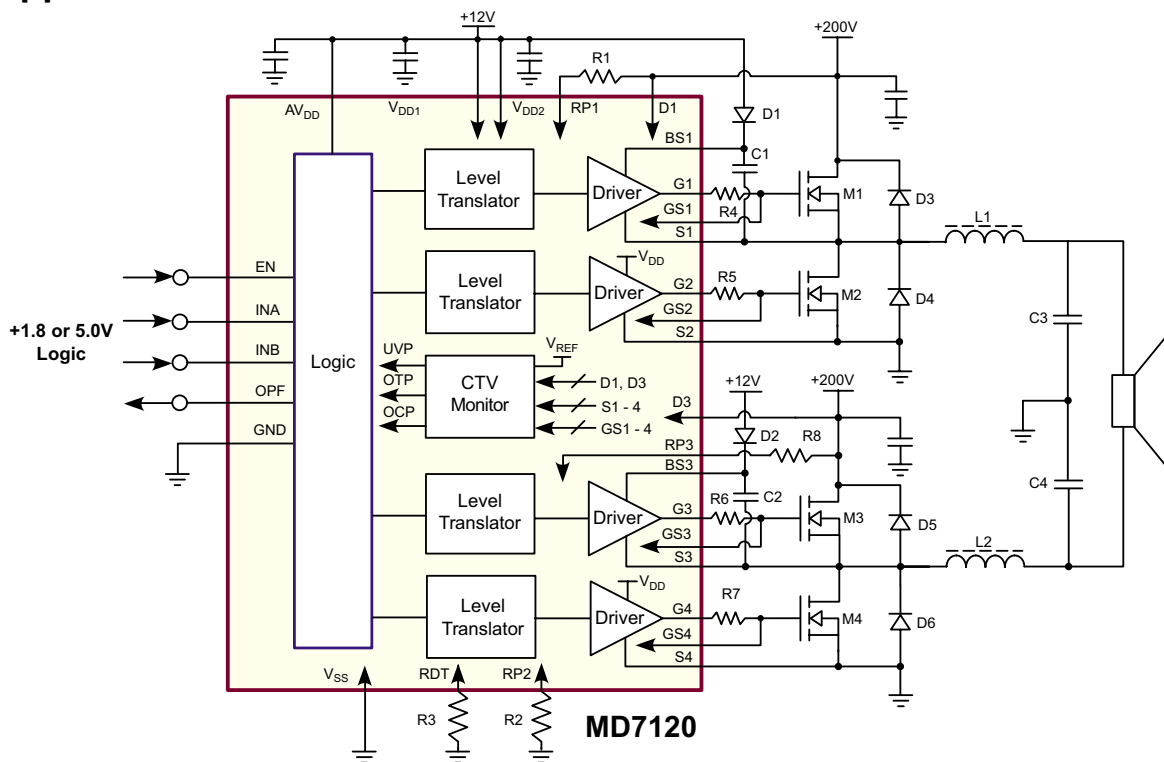
The Supertex MD7120 is a high voltage, high speed, full-bridge driver. It is ideal for Class-D audio amplifier applications and other high frequency PWM driver applications, such as motor driving. This high-voltage and high-speed driver can also be used for other applications: as a piezo-electric transducer driver; as a MOSFET driver in a switched mode power supply; or as a two channel driver for half-bridge power supplies.

The new IC topology is designed to drive dual N-MOSFETs as power switches for both the high side and low side. It consists of controller logic circuits, level translators, and a bootstrap floating powered gate driver and over current protection circuits without using current sensing resistors. The thresholds of the OCP for the high and low side are resistor-programmable.

The power MOSFET top drain can be connected to up to +200V while the bottom N-channel MOSFET source is grounded. They are designed to provide 3.0A peak driving current with well-matched output impedance and propagation delay on the high and low sides, as well as from device-to-device.

The EN pin serves a dual purpose: the logic high level is used to compute the threshold voltage level of inputs; and the logic low level disables the outputs. The IC is in a low inductance and thermally enhanced package.

## Typical Application Circuit



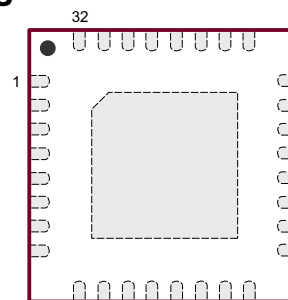
## Ordering Information

Device	Package Option
	32-Lead QFN, 7x7mm body, 1.00mm height (max.), 0.65 pitch
MD7120	MD7120K6-G

-G indicates package is RoHS compliant ("Green")

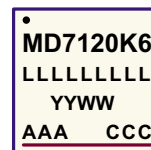


## Pin Configuration



32-Lead QFN (K6)  
(top view)

## Product Marking



L = Lot Number  
YY = Year Sealed  
WW = Week Sealed  
A = Assembler ID  
C = Country of Origin  
— = "Green" Packaging

32-Lead QFN (K6)

## Absolute Maximum Ratings

Parameter	Value
V <sub>DD</sub> , (BS1-S1), (BS3-S3) supply voltage	-0.5V to 15V
V <sub>PP</sub> , high voltage supply	10V to +220V
EN, IN <sub>A</sub> , IN <sub>B</sub> logic input voltage	-0.5V to 7.5V
OPF, open drain output voltage	-0.5V to 15V
Junction operating temperature range	-40°C to +125°C
Storage temperature	-65°C to 150°C
Thermal resistance ( $\theta_{JA}$ )*	29.3°C/W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

\* 1oz, 4-layer, 4x3" PCB

DC Electrical Characteristics (Over operating conditions, unless otherwise specified. V<sub>DD</sub> = 12V, V<sub>PP</sub> = 200V, T<sub>A</sub> = 25°C)

Sym	Parameter	Min	Typ	Max	Units	Conditions
V <sub>DD</sub>	Positive drive supply voltage	9.0	12	13	V	---
V <sub>PP</sub>	High supply voltage	-	150	200	V	---
V <sub>EN</sub>	EN input voltage range	1.8	-	5.0	V	---
V <sub>PT</sub>	Input positive threshold	-	-	70	%	Percent of V <sub>EN</sub> voltage
V <sub>NT</sub>	Input negative threshold	30	-	-	%	Percent of V <sub>EN</sub> voltage
V <sub>HY</sub>	Input threshold hysteresis	9.0	-	30	%	Percent of V <sub>EN</sub> voltage
I <sub>DDQ</sub>	V <sub>DD</sub> quiescent current, EN=0	-	140	-	µA	---
I <sub>D DEN</sub>	V <sub>DD</sub> average current	-	6.0	-	mA	INA = INB = 0 (measured)
I <sub>DD</sub>	V <sub>DD</sub> average current at 500KHz	-	57	-	mA	INA = INB = 500KHz 50%, G1~4 to S1~4 with four 1000pF load capacitors
R <sub>IN</sub>	Input logic impedance to GND	-	250	-	kΩ	---
C <sub>IN</sub>	Logic input capacitance	-	5.0	10	pF	---

## Gate Driver Outputs

Sym	Parameter	Min	Typ	Max	Units	Conditions
R <sub>HSC</sub>	Sourcing output resistance	-	5.0	-	Ω	I <sub>DS</sub> = 1.0A
R <sub>HSK</sub>	Sinking output resistance	-	5.0	-	Ω	I <sub>DS</sub> = 1.0A
R <sub>LSC</sub>	Sourcing output resistance	-	5.0	-	Ω	I <sub>DS</sub> = 1.0A
R <sub>LSK</sub>	Sinking output resistance	-	5.0	-	Ω	I <sub>DS</sub> = 1.0A

## Under Voltage and Over Current / Temperature Protection

(Over operating conditions, unless otherwise specified.  $V_{DD} = 12V$ ,  $V_{PP} = 200V$ ,  $T_A = 0$  to  $70^\circ C$ )

Sym	Parameter	Min	Typ	Max	Units	Conditions
$V_{OL\_OPF}$	OPF flag output low voltage	-	-	1.0	V	OPF = low, $I_{PULL\_UP} = 1.0mA$
$V_{PULL\_UP}$	Open drain pull-up voltage	-	-	15	V	$I_{OPF} = 1.0mA$
$I_{OPF}$	OPF sinking current limit	-	1.0	1.5	mA	---
$V_{UVT}$	$V_{DD}$ rising threshold	6.8	7.8	8.8	V	---
$V_{UVH}$	$V_{DD}$ UV hysteresis	-	0.6	-	V	---
$I_{RP1}, I_{RP3}$	High-side current reference	-	55	-	$\mu A$	---
$I_{RP2}$	Low-side current reference	-	55	-	$\mu A$	---
$V_{GS1-4}$	Gate sense voltage threshold	4.5	6.0	7.5	V	Reference to S1-4
$T_{OTP}$	Over-temperature threshold	95	110	120	$^\circ C$	If over temperature, OPF low and M1~4 off
$T_{OTH}$	Over-temperature hysteresis	-	7.0	-	$^\circ C$	---

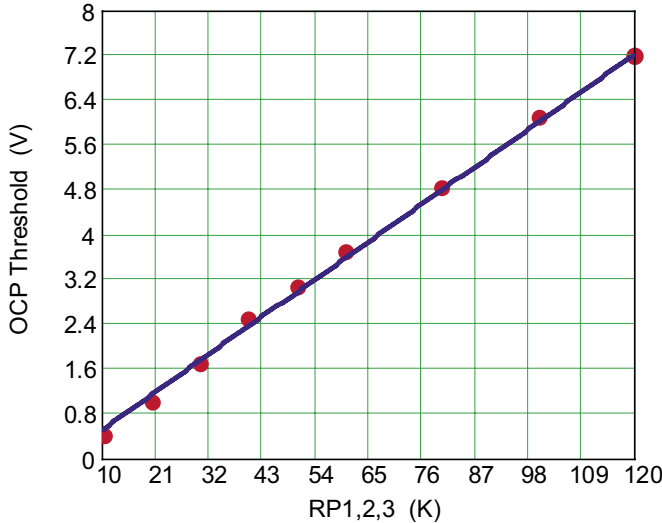
## AC Electrical Characteristics (Over operating conditions, unless otherwise specified. $V_{DD} = 12V$ , $V_{PP} = 200V$ , $T_A = 0$ to $70^\circ C$ )

Sym	Parameter	Min	Typ	Max	Units	Conditions
$f_S$	Switch frequency	-	-	1.0	MHz	---
$t_{dr}$	Switch on delay + dead time	-	35	-	ns	When $t_{dt} = \text{min}$
$t_{df}$	Switch off delay time	-	40	-	ns	See timing diagram
$t_r$	Output rise time	-	28	-	ns	With 1.0nF load
$t_f$	Output fall time	-	29	-	ns	With 1.0nF load
$t_{dm}$	Dead time matching	-	-	$\pm 5$	ns	Channel to channel
$\Delta t_{dtr}$	Dead time adjustable range	15	-	50	ns	RDT = 1.0k $\Omega$ to 200k $\Omega$
$\Delta t_{dta}$	Dead time accuracy	-	$\pm 5.0$	$\pm 10$	%	15ns to 50ns
THD	Total Harmonic Distortion	-	0.0007	-	%	Time jitter contribution, $f_j = 10Hz$ , $f_s = 500KHz$ , $f_A = 1.0KHz$
$t_{EN}$	Enable ready time	-	-	80	ns	See timing diagram
$t_{PWR\_UP}$	Power-up time	-	-	200	$\mu s$	See timing diagram

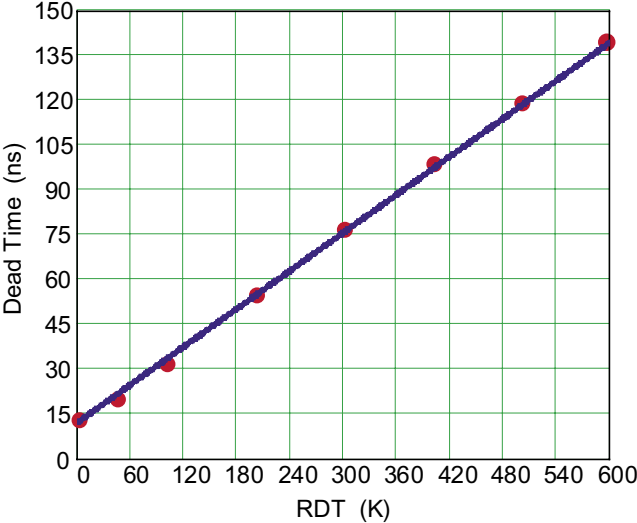
## Logic Table

Logic Input			Power MOSFET Output	
EN	INA	INB	A Bridge Output	B Bridge Output
1	0	0	L	L
1	0	1	L	H
1	1	0	H	L
1	1	1	H	H
0	X	X	Hi-Z	Hi-Z

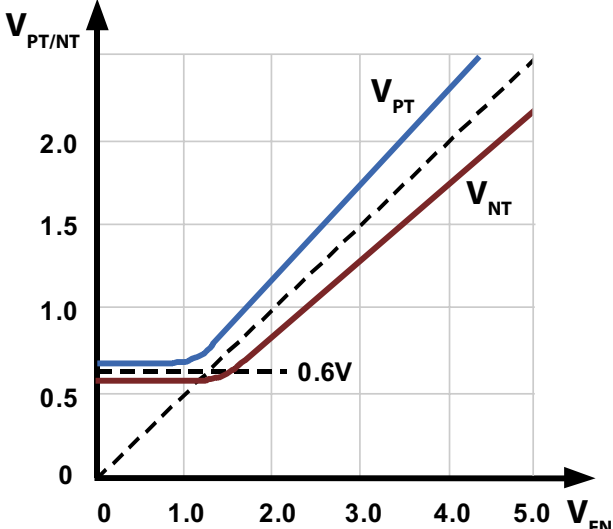
OCP Threshold vs RP1, 2, 3



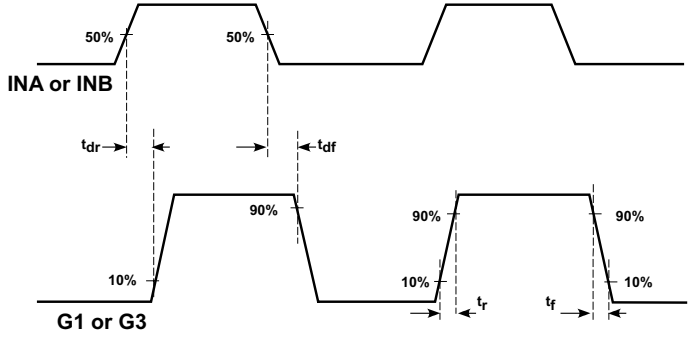
Dead Time vs RDT



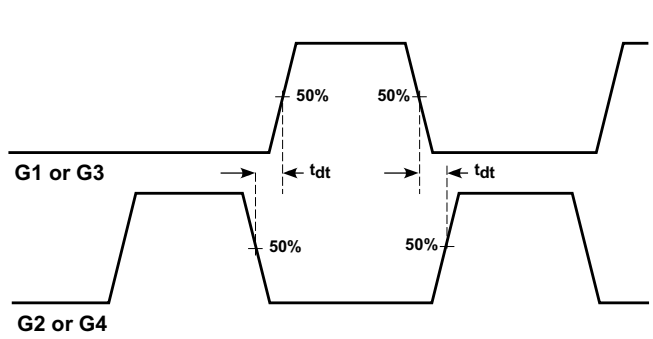
Logic  $V_{PT/NT} / V_{EN}$  Curve



Switch Timing Diagram



Adjustable Delay Time Diagram



## Pin Description

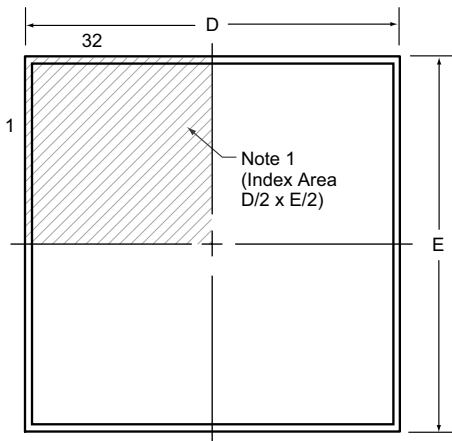
Pin #	Name	Function
1	GND	Logic signal ground.
2	AVDD	Logic AVDD voltage supply (+12V). Not connected to VDD1 or VDD2 internally.
3	INA	Input logic control of the half-bridge A output.
4	EN	Chip power enable, EN = Hi chip enabled, EN = Lo disabled, EN resets the OPF flag latch.
5	INB	Input logic control of the half-bridge B output.
6	OPF	Open drain output of over/under voltage, over current or temperature flag, Active = Low.
7	VSS	Return of voltage supply.
8	NC	Not connected.
9	RDT	Dead time program resistor.
10	S4	Low side MOSFET source.
11	G4	Low side MOSFET gate.
12	GS4	Low side MOSFET gate voltage sense.
13	VDD2	Positive voltage supply (+12V). May not connected to VDD1 internally.
14	NC	Not connected.
15	S3	High side MOSFET source.
16	G3	High side MOSFET gate.
17	GS3	High side MOSFET gate voltage sense.
18	BS3	High side boost external capacitor.
19	D3	High side MOSFET drain.
20	RP1	High side program resistor OCP threshold for MOSFET M1.
21	RP3	High side program resistor OCP threshold for MOSFET M3.
22	D1	High side MOSFET drain.
23	BS1	High side boost external capacitor.
24	GS1	High side MOSFET gate voltage sense.
25	G1	High side MOSFET gate.
26	S1	High side MOSFET source.
27	NC	Not connected.
28	VDD1	Positive voltage supply (+12V). May not connected to VDD2 internally.
29	GS2	Low side MOSFET gate voltage sense.
30	G2	Low side MOSFET gate.
31	S2	Low side MOSFET source.
32	RP2	Low side program resistor OCP threshold for MOSFET M2 and M4.

**Note:**

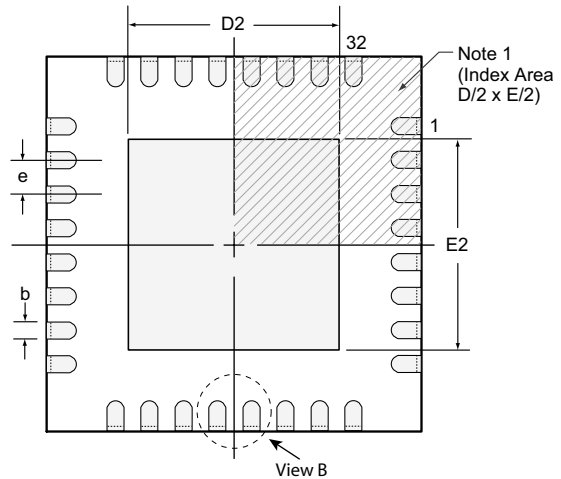
*The thermal pad must be connected to VSS externally.*

# 32-Lead QFN Package Outline (K6)

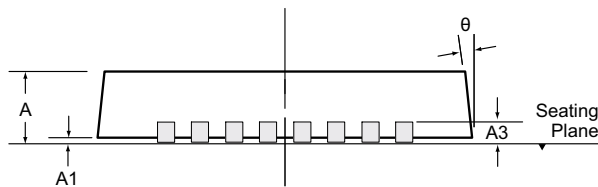
7x7mm body, 1.00mm height (max), 0.65mm pitch



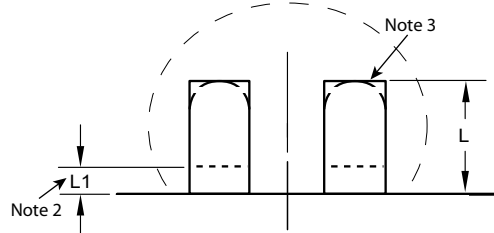
**Top View**



**Bottom View**



**Side View**



**View B**

**Notes:**

1. Details of Pin 1 identifier are optional, but must be located within the indicated area. The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.
2. Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.
3. The inner tip of the lead may be either rounded or square.

Symbol	A	A1	A3	b	D	D2	E	E2	e	L	L1	θ	
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.25	6.85	5.00*	6.85	5.00*	0.65 BSC	0.45*	0.00	0°
	NOM	0.90	0.02		0.30	7.00	5.51*	7.00	5.15*		0.55*	-	-
	MAX	1.00	0.05		0.35	7.15	5.25*	7.15	5.25*		0.65*	0.15	14°

JEDEC Registration MO-220, Variation VKKC-1, Issue K, June 2006

\* This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.

Drawings not to scale.

Supertex Doc. #: DSPD-32QFNK67X7P065, Version A061808

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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