DiskOnChip® DIMM Plus

Flash Disk with Protection and Security-Enabling Features

M-Systems
Flash Disk Pioneers

Highlights

DiskOnChip DIMM Plus is a member of M-Systems' growing family of DiskOnChip flash disk products. Based on M-Systems' award-winning DiskOnChip Millennium Plus, it packages the most advanced flash disk technology in an SO-DIMM form factor.

Using Toshiba's state-of-the-art 0.16µ NAND technology, DiskOnChip DIMM Plus features:

- Advanced protection and security-enabling features for data and code
- Proprietary TrueFFS® technology for full hard disk emulation, high data reliability and maximum flash lifetime
- Capacities ranging from 32Mbyte (256Mbit) to 128MByte (1,024Mbit)
- 144-pin SO-DIMM package
- NAND-based flash technology which enables high density and small die size
- Exceptional read, write and erase performance with a unique, full 16-bit bus flash interface
- Configurable for 8/16-bit bus interface
- Programmable Boot Block (1KB)
- Data integrity with Reed-Solomon Error Detection Code/Error Correction Code (EDC/ECC)
- Deep Power-Down mode for reduced power consumption
- 3.3 V power supply
- Software tools for programming, duplicating, testing and debugging
- Support for all major OSs, including VxWorks, Windows CE, Linux, pSOS, QNX, etc.

Performance

- Burst read/write speed: 20MB/sec
- Sustained write speed: 1.5MB/sec
- Sustained read speed: 3MB/sec

Protection and Security-Enabling Features

- Unique Identification (UID) number
- User-configurable One Time Programmable (OTP) area
- Two configurable write and read-protected partitions for data and boot code
- Two levels of hardware data and code protection: Protection Key and LOCK# signal

Boot Capability

- Programmable Boot Block (1KB) with eXecute In Place (XIP) capability to replace boot ROM
- Download Engine (DE) for automatic download of boot code
- Boot capabilities
  - Platform initialization
  - OS boot

Reliability

- On-the-fly Reed-Solomon Error Detection Code/Error Correction Code (EDC/ECC)
- Guaranteed data integrity after power failure
- Automatic bad block management
- Dynamic and static wear-leveling

Hardware Compatibility

- Simple, SRAM-like hardware interface
- Compatible with all major CPUs, including:
  - X86
  - Geode® SCxxxx
  - StrongARM
  - PowerPC™ MPC8xx
  - MediaGX
  - 68K
  - MIPS
  - SuperH™ SH-x
- 8-bit and 16-bit bus architecture support

TrueFFS Software

- Full hard-disk read/write emulation for transparent file system management
- Identical software for all DiskOnChip capacities
- Patented methods to extend flash lifetime, including:
  - Dynamic virtual mapping
  - Dynamic and static wear-leveling
- Support for all major OS environments, including:
  - Windows CE
  - Linux
  - VxWorks
  - Windows Embedded NT 4.0
  - BE
  - PSOS+
  - QNX
  - LynxOS
  - ATI Nucleus
  - DOS
- Support for OS-less environments
- Small 8KB memory window

Applications

- Internet set-top boxes, interactive TVs, web browsers
- WBT, thin clients, network computers
- Embedded systems
- Routers, switches, networking equipment
- Car PCs, automotive computing
- Point of sale (POS) terminals, industrial PCs
- Medical equipment
- PDAs and smart handsets

Power Requirements

- Operating voltage: 3.3V
- Current (Typical)
  - Active: 45mA
  - Deep Power-Down: 10-40µA (depending on capacity)

Capacity

- 32Mbyte (256Mbit) to 128MByte (1,024Mbit)

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1. Introduction

This data sheet includes the following sections:

Section 1: Overview of data sheet contents

Section 2: Product overview, including a brief product description, a pin diagram and signal descriptions

Section 3: Theory of operation for the major building blocks

Section 4: Hardware protection mechanism

Section 5: Modes of operation

Section 6: TrueFFS technology, including power failure management and 8Kbyte memory window

Section 7: Register description

Section 8: Using DiskOnChip DIMM Plus as a boot device

Section 9: Hardware and software design considerations

Section 10: Environmental, electrical, timing and product specifications

Section 11: Information on ordering DiskOnChip DIMM Plus

Appendix A: Example code to verify DiskOnChip DIMM Plus operation

To contact M-Systems' worldwide offices for general information and technical support, please see the listing on the back cover.

2. Product Overview

2.1 Product Description

DiskOnChip DIMM Plus is a member of M-Systems' DiskOnChip product series. DiskOnChip DIMM Plus provides a complete, easily integrated flash disk for highly reliable data and code storage. DiskOnChip DIMM Plus also offers advanced protection and security-enabling features for both data and code storage. Available in 144-pin SO-DIMM form factor, it is optimized for applications such as connected devices, set-top boxes, thin clients, network computers, telecommunication and embedded systems.

DiskOnChip DIMM Plus protection and security-enabling features offer a number of benefits. Two write and read-protected partitions, with both software and hardware-based protection, can be configured independently for maximum design flexibility. The Unique ID (UID) identifies each flash device, eliminating the need for a separate ID device (i.e. EEPROM) on the motherboard. The user-configurable One Time Programmable (OTP) area, written to once and then locked to prevent data and code from being altered, is ideal for storing customer and product-specific information.

DiskOnChip DIMM Plus is based on Toshiba's cutting-edge 0.16µ NAND flash technology. This technology enables DiskOnChip DIMM Plus to provide unmatched physical and performance-related benefits. It has the highest flash density in the smallest die size available on the market, for the best cost structure and the smallest real estate. Using 16-bit internal flash access, it features unrivaled write and read performance: 1.5MB/sec write and 3 MB/sec read.

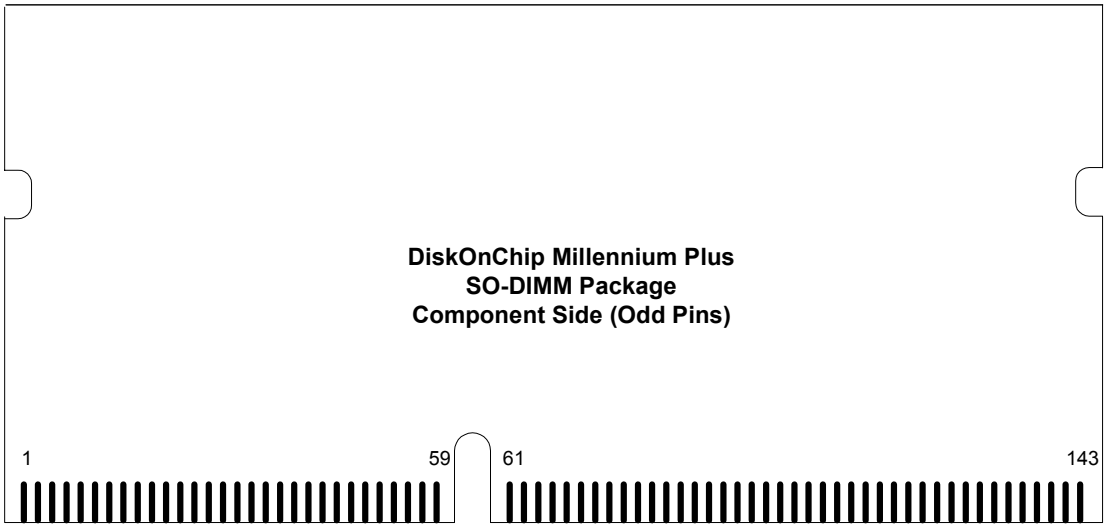
M-Systems' patented TrueFFS software technology fully emulates a hard disk to manage the files stored on DiskOnChip DIMM Plus. This transparent file system management enables read/write operations that are identical to a standard, sector-based hard disk. In addition, TrueFFS employs various patented methods, such as dynamic virtual mapping, dynamic and static wear-leveling, and automatic bad block management to ensure high data reliability and to maximize flash lifetime. TrueFFS binary drivers are available for a wide range of popular OSs, including VxWorks, Windows CE, Windows XP, Linux, pSOS, QNX. Customers developing for target platforms not supported by TrueFFS binary drivers can use the TrueFFS Software Development Kit (SDK). For customized boot solutions, M-Systems provides the Boot SDK.

DiskOnChip DIMM Plus is a cost-effective solution for code storage as well as data storage. A Programmable Boot Block with eXecute In Place (XIP) capability can store boot code, replacing the boot ROM to function as the only non-volatile memory on board. This reduces hardware expenditures and board real-estate. M-Systems' Download Engine (DE) is an automatic bootstrap mechanism that expands the functionality of the physical 1KB programmable boot block to enable system initialization from DiskOnChip.

DiskOnChip DIMM Plus is available in capacities ranging from 32Mbyte (256Mbit) to 128Mbyte (1,024Mbit). The same pinout is retained for all capacities, enabling an easy upgrade path and maximum design flexibility.

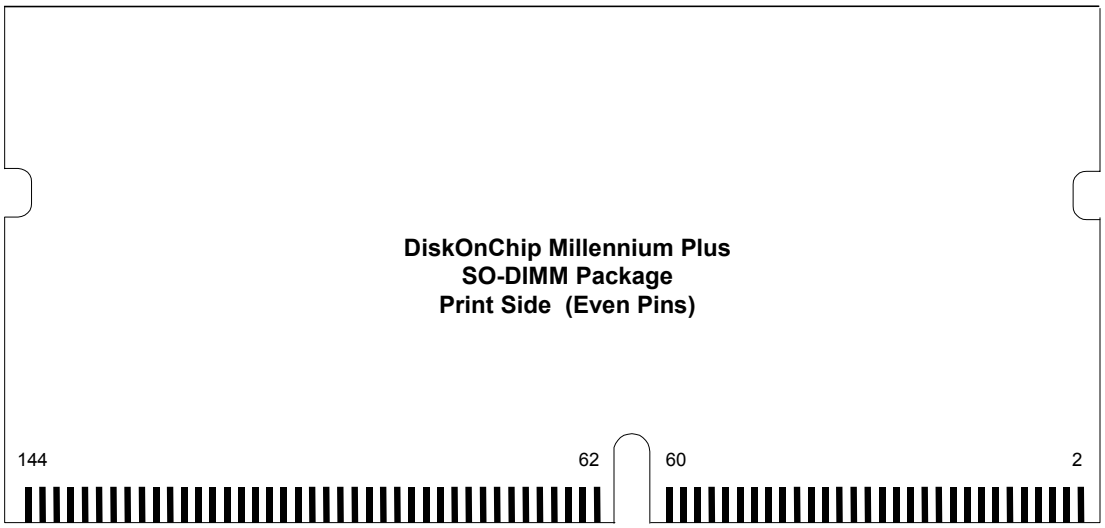
2.2 Pinout

See Figure 1 and Figure 2 for the DiskOnChip DIMM Plus pin diagram.



1	VSS	61	Reserved
3, 5, 7, 9	D[0:3]	63	VCC
11	VCC	65	RSTIN#
13, 15, 17, 19	D[4:7]	67	WE#
21	VSS	69	Reserved
23	CE#	71	Reserved1
25	Reserved	73	OE#
27	VCC	75	VSS
29, 31, 33	A[0:2]	77, 79	Reserved
35	VSS	81	VCC
37, 39, 41, 43	D[8:11]	83, 85, 87, 89	Reserved
45	VCC	91	VSS
47, 49, 51, 53	D[12:15]	93, 95, 97, 99	Reserved
55	VSS	101	VCC
57	Reserved	103, 105	A6, A8
59	BUSY#	107	VSS
		109.111	A9, A10
		113	VCC
		115, 117	Reserved
		119	VSS
		121, 123, 125, 127	Reserved
		129	VCC
		131, 133, 135, 137	Reserved
		139	VSS
		141	Reserved
		143	VCC

Figure 1: SO-DIMM Component Side (CS) Pinout



62	Reserved	2	VSS
64	VCC	4, 6, 8, 10	Reserved
66	BHE#	12	VCC
68	Reserved	14, 16, 18, 20	Reserved
70	IF_CFG	22	VSS
72	LOCK#	24, 26	Reserved
74	Reserved	28	VCC
76	VSS	30, 32, 34	A[3:5]
78, 80	Reserved	36	VSS
82	VCC	38, 40, 42, 44	Reserved
84, 86, 88, 90	Reserved	46	VCC
92	VSS	48, 50, 52, 54	Reserved
94, 96, 98, 100	Reserved	56	VSS
102	VCC	58, 60	Reserved
104, 106	A7, A11		
108	VSS		
110	A12		
112	Reserved		
114	VCC		
116, 118	Reserved		
120	VSS		
122, 124, 126, 128	Reserved		
130	VCC		
132, 134, 136, 138	Reserved		
140	VSS		
142	Reserved		
144	VCC		

Figure 2: SO-DIMM Print Side (PS) Pinout

2.3 System Interface

See Figure 3 for a simplified I/O diagram.

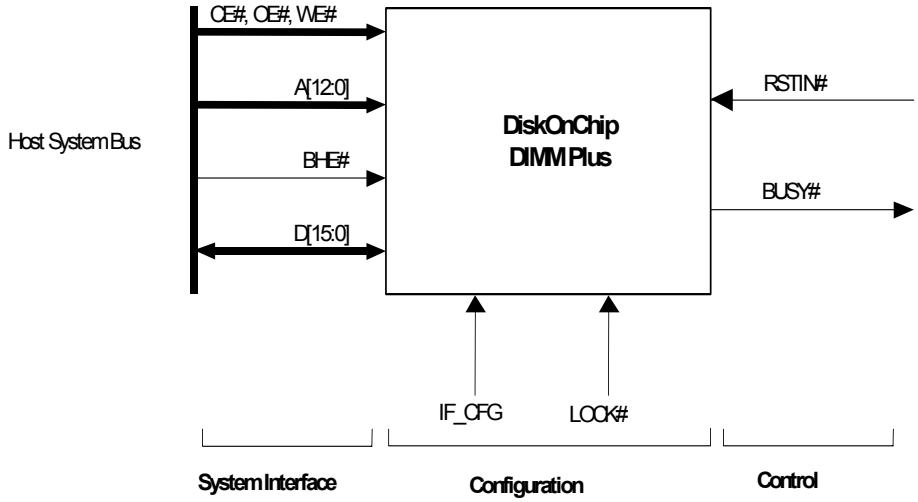


Figure 3: Simplified I/O Diagram

2.4 Signal Descriptions

Table 1 contains brief signal descriptions, presented in logic groups. The following abbreviations are used:

IN Standard (non-Schmidt) input
ST Schmidt Trigger input
OD Open drain
R8 Nominal 22 KOhm pull-up resistor, enabled only for 8-bit interface mode (IF_CFG input is 0)
R 3.7 MOhm nominal pull-up resistor

Table 1: Signal Description

Signal	Pin No.	Input Type	Description	Signal Type
System Interface				
A[12:0]	See Figure 1 and Figure 2	ST	Address bus	Input
BHE#	66	ST, R8	Byte High Enable, active low. When low, data transaction on D[15:8] is enabled. Not used and may be left floating when IF_CFG is set to 0 (8-bit mode). This signal is relevant only during boot phase.	Input
CE#	23	ST, R	Chip Enable, active low	Input
D[7:0]	See Figure 1 and Figure 2	IN	Data bus, low byte	Input/ Output
D[15:8]	See Figure 1 and Figure 2	IN, R8	Data bus, high byte. Not used and may be left floating when IF_CFG is set to 0 (8-bit mode).	Input
OE#	73	ST	Output Enable, active low	Input
WE#	67	ST	Write Enable, active low	Input
Configuration				
IF_CFG	70	ST	Interface Configuration, 1 for 16-bit interface mode, 0 for 8-bit interface mode.	Input
LOCK#	72	ST	Lock, active low. When active, provides full hardware data protection of selected partitions.	Input
Control				
BUSY#	59	OD	Busy, active low, open drain. Indicates that DiskOnChip is initializing and should not be accessed. A 10 KOhm pull-up resistor is required even if the pin is not used.	Output
RSTIN#	65	ST	Reset In, active low	Input
Power				
VCC	See Figure 1 and Figure 2	-	Device supply. All VCC pins must be connected.	Supply
VSS	See Figure 1 and Figure 2	-	Ground. All VSS pins must be connected.	Supply
Reserved				
Reserved	See Figure 1 and Figure 2	-	Pins not listed in this tabled are reserved, and must be left floating.	
Reserved1	71	-	Reserved signal. To insure minimum power consumption, a 10KΩ pull-up resistor is required.	

3. Theory of Operation

3.1 Overview

DiskOnChip DIMM Plus consists of the following major functional blocks, as shown in Figure 4:

- **System Interface** for host interface
- **Configuration Interface** for configuring the DiskOnChip to operate in 8/16 bit mode, and hardware write protection.
- **Protection and Security-Enabling block**, containing Write/Read protection and One-Time Programming (OTP), for advanced data/code security and protection
- Programmable **Boot Block** enhanced with a **Download Engine (DE)** for system initialization capability
- **Reed-Solomon Error Detection and Error Correction Code (EDC/ECC)** for on-the-fly error handling
- **Data Pipeline** through which the data flows from the host to the NAND flash arrays.
- **Control & Status** that contains registers responsible for transferring the address, data and control information between the TrueFFS driver and the flash media.
- **Flash Interface** and a 32MB interleaved dual-bank architecture consisting of **two embedded 16MB NAND flash arrays**
- **Bus Control** for translating the host bus address, data and control signals into valid NAND flash signals.
- **Address Decoder** to enable the relevant unit inside DiskOnChip controller, according to the address range received from the system interface.

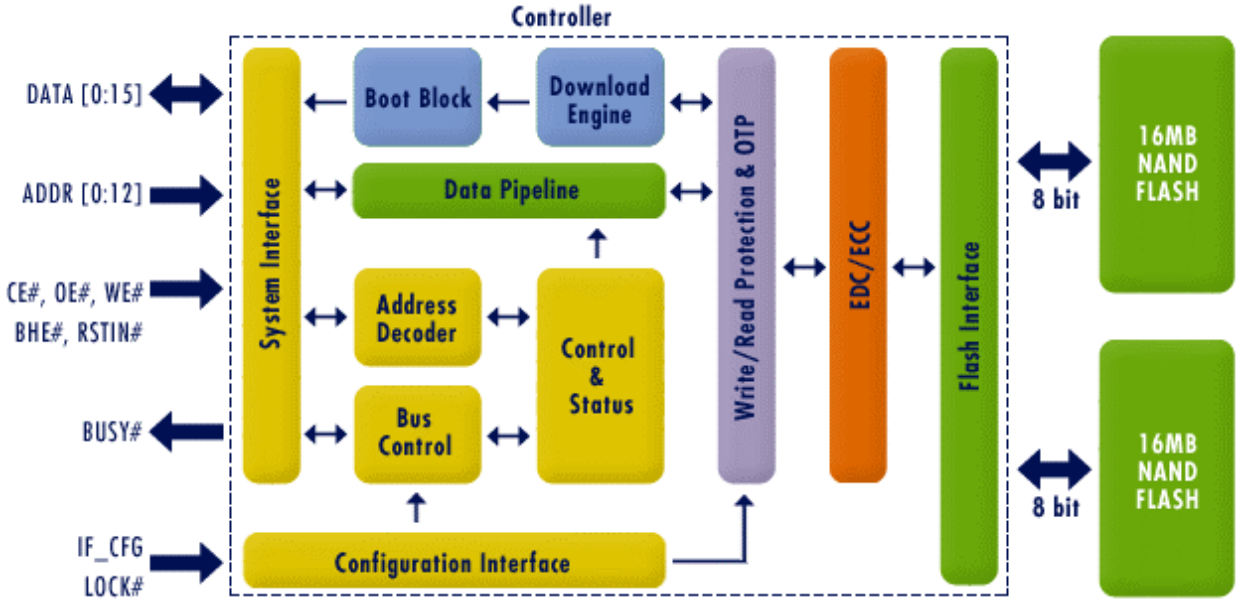


Figure 4: DiskOnChip DIMM Plus Simplified Block Diagram

3.2 System Interface

The system interface block provides an easy-to-integrate SRAM-like (also EEPROM-like) interface to DiskOnChip, enabling it to interface with various CPU interfaces, such as a local bus, ISA bus, SRAM interface, EEPROM interface or any other compatible interface. In addition, the EEPROM-like interface enables direct access to the Programmable Boot Block to permit XIP functionality during system initialization.

A 13-bit wide address bus enables access to the DiskOnChip 8KB memory window (as shown in section 6.2). The 16-bit data bus permits full 16-bit wide access to the flash, due to an internal, dual-bank, interleaved-operation architecture. With both internal and external 16-bit access, DiskOnChip DIMM Plus provides unrivaled performance.

The Chip Enable (CE#), Write Enable (WE#) and Output Enable (OE#) signals trigger read and write cycles. A write cycle occurs while both the CE# and the WE# inputs are asserted. Similarly, a read cycle occurs while both the CE# and OE# inputs are asserted. Note that DiskOnChip DIMM Plus does not require a clock signal. DiskOnChip features a unique analog static design, optimized for minimal power consumption. The CE#, WE# and OE# signals trigger the controller (e.g., system interface block, bus control and data pipeline) and flash access.

The Reset In (RSTIN#) and Busy (BUSY#) control signals are used in the reset phase. See section 5.2 for details.

DiskOnChip DIMM Plus contains several configuration signals. The Interface Configuration (IF_CFG) signal configures DiskOnChip for 16-bit or 8-bit mode of operation (see section 9.3.4). The Lock (LOCK#) signal enables hard-wire hardware-controlled protection of code and data, as described below on protection and security-enabling features.

3.3 Configuration Interface

The Configuration Interface block enables the designer to configure the DiskOnChip to operate in certain modes. The IF_CFG pin is used to configure the device for 8/16 bit access mode and the LOCK# pin is used for hardware write/read protection.

3.4 Protection and Security-Enabling Features

The Protection and Security-Enabling block, consisting of read/write protection, Unique ID and OTP area, enables advanced data and code security and protection. Located on the main route of traffic between the host and the flash, this block monitors and controls all data and code transactions to and from DiskOnChip.

3.4.1 Read/Write Protection

Data and code protection is implemented through a Protection State Machine (PSM). The user can configure one or two independently programmable areas of the flash memory as read protected, write protected, or read/write protected.

A Protection Area may be protected by either/both of these hardware mechanisms:

- 64-bit Protection Key
- Hard-wired LOCK# signal

The size and location of each area is user-defined to provide maximum flexibility for the target platform and application requirements.

The configuration parameters of the protected areas are stored on the flash media and are automatically downloaded from the flash to the PSM upon power-up, to enable robust protection throughout the flash lifetime.

In the event of an attempt to bypass the protection mechanism, illegally modify the protection key or in any way sabotage the configuration parameters, the entire DiskOnChip becomes both read and write protected, and is completely inaccessible.

For further information on the hardware protection mechanism, refer to section 4.

3.4.2 Unique Identification (UID) Number

Each DiskOnChip DIMM Plus is assigned a 16-byte UID number. Burned onto the flash during production, the UID cannot be altered and is unique worldwide. The UID is essential in security-related applications, and can be used to identify end-user products in order to fight fraudulent duplication by imitators.

The UID on DiskOnChip DIMM Plus eliminates the need for an additional on-board ID device, such as a dedicated EEPROM.

3.4.3 One-Time Programmable (OTP) Area

The 6 KByte OTP area is user-programmable for complete customization. The user can write to this area once, after which it is automatically locked permanently. After it is locked, the OTP area becomes read only, just like a ROM device.

Typically, the OTP area is used to store customer and product information such as: product ID, software version, production data, customer ID and tracking information.

3.5 Programmable Boot Block with XIP Capability

During boot, code must be executed directly from the flash media, rather than first copied to the host RAM and then executed from there. This direct XIP code execution capability is essential for booting.

The Programmable Boot Block with XIP capability enables DiskOnChip DIMM Plus to act as a boot ROM device in addition to being a flash disk. This unique design enables the user to benefit from the advantages of NOR flash, typically used for boot and code storage, and NAND flash, typically used for data storage. No other boot device is required on the motherboard.

The Programmable Boot Block on DiskOnChip consists of 1KB of programmable SRAM. The Download Engine (DE) described in the next section expands the functionality of this block by copying the boot code from the flash into the internal SRAM.

3.6 Download Engine (DE)

Upon power up or when the RSTIN# signal is asserted, the DE automatically downloads the Initial Program Loader from page 3 of the third block on the flash to the Programmable Boot Block. The Initial Program Loader (IPL) is responsible for starting the booting process. The download process is fairly quick and is designed so that when the CPU accesses DiskOnChip for code execution, the IPL code is already located in the internal SRAM in the Programmable Boot Block.

In addition, the DE downloads the Data Protection Structures (DPS) from the flash to the Protection State Machines, so that DiskOnChip is secure and protected from the first moment it is active.

During the download process, the DiskOnChip DIMM Plus asserts the BUSY# pin to indicate to the system that it is not yet ready to be accessed. Once the BUSY# pin is negated, the system can access the DiskOnChip.

A failsafe mechanism prevents improper initialization due to a faulty VCC or invalid assertion of the RSTIN# input. Another failsafe mechanism is designed to overcome possible NAND flash data errors. It prevents internal registers from powering up in a state that bypasses the intended data protection. In addition, in any attempt to sabotage the data structures the entire DiskOnChip will turn both read and write protected and will be completely inaccessible.

3.7 Error Detection Code/Error Correction Code (EDC/ECC)

NAND flash, being an imperfect memory, requires error handling. DiskOnChip DIMM Plus implements Reed-Solomon Error Detection Code (EDC). A hardware-generated, 6-byte error detection signature is computed each time a page (512 Bytes) is written to or read from DiskOnChip.

The TrueFFS driver implements complementary Error Correction Code (ECC). Unlike error detection, which is required on every cycle, error correction is relatively seldom required, hence implemented in software. The

combination of DiskOnChip built-in EDC mechanism and the TrueFFS driver ensures highly reliable error detection and correction, while providing maximum performance.

The following detection and correction capability is provided for each 512 Bytes:

- Corrects up to two 10-bit symbols, including two random bit errors.
- Corrects single bursts up to 11 bits.
- Detects single bursts up to 31 bits and double bursts up to 11 bits.
- Detects up to 4 random bit errors.

3.8 Data Pipeline

DiskOnChip DIMM Plus uses a two-stage pipeline mechanism, designed for maximum performance while enabling on-the-fly data manipulation, such as read/write protection and Error Detection/Error Correction.

For more information on this mechanism, refer to technical note *TN-DOC-014 Pipeline Mechanism in DiskOnChip*.

3.9 Control and Status

The Control and Status block contains registers responsible for transferring the address, data and control information between the DiskOnChip TrueFFS driver and the flash media. Additional registers are used to monitor the status of the flash media (ready/busy) and of the DiskOnChip controller. For further information on the DiskOnChip DIMM Plus registers, refer to section 7).

3.10 Flash Architecture

3.10.1 Two Banks of 16MB NAND Flash

DiskOnChip DIMM Plus is designed with a dual-bank interleave architecture consisting of two banks of 16MB NAND flash, using 0.16µ flash technology. The interleave architecture allows 16-byte flash access instead of the standard 8-byte flash access, thereby providing double the performance for read, write and erase operations.

3.10.2 Internal Architecture

Each of the two 16MB flash banks consists of 1024 pages organized in 32 blocks, as follows:

- **Page** – Each page contains 512 bytes of user data and a 16-byte extra area used to store flash management and EDC/ECC signature data, as shown in Figure 5. A page is the minimal unit for read/write operations.
- **Block** – Each block contains 32 pages (total of 16KB), as shown in Figure 6. A block is the minimal unit that can be erased, and is sometimes referred to as an erase block.

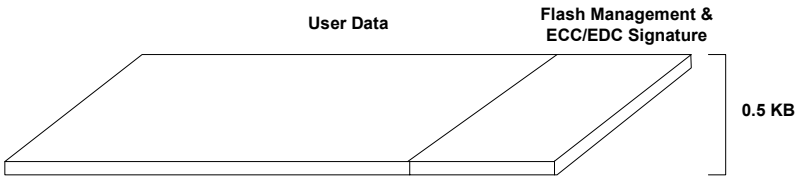


Figure 5: Page Structure

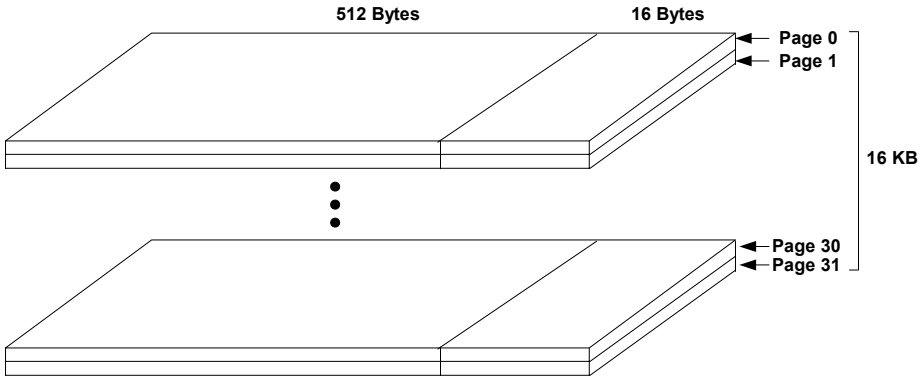


Figure 6: Block Structure

Because of its interleave architecture, DiskOnChip DIMM Plus consists of 1024 dual pages organized in 32 dual blocks, for a total capacity of 32MB, as shown in Figure 7.

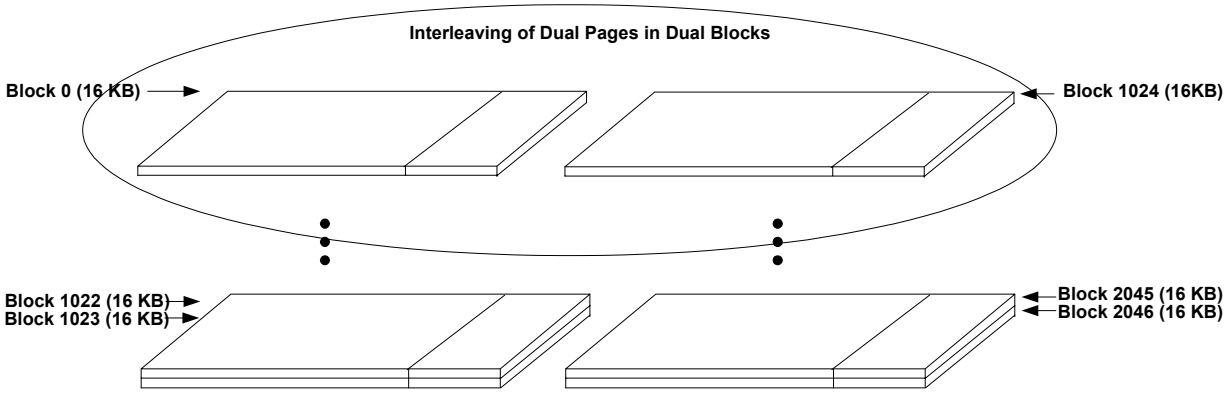


Figure 7: Interleave Architecture Structure

4. Hardware Protection

4.1 Method of Operation

DiskOnChip DIMM Plus enables the user to define two partitions that are protected (in hardware) against any combination of read or write operations. The two protected areas can be configured as read protected or write-protected, and are protected by a protection key (i.e. password) defined by the user. Each of the protected areas can be configured separately and can function separately, providing maximal flexibility for the user.

The size and protection attributes (protection key/read/write/changeable/lock) of the protected partition are defined in the media formatting stage (DFORMAT utility or the format function in the TrueFFS SDK).

In order to set or remove a read/write protection, the protection key (i.e., password) must be used, as follows:

- Insert the protection key to remove read/write protection.
- Remove the protection key to set read/write protection.

DiskOnChip DIMM Plus has an additional hardware safety measurement. If the Lock option is enabled (by means of software) and the LOCK# pin is asserted, the protected partition has an additional hardware lock that prevents read/write access to the partition, even with the use of the correct protection key. The LOCK# pin must be asserted during DFORMAT (and later when the partition is defined as changeable) to enable the additional hardware safety lock.

Note: The target volume (i.e. partition) does not have to be mounted before calling a hardware protection routine.

Only one partition can be defined as “changeable”; i.e., its password and attributes are fully configurable at any time (from read to write, both or none and vise versa). Note that “un-changeable” partition attributes cannot be changed unless the media is reformatted.

A change of any of the protection attributes causes a reset of the protection mechanism and consequently the removal of *all* device protection keys. That is, if the protection attributes of one partition are changed, the other partition will lose its key-protected read/write protection.

The only way to read or write from a read or write protected partition is to use the insert key call (even DFORMAT does not remove the protection). This is also true for modifying its attributes (key, read, write and lock enable state). Read/write protection is disabled in each one of the following events:

- Power-down
- Change of any protection attribute (not necessarily in the same partition)
- Write operation to the IPL area
- Removal of the protection key.

For further information on hardware protection, please refer to *TrueFFS SDK User Manual* or application note *AP-DOC-057 Protection and Security-Enabling Features in DiskOnChip Millennium Plus.*

4.2 Low Level Structure of Protected Area

The first three blocks on DiskOnChip DIMM Plus contain foundry information, the Data Protect structures, Initial Program Loader (IPL) code, and bad block mapping information. See Figure 8.

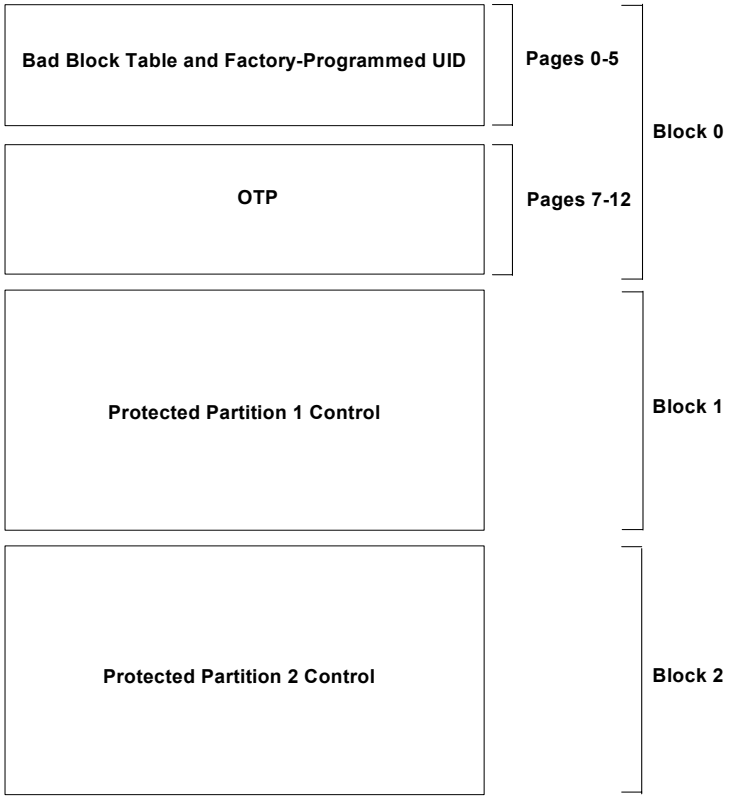


Figure 8: Low Level Format DiskOnChip DIMM Plus

Blocks 0, 1 and 2 in DiskOnChip DIMM Plus contain the following information:

Block 0

- Bad Block Table (page 2). Contains the mapping information to unusable Erase units on the flash media.
- UID (16 bytes). This number is written during the manufacturing stage, and cannot be altered at a later time.
- One Time Programming (OTP) area (pages 7-12). The OTP area is written once and then locked.

Block 1

- Data Protect Structure 0. This structure contains configuration information on one of the two user-defined protected partitions.

Block 2

- Data Protect Structure 1. This structure contains configuration information on one of the two user-defined protected partitions.
- IPL Code (1KB). This is the boot code that is downloaded by the DE to the internal boot block.

5. Modes of Operation

DiskOnChip DIMM Plus has three modes of operation:

- Reset
- Normal
- Deep Power-Down.

Mode changes can occur due to any of the following events, as shown in Figure 9:

- Assertion of the RSTIN# signal sets the device in Reset mode.
- During Power-Up boot detector circuitry sets the device into Reset mode.
- A valid write sequence to the DiskOnChip DIMM Plus Control register and the Control Confirmation register sets the device in Normal mode.
- Power down
- A valid write sequence, initiated by software sets the device from Normal Mode into Deep Power Down Mode and vice versa.

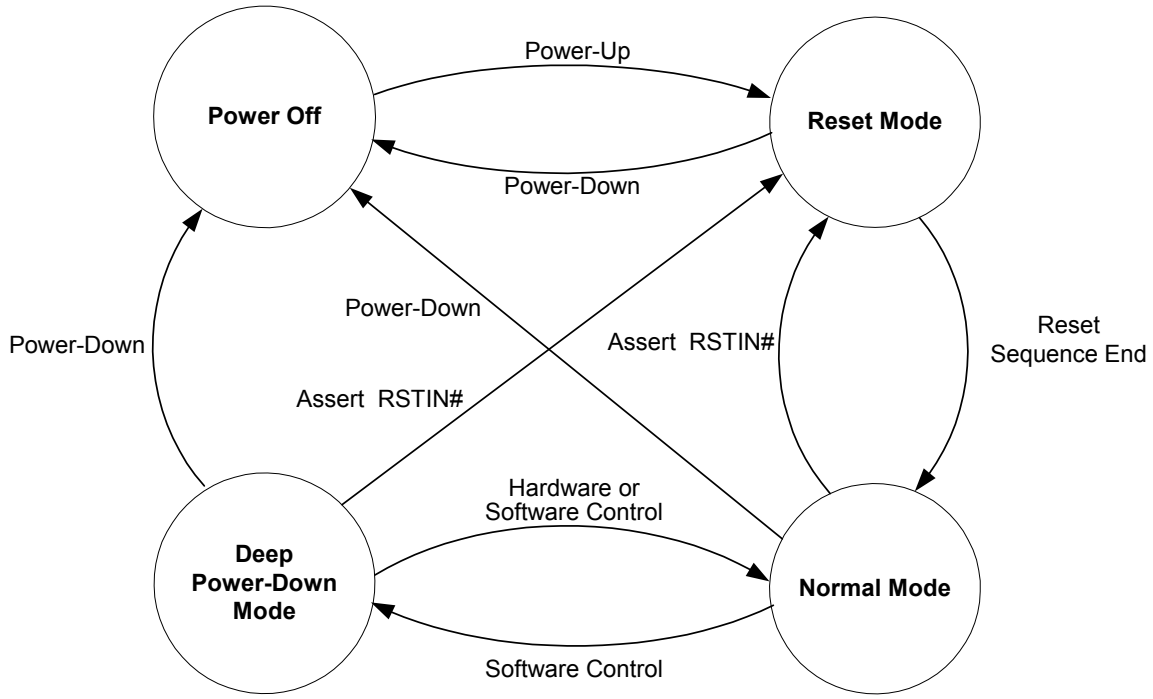


Figure 9: Operation Modes and Related Events

5.1 Normal Mode

This is the mode in which standard operations involving the flash memory are performed. Normal mode is automatically entered when a valid write sequence is sent to the DiskOnChip Control register and Control Confirmation register.

A write cycle occurs when both the CE# and WE# inputs are asserted. Similarly, a read cycle occurs when both the CE# and OE# inputs are asserted. Because the flash controller generates its internal clock from these CPU cycles and some read operations return volatile data, it is essential that the specified timing requirements contained in

section 10.4.1 be met. It is also essential that read and write cycles are not interrupted by glitches or ringing on the CE#, WE#, OE# address inputs.

Note: All inputs to DiskOnChip DIMM Plus are Schmidt trigger types to improve noise immunity.

In normal mode, DiskOnChip DIMM Plus responds to every valid hardware cycle. When there is no activity, power consumption automatically drops to a typical standby current of 400µA.

5.2 Reset Mode

In Reset mode, DiskOnChip DIMM Plus ignores all write cycles, except for those to the DiskOnChip Control register and Control Confirmation register. All register read cycles return a value of 00H.

Before attempting to perform a register read operation, the device is set to Normal mode by TrueFFS software.

5.3 Deep Power-Down Mode

In Deep Power-Down mode, DiskOnChip DIMM Plus internal high current voltage regulators are disabled to reduce quiescent power consumption. The following signals are also disabled in this mode: input buffers A[12:0], BHE#, WE#, D[15:0] and OE# (when CE# is negated).

To enter Deep Power-Down mode, a proper sequence must be written to the DiskOnChip. In Deep Power-Down mode, write cycles have no effect and read cycles return indeterminate data (DiskOnChip DIMM Plus does not drive the data bus). Entering Deep Power-Down mode and then returning to the previous mode does not affect the value of any register.

To exit Deep Power-Down mode, perform the following sequence:

- Read any address (1FFFH is suggested) three times. The data returned is undefined. The regulators are enabled at the beginning of the first cycle. The input buffers (A[12:0], BHE#, WE#, D[15:0] and OE#) are enabled at the end of the third cycle.
- Read the selected address one more time (data returned is still undefined).

Applications that require both Deep Power-Down mode and boot detection require BIOS support to ensure that DiskOnChip DIMM Plus exits from Power-Down mode prior to the expansion ROM scan. Similarly, applications that use DiskOnChip DIMM Plus as a boot ROM must ensure that the device is *not* in Deep Power-Down mode before reading the boot vector/instructions, either by pulsing RSTIN# to the asserted state and waiting for the BUSY# output to be negated, or by entering Reset mode via software.

6. TrueFFS Technology

6.1 General Description

M-Systems' patented TrueFFS technology was designed to maximize the benefits of flash memory while overcoming inherent flash limitations that would otherwise reduce its performance, reliability and lifetime. TrueFFS emulates a hard disk, making it completely transparent to the OS. In addition, since it operates under the OS file system layer (see Figure 10), it is completely transparent to the application.

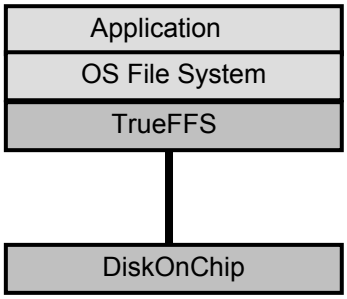


Figure 10: TrueFFS Location in System Hierarchy

TrueFFS technology support includes:

- Binary driver support for all major OSs
- TrueFFS Software Development Kit (TrueFFS SDK)
- Boot Software Development Kit (Boot SDK)
- Support for all major CPUs, including 8, 16 and 32-bit bus architectures

TrueFFS technology features:

- Block device API
- Flash file system management
- Bad block management
- Dynamic virtual mapping
- Dynamic and static wear-leveling
- Power failure management
- Implementation of Reed-Solomon EDC/ECC
- Performance optimization
- Compatible with all DiskOnChip products

6.1.1 Built-in Operating System Support

The TrueFFS driver is integrated into all major OSs including: Windows CE, NT, NT Embedded, XP, Linux (various kernels), VxWorks, Nucleus, pSOS, QNX, DOS, BE, LynxOS, EPOC and others. For a complete listing of all available drivers, please refer to M-Systems' web site http://www.m-sys.com. It is advised to use the latest driver versions that can be downloaded from the DiskOnChip DIMM Plus web page on the M-Systems' site.

6.1.2 TrueFFS Software Development Kit (SDK)

The basic TrueFFS Software Development Kit (SDK) provides the source code of the TrueFFS driver. It can be used in an OS-less environment or when special customization of the driver is required for proprietary OSs.

When using DiskOnChip DIMM Plus as the boot replacement device, TrueFFS SDK also incorporates in its source code the Boot SDK, software that is required for this configuration (this package is also available separately). Please refer to installation manual *IM-DOC-020 Boot SDK* for further information on the usage of this software package.

6.1.3 File Management

TrueFFS accesses the flash memory within DiskOnChip DIMM Plus through an 8KB window in the CPU memory space. It provides block device API, by using standard file system calls, identical to those used by a mechanical hard disk, to enable reading from and writing to any sector on DiskOnChip. This makes it compatible with any file system and file system utilities such as diagnostic tools and applications. When using the Flash Allocation Table (FAT) file system, the data stored on DiskOnChip uses FAT-16.

Note: Please note that DiskOnChip DIMM Plus is shipped unformatted and contains virgin media.

6.1.4 Bad Block Management

Since NAND flash is an imperfect storage media, it contains some bad blocks that cannot be used for storage because of their high error rates. TrueFFS automatically detects and maps bad blocks upon system initialization, ensuring that they are not used for storage. This management process is completely transparent to the user, who remains unaware of the existence and location of bad blocks, while remaining confident of the integrity of data stored.

6.1.5 Wear-Leveling

Flash memory can be erased a limited number of times. This number is called the *erase cycle limit* or *write endurance limit* and is defined by the flash array vendor. The erase cycle limit applies to each individual erase block in the flash device. In DiskOnChip DIMM Plus, the erase cycle limit of the flash is 100,00 erase cycles. This means that after approximately 100,00 erase cycles, the erase block begins to make storage errors at a rate significantly higher than the error rate that is typical to the flash.

In a typical application and especially if a file system is used, a specific page or pages are constantly updated (e.g., the page/s that contain the FAT, registry etc.). Without any special handling, these pages would wear out more rapidly than other pages, reducing the lifetime of the entire flash.

To overcome this inherent deficiency, TrueFFS uses M-Systems patented wear-leveling algorithm. The wear-leveling algorithm ensures that consecutive writes of a specific sector are not written physically to the same page in the flash. This spreads flash media usage evenly across all pages, thereby maximizing flash lifetime. TrueFFS wear-leveling extends the flash lifetime 10 to 15 years beyond the lifetime of a typical application.

Dynamic Wear-Leveling

TrueFFS uses statistical allocation to perform dynamic wear-leveling on newly written data. This not only minimizes the number of erase cycles per block, it also minimizes the total number of erase cycles. Because a block erase is the most time-consuming operation, dynamic wear-leveling has a major impact on overall performance. This impact cannot be noticed during the first write to flash (since there is no need to erase blocks beforehand), but it is more and more noticeable as the flash media becomes full.

Static Wear-Leveling

Areas on the flash media may contain static files, characterized by blocks of data that remain unchanged for very long periods of time, or even for the whole device lifetime. If wear-leveling were only applied on newly written pages, static areas would never be cycled. This limited application of wear-leveling would lower life expectancy significantly in cases where flash memory contains large static areas. To overcome this problem, TrueFFS forces data transfer in static areas as well as in dynamic areas, thereby applying wear-leveling to the entire media.

6.1.6 Power Failure Management

TrueFFS uses algorithms based on “erase after write” instead of "erase before write" to ensure data integrity during normal operation and in the event of a power failure. Used areas are reclaimed for erasing and writing the flash management information into them only *after* an operation is complete. This procedure serves as a check on data integrity.

The “erase after write” algorithm is also used to update and store mapping information on the flash memory. This keeps the mapping information coherent even during power failures. The only mapping information held in RAM is a table pointing to the location of the actual mapping information. This table is reconstructed during power-up or after reset from the information stored in the flash memory.

To prevent data from being lost or corrupted, TrueFFS uses the following mechanisms:

- When writing, copying, or erasing the flash device, the data format remains valid at all intermediate stages. Previous data is never erased until the operation has been completed and the new data has been verified.
- A data sector cannot exist in a partially written state. Either the operation is successfully completed, in which case the new sector contents are valid, or the operation has not yet been completed or has failed, in which case the old sector contents remain valid.

6.1.7 Error Detection/Correction

TrueFFS implements a Reed-Solomon Error Correction Code (ECC) algorithm to ensure data reliability. Refer to section 3.5 for further information on the EDC/ECC mechanism.

6.1.8 Special Features through I/O Control (IOCTL) Mechanism

In addition to standard storage device functionality, the TrueFFS driver provides extended functionality. This functionality goes beyond simple data storage capabilities to include features such as: format the media, read/write protect, binary partition(s) access, flash defragmentation and other options. This unique functionality is available in all TrueFFS-based drivers through the standard I/O control command of the native file system.

For further information, please refer to application note *AP-DOC-046 Extended Functions of TrueFFS Driver for DiskOnChip.*

6.1.9 Compatibility

The TrueFFS driver supports all released DiskOnChip products. Upgrading from one product to another requires no additional software integration.

When using different drivers (e.g. TrueFFS SDK, Boot SDK, BIOS extension firmware, etc.) to access DiskOnChip DIMM Plus, the user must verify that all software is based on the same code base version. It is also important to use only tools (e.g. DFORMAT, DINFO, GETIMAGE, etc.) derived from the same version as the firmware version and the TrueFFS drivers used in the application. Failure to do so may lead to unexpected results, such as lost or corrupted data. The driver and firmware version can be verified by the sign-on messages displayed, or by the version information stored in the driver or tool.

Note: When a new M-Systems’ DiskOnChip product with new features is released, a new TrueFFS version is required.

6.2 8KB Memory Window

TrueFFS utilizes an 8KB memory window in the CPU address space, consisting of four 2KB sections as depicted in Figure 11. When in Reset mode, read cycles from sections 1 and 2 always return the value 00H to create a fixed and known checksum. When in Normal mode, these two sections are used for the internal registers. The 1K Programmable Boot Block is aliased twice, in section 0 and section 3, to support systems that search for a checksum at the boot stage both from the top and bottom of memory. The addresses described here are relative to the absolute starting address of the 8KB memory window.

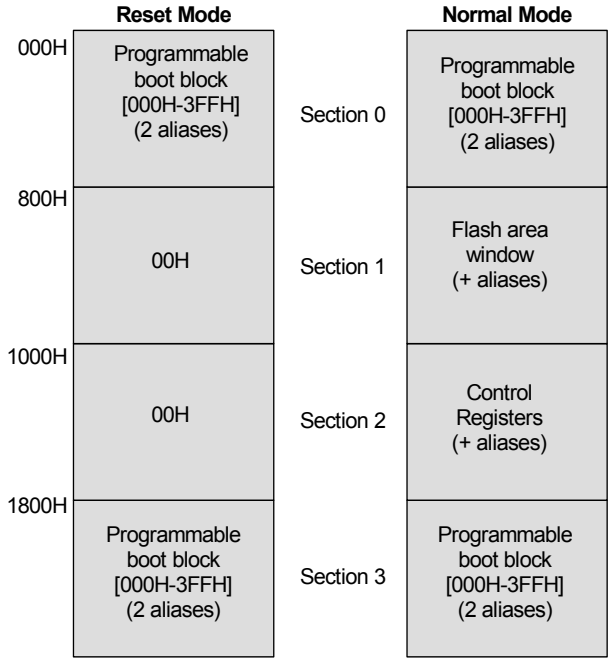


Figure 11: DiskOnChip DIMM Plus Memory Map

7. Register Descriptions

This section describes various DiskOnChip DIMM Plus registers and their functions, as listed in Table 2. This section can be used to enable the designer to better evaluate DiskOnChip technology.

Table 2: DiskOnChip DIMM Plus Registers

Address (Hex)	Register Name
1000	Chip Identification (ID)
1002	No Operation (NOP)
1004	Alias Resolution
1006	DiskOnChip Control
1046	Toggle Bit
1076	DiskOnChip Control Confirmation

7.1 Definition of Terms

The following abbreviations and terms are used within this section:

RFU Reserved for future use. This bit is undefined during a read cycle and "don't care" during a write cycle.

RFU_0 Reserved for future use; when read, this bit always returns the value 0; when written, software should ensure that this bit is always set to 0.

RFU_1 Reserved for future use; when read, this bit always returns the value 1; when written, software should ensure that this bit is always set to 1.

Reset Value Refers to the value immediately present after exiting from Reset mode to Normal mode.

7.2 Reset Values

All registers return the value 00H while in Reset mode. The Reset value that is written in the register description is the register value after exiting from Reset mode and entering Normal mode. Please note that the contents of some registers are undefined at that time (N/A).

7.3 Chip Identification (ID) Register

Description: This register is used to identify the device residing on the host platform. This register always returns the value 40H when read.

Address (hex): 1000

Type: Read only

Reset Value: 40H

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
40H							

7.4 No Operation (NOP) Register

Description: A call to this register results in no operation. To aid in code readability and documentation, it is recommended that software access this register when performing cycles intended to create a time delay.

Address (hex): 1002

Type: Write

Reset Value: None

7.5 Alias Resolution Register

Description: This register enables software to identify multiple DiskOnChip DIMM Plus devices or multiple aliases in the CPUs memory space. Data written is stored but does not affect the behavior of DiskOnChip DIMM Plus.

Address (hex): 1004

Type: Read/Write

Reset Value: 00H

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D[7:0]							

Bit No.	Description
0-7	D[7:0]: Data bits

7.6 DiskOnChip Control Register/Control Confirmation Register

Description: These two registers are identical and contain information on the operation mode of DiskOnChip. After writing the required value to the DiskOnChip Control register, the complement of that data byte must also be written to the Control Confirmation register. The two writes cycles must not be separated by any other read or write cycles to DiskOnChip DIMM Plus memory space, except for reads from the Programmable Boot Block space.

Address (hex): 1006/1076

Type: Read/Write

Reset Value: 10H

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU_0		RFU_0	RST_LAT	BDET	MDWREN	Mode[1:0]	

Bit No.	Description
0-1	Mode. These bits select the mode of operation, as follows: 00: Reset 01: Normal 10: Deep Power-Down
2	MDWREN (Mode Write Enable). This bit must be set to 1 before changing the mode of operation.
3	BDET (Boot Detect). This bit is set whenever the device has entered Reset Mode as a result of the Boot Detector triggering. It is cleared by writing a 1 to this bit.
4	RST_LAT (Reset Latch). This bit is set whenever the device has entered the Reset Mode as a result of the RSTIN# input signal being asserted or the internal voltage detector triggering. It is cleared by writing a 1 to this bit.
5-7	Reserved for future use

7.7 Toggle Bit Register

Description: This register controls the Reed-Solomon ECC logic.

Address (hex): 1046

Type: Read/Write (except for bits 2 and 7 which are Read Only)

Reset Value: 82H

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ERROR	RFU	ECC_RW	RFU_0	ECC_EN	TOGGLE	RFU_1	IGNORE

Bit No.	Description
0	IGNORE. When set to a 1, data read from or written to the Flash Data register is not processed by the ECC unit.
1, 4, 6	Reserved for future use
2	TOGGLE. This read only bit toggles on consecutive reads and serves to identify the presence of the device.
3	ECC_EN (ECC Enable). 0: Resets the ECC logic and reloads the ECC Syndrome Register[5:0] with their Reset values. 1: Enables the Reed-Solomon ECC and parity generators, allowing new data to be clocked into the ECC unit.
5	ECC_RW (ECC Read/Write). 0: The ECC unit is in 'Read Mode'. In this mode, a block of data and the 6-byte syndrome are read from flash memory into the ECC unit and are checked for errors. The status of the error detection process is indicated by the state of the ERROR bit. 1: The ECC unit is put into 'Write Mode', where a block of data (512 bytes) is passed through the ECC unit as it is written into the flash memory. At the end of this pass, TrueFFS reads the 6-byte syndrome from the ECC Control Register and writes it into the flash.
7	ERROR. This bit is read only. After reading a block of data and six ECC syndrome bytes, this bit should be examined. 0: No error detected 1: Error detected

8. Booting from DiskOnChip DIMM Plus

8.1 Introduction

DiskOnChip DIMM Plus can function both as a flash disk and the system boot device.

If DiskOnChip is configured as a flash disk, it can operate as the OS boot device. DiskOnChip default firmware contains drivers to enable it to perform as the OS boot device under DOS (see section 8.2). For other OSs, please refer to the *readme* file of the TrueFFS driver.

If DiskOnChip DIMM Plus is configured as a flash disk and as the system boot device, it contains the boot loader, an OS image and a file system. In such a configuration, DiskOnChip DIMM Plus can serve as the only non-volatile device on board. Refer to section 8.3.2 for further information on boot replacement.

8.2 Boot Procedure in PC Compatible Platforms

When used in PC compatible platforms, DiskOnChip DIMM Plus is connected to an 8KB memory window in the BIOS expansion memory range, typically located between 0C8000H to 0EFFFFH. During the boot process, the BIOS loads the TrueFFS firmware into the PC memory and installs DiskOnChip as a disk drive in the system. When the operating system is loaded, DiskOnChip is recognized as a standard disk. No external software is required to boot from DiskOnChip.

Figure 12 illustrates the location of the DiskOnChip DIMM Plus memory window in the PC memory map.

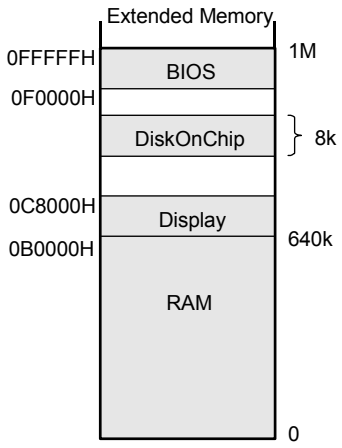


Figure 12: DiskOnChip DIMM Plus Memory Window in PC Memory Map

After reset, the BIOS code first executes the Power On Self-Test (POST) and then searches for all expansion ROM devices. When DiskOnChip DIMM Plus is found, the BIOS code executes from it the IPL (Initial Program Loader) code, located in the XIP portion of the Programmable Boot Block. This code loads the TrueFFS driver into system memory, installs DiskOnChip DIMM Plus as a disk in the system, and then returns control to the BIOS code. The operating system subsequently identifies DiskOnChip DIMM Plus as an available disk. TrueFFS responds by emulating a hard disk.

From this point onward, DiskOnChip DIMM Plus appears as a standard disk drive. It is assigned a drive letter and can be used by any application, without any modifications to either the BIOS set-up or the autoexec.bat/ config.sys files. DiskOnChip DIMM Plus can be used as the only disk in the system, with or without a floppy drive, and with or without hard disks. The drive letter assigned depends on how DiskOnChip DIMM Plus is used in the system, as follows:

- If DiskOnChip DIMM Plus is used as the only disk in the system, the system boots directly from it and assigns it drive C.
- If DiskOnChip DIMM Plus is used with other disks in the system:
  - DiskOnChip DIMM Plus can be configured as the last drive (the default configuration). The system assigns drive C to the hard disk and drive D to DiskOnChip DIMM Plus.
  - Alternatively, DiskOnChip DIMM Plus can be configured as the system's first drive. The system assigns drive D to the hard disk and drive C to DiskOnChip DIMM Plus.
- If DiskOnChip DIMM Plus is used as the OS boot device when configured as drive C, it must be formatted as a bootable device by copying the OS files onto it. This is done by using the SYS command when running DOS.

8.3 Boot Replacement

8.3.1 PC Architectures

In current PC architectures, the first CPU fetch (after reset is negated) is mapped to the boot device area, also known as the *reset vector*. The reset vector in PC architectures is located at address FFFF0, by using a Jump command to the beginning of the BIOS chip (usually F0000 or E0000). The CPU executes the BIOS code, initializes the hardware and loads DiskOnChip DIMM Plus software using the BIOS expansion search routine (e.g. D0000). Refer to section 8.2 for a detailed explanation on the boot sequence in PC compatible platforms.

DiskOnChip DIMM Plus implements both disk and boot functions when it replaces the BIOS chip. To enable this, DiskOnChip DIMM Plus requires a location at two different addresses:

- After power-up, DiskOnChip DIMM Plus must be mapped in F segment, so that the CPU fetches the reset vector from address FFFF0, where DiskOnChip DIMM Plus is located.
- After the BIOS code is loaded into RAM and starts execution, DiskOnChip DIMM Plus must be reconfigured to be located in the BIOS expansion search area (e.g. D0000) so it can load the TrueFFS software.

This means that the CS# signal must be remapped between two different addresses. For further information on how to achieve this, refer to application note *AP-DOC-047 Designing DiskOnChip as a Flash Disk & Boot Device Replacement*.

8.3.2 Non-PC Architectures

In non-PC architectures, the boot code is executed from a boot ROM, and the drivers are usually loaded from the storage device.

When using DiskOnChip DIMM Plus as the system boot device, the CPU fetches the first instructions from the DiskOnChip DIMM Plus Programmable Boot Block, which contains the IPL. Since in most cases this block cannot hold the entire boot loader, the Initial Program Loader (IPL) runs minimum initialization, after which the Secondary Program Loader (SPL) is copied to RAM from flash. The remainder of the boot loader code then runs from RAM.

The IPL and SPL are located in a separate (binary) partition on DiskOnChip DIMM Plus, and can be hardware protected if required.

For further information on software boot code implementation, refer to application note *AP-DOC-070 Writing an IPL for DiskOnChip Millennium Plus.*

9. Design Considerations

9.1 Design Environment

DiskOnChip DIMM Plus provides a complete design environment consisting of:

- Evaluation Boards (EVB) for enabling software integration and development with DiskOnChip DIMM Plus, even before the target platform is available. An EVB with DiskOnChip DIMM Plus soldered on it is available with an ISA standard connector and a PCI standard connector for immediate plug and play usage.
- Programming solutions
  - GANG programmer
  - Programming house
  - On-board programming
- TrueFFS Software Development Kit (SDK) and Boot SDK
- DOS Utilities
  - DFORMAT
  - GETIMG/PUTIMG
  - DLOWLVL
- Documentation
  - Data Sheet
  - Application Notes
  - Technical Notes
  - Articles
  - White Papers

Please visit M-Systems website (www.m-sys.com) for the most updated documentation, utilities and drivers.

9.2 System Interface

9.2.1 Typical Design

DiskOnChip DIMM Plus uses an SRAM-like interface that can easily be connected to any microprocessor bus. It requires 13 address lines, 8 data lines and basic memory control signals (CE#, OE#, WE#), as shown in Figure 13 below. Typically, DiskOnChip DIMM Plus can be mapped to any free 8KB memory space. In a PC compatible platform, it is usually mapped into the BIOS expansion area. If the allocated memory window is larger than 8KB, an automatic anti-aliasing mechanism prevents the firmware from being loaded more than once during the ROM expansion search.

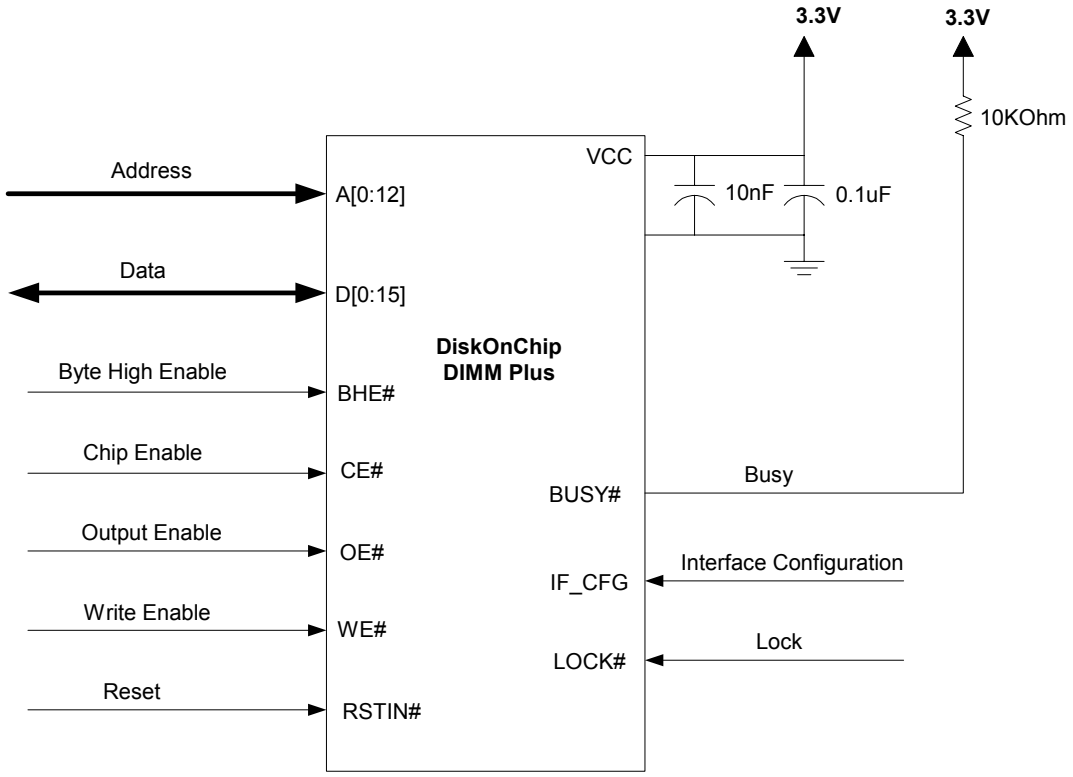


Figure 13: Typical System Interface

Notes: 1. The 0.1µF and the 10nF low-inductance high-frequency capacitors must be attached to each of the device's VCC and GND pins. These capacitors must be placed as close as possible to the package leads.

2. DiskOnChip DIMM Plus is an edge-sensitive device. CE#, OE# and WE# should be properly terminated (according to board layout, serial parallel or both terminations) to avoid signal ringing.

9.2.2 Connecting Signals

DiskOnChip DIMM Plus uses standard SRAM-like control signals, which should be connected as follows:

- Address (A[12:0]) – Connect these signals to the host address bus.
- Data (D[15:0]) – Connect these signals to the host data bus.
- Write (WE#) and Output Enable (OE#) – Connect these signals to the host WR# and RD# signals, respectively.
- Chip Enable (CE#) – Connect this signal to the memory address decoder.
- Power-On Reset In (RSTIN#) – Connect this signal to the host Power-On Reset signal.
- Busy (BUSY#) – Connect this signal to an input port. It indicates when the device is ready for first access after reset.
- Byte High Enable (BHE#) – This signal definition is compatible with 16 bit platforms that use the BHE#/BLE# protocol. See section 8.3.4. This signal is only relevant during the boot phase.
- Hardware Lock (LOCK#) – This signal prevents the use of the Write Protect Key to disable the protection.
- 8/16 bit Configuration (IF_CFG) – This signal is required for configuring the device for 8 or 16-bit access mode. When negated, the device is configured for 8-bit access mode. When asserted, 16-bit access mode is operative.

DiskOnChip DIMM Plus derives its internal clock signal from the CE#, OE# and WE# inputs. Since access to DiskOnChip DIMM Plus' registers is volatile, much like a FIFO or UART, ensure that these signals have clean rising and falling edges, and are free from ringing that can be interpreted as multiple edges. PC board traces for these three signals must either be kept short or properly terminated to guarantee proper operation.

9.3 Platform-Specific Issues

The following section describes hardware design issues.

9.3.1 Wait State

Wait states can be implemented only when DiskOnChip DIMM Plus is designed in a bus that supports a Wait state insertion, and supplies a WAIT signal.

9.3.2 Big and Little Endian Structures

PowerPC, ARM, and other RISC processors can use either Big or Little Endian structures. The DiskOnChip is a Little Endian device. Therefore bytes D[7:0] are its Least Significant Byte (LSB) and bytes D[15:8] are its Most Significant Byte (MSB). Within the bytes, bit D0 and bit D8 are the least significant bits of their respective byte. When connecting the DiskOnChip to a Big Endian device, make sure to that the bytes of the CPU and the DiskOnChip match.

Note: Processors, such as the PowerPC, also change the bit ordering within the bytes. Failing to follow these rules will result in improper connection of the DiskOnChip and will prevent the TrueFFS driver from identifying the DiskOnChip.

9.3.3 Busy Signal

The Busy signal (BUSY#) indicates that DiskOnChip DIMM Plus has not yet completed internal initialization. After reset, BUSY# is asserted while the IPL is downloaded into the internal SRAM and the Data Protection Structures (DPS) are downloaded to the Protection State Machines. Once the download process is completed, BUSY# is negated. It can be used to delay the first access to DiskOnChip DIMM Plus until it is ready to accept valid cycles.

Note: The TrueFFS driver does NOT use this signal to indicate that the flash is in busy state (e.g. program, read, or erase).

9.3.4 8-Bit/16-Bit Bus Width Interface

DiskOnChip DIMM Plus can be configured for either 8-bit or 16-bit bus operations via the IF_CFG signal.

8-Bit (Byte) Data Access Mode

When configured for 8-bit operation, IF_CFG should be negated. Data should then be driven only on the low data bus signals D[7:0]. D[15:8] and BHE# are internally pulled up and may be left floating.

16-Bit (Word) Data Access Mode

When configured for 16-bit operation, IF_CFG should be asserted. The following definition is compatible with 16-bit platforms using the BHE#/BLE# protocol:

- When the hosts' BLE# signal asserts DiskOnChip A[0], data is valid on D[7:0].
- When the hosts' BHE# signal asserts DiskOnChip BHE#, data is valid on D[15:8].
- When both A[0] and BHE# are at logic 0, data is valid on D[15:0].
- No data is transferred when both BHE# and A[0] are logic 1.
- 16-bit hosts that do not support byte transfers may hardwire the A[0] and BHE# inputs to logic 0.

Table 3 shows the active data bus lanes in 16-bit configuration.

Table 3: Active Data Bus Lanes in 16-bit Configuration

Inputs		Data Bus Activity		Transfer Type
BHE#	A0	D[7:0]	D[15:8]	
0	0	✓	✓	Word
0	1		✓	Odd Byte
1	0	✓		Even Byte
1	1			No operation

TrueFFS Driver Modifications

TrueFFS supports a wide range of OSs (see section 6.1.1). The TrueFFS driver is set to work in 8-bit data access mode as the default. To support 16-bit data access modes and their related memory window allocations, TrueFFS must be modified. In Windows CE and Windows NT-Embedded, these changes can be implemented through the Registry Entries. In all other cases, some minor customization is required in the driver. Please refer to the Installation Manual of each specific driver for further information.

10. Product Specifications

10.1 Environmental Specifications

10.1.1 Operating Temperature Ranges

Commercial Temperature Range: 0°C to 70°C

Extended Temperature Range: -40°C to +85°C

10.1.2 Thermal Characteristics

Table 4: Thermal Characteristics

Thermal Resistance (°C/W)	
Junction to Case (θ_{JC}): 30	Junction to Ambient (θ_{JA}): 85

10.1.3 Humidity

10% to 90% relative, non-condensing

10.1.4 Endurance

DiskOnChip DIMM Plus is based upon NAND flash technology, which has a limited number of erase cycles. The TrueFFS wear-leveling algorithm significantly enhances the endurance of the flash, increasing the expected life span by an order of magnitude. Refer to the life span calculator available on M-Systems' web site (www.m-sys.com) for more information.

10.2 Disk Capacity

Table 5: Disk Capacity (in Bytes)

DOS 6.22		VxWorks	
Formatted Capacity	**Sectors**	**Formatted Capacity**	**Sectors**
32,800,768	64,064	32,724,992	63,916
65,601,536	128,128	65,634,304	128,192
98,402,304	192,192	98,467,840	192,320
131,203,072	256,256	131,301,376	256,448

10.3 Electrical Specifications

10.3.1 Absolute Maximum Ratings

Table 6: Absolute Maximum Ratings

Parameter	Symbol	Rating[1]	Units	Notes
DC supply voltage	V_{CC}	-0.6 to 4.6	V	
Input pin voltage[2]	V_{IN}	-0.6 to Vcc+0.3	V	
Input pin current	I_{IN}	-10 to 10	mA	25°C
Storage temperature	T_{STG}	-55 to 150	°C	
Lead temperature	T_{LEAD}	260	° C	10 sec

1. Permanent device damage may occur if absolute maximum ratings are exceeded. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The voltage on any pin may undershoot to -2.0V or overshoot to 6.6V for less than 20ns.

10.3.2 Capacitance

Table 7: Capacitance

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V			10	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V			10	pF

Capacitance is not 100% tested.

10.3.3 DC Electrical Characteristics

Table 8: DC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
System Supply Voltage	V_{CC}		2.7	3.3	3.6	V
High-level Input Voltage	V_{IH}		2.1			V
Low-level Input Voltage	V_{IL}				0.7	V
High-level Output Voltage	V_{OH}	I_{OH} = -8mA;	2.4			V
Low-level Output Voltage	V_{OL}	I_{OL} = 8mA			0.4	V
Input Leakage Current [1,2]	I_{IL}				±10	µA
Output Leakage Current	I_{OZ}				±10	µA
Active Supply Current[3]	I_{CC}	8-bit; Cycle time = 100ns		25	45	mA
		16-bit; Cycle time = 100ns		25	45	
Standby Supply Current	I_{CCS}	Deep power-down mode CE# > V_{CC} – 0.2 All other input 0V or V_{CC}		10	40	µA
		Non power-down mode or CE# =V_{CC} All other inputs 0V or V_{CC}		400	600	µA

1. The CE# input includes a pull-up resistor which sources 0.3 ~ 1.4 µA at Vin = 0V.
2. The D[15:8] and BHE# inputs each include a pull-up resistor which sources 58 ~ 234 µA at Vin = 0V when IF_CFG is logic '0'.
3. VCC = 3.3V, outputs open.

10.3.4 AC Characteristics

Environmental and timing specifications are based on the following conditions.

Table 9: AC Test Conditions

Parameter	Value	Unit
Ambient Temperature (T_A)	-40 °C to +85 °C	°C
Supply Voltage (VCC)	2.7 to 3.6	V
Input Pulse Levels	0 to 2.7	V
Input Rise and Fall Times	3	ns
Input Timing Levels	1.5	V
Output Load (VCCQ = 2.7 to 3.6V)	100	pF

10.4 Timing Specifications

10.4.1 Read Cycle Timing

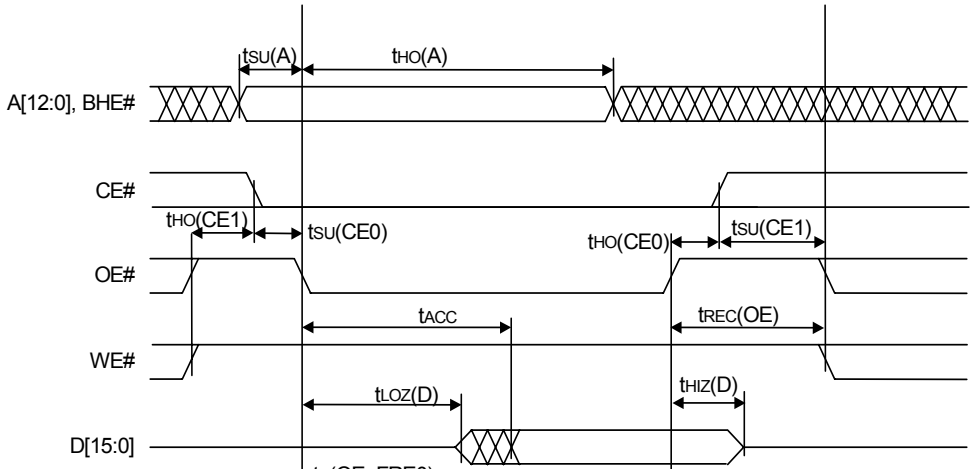


Figure 14: Read Cycle Timing

Table 10: Read Cycle Timing Definitions

Symbol	Description	2.7V - 3.6V		Units
		Min	Max	
Tsu(A)	Address to OE# ↓ setup time	10		ns
THO(A)	OE# ↓ to Address hold time	28		ns
TSU(CE0)[1]	CE# ↓ to OE# ↓ setup time	—		ns
THO(CE0)[2]	OE# ↑ to CE# ↑ hold time	—		ns
THO(CE1)	OE# or WE# ↑ to CE# ↓ hold time	6		ns
TSU(CE1)	CE# ↑ to WE# ↓ or OE# ↓ setup time	6		ns
TREC(OE)	OE# negated to start of next cycle	20		ns
TACC	Read access time (RAM)[3,4]		103	ns
	Read access time (all other addresses)[3]		85	ns
TLOZ(D)	OE# ↓ to D driven	10		ns
THIZ(D)	OE# ↑ to D Hi-Z delay		25	ns

1. CE# may be asserted any time before or after OE# is asserted. If CE# is asserted after OE#, all timing relative to when OE# was asserted will be referenced to the time CE# was asserted.
2. CE# may be negated any time before or after OE# is negated. If CE# is negated before OE#, all timing relative to when OE# was negated will be referenced to the time CE# was negated.
3. The boot block is located at addresses 0000~07FFH and 1800H~1FFFH. Registers located at addresses 0800H~17FFH have a faster access time than the boot block. Access to the boot block is not required after the boot process has completed.
4. Systems that do not access the boot block may implement only the read access timing for “all other registers”. This will increase the systems performance, however it will prevent access to the boot block.

10.4.2 Write Cycle Timing

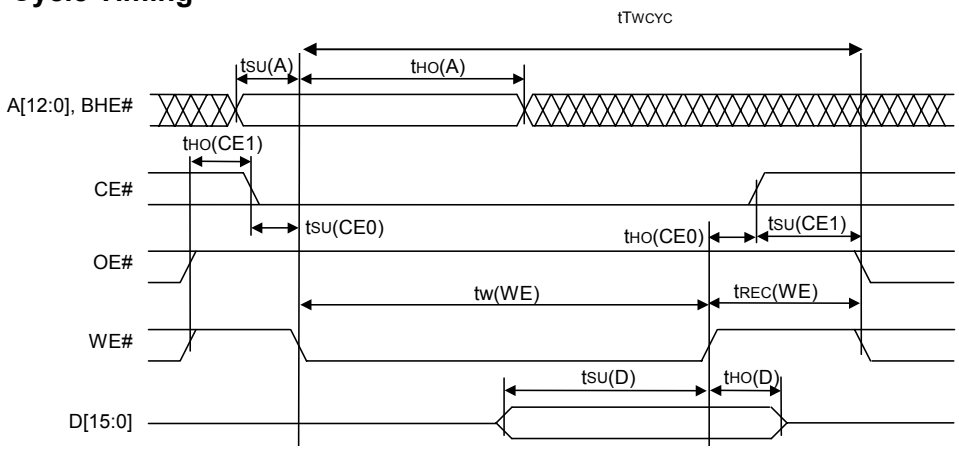


Figure 15: Write Cycle Timing

Table 11: Write Cycle Timing Definitions

Symbol	Description	2.7V - 3.6V		Units
		Min	Max	
tSU (A)	Address to WE# ↓ setup time	10		ns
tHO (A)	WE# ↓ to Address hold time	28		ns
tW(WE)	WE# asserted width (RAM	46		ns
	WE# asserted width (all other addresses)	47		
Twcyc	Write Cycle Time	80		ns
tSU (CE0)[1]	CE# ↓ to WE# ↓ setup time	—		ns
tHO (CE0)[2]	WE# ↑ to CE# ↑ hold time	—		ns
tHO (CE1)	OE# or WE# ↑ to CE# ↓ hold time	6		ns
tSU (CE1)	CE# ↑ to WE# ↓ or OE# ↓ setup time	6		ns
tREC (WE)	WE# ↑ to start of next cycle	20		ns
tSU(D)	D to WE# ↑ setup time	51		ns
tHO (D)	WE# ↑ to D hold time	0		ns

1. CE# may be asserted any time before or after WE# is asserted. If CE# is asserted after WE#, all timing relative to WE# asserted should be referenced to the time CE# was asserted.
2. CE# may be negated any time before or after WE# is negated. If CE# is negated before WE#, all timing relative to WE# negated will be referenced to the time CE# was negated.

10.4.3 Power-Up Timing

DiskOnChip DIMM Plus is reset by assertion of the RSTIN# input. When this signal is asserted, DiskOnChip initiates a download procedure from the flash memory into the internal XIP of the Programmable Boot Block. During this procedure, DiskOnChip DIMM Plus does not respond to read or write accesses.

Host systems that boot from DiskOnChip DIMM Plus must employ either option c below or another method to guarantee the required timing of the first access. All other host systems can employ any of the following methods to guarantee first-access timing requirements:

a. Use a software loop to wait at least Tp (BUSY1) before accessing the device after the reset signal is negated.

b. Poll the state of the BUSY# output.

c. Use the BUSY# output to hold the host CPU in wait state before completing the first access.

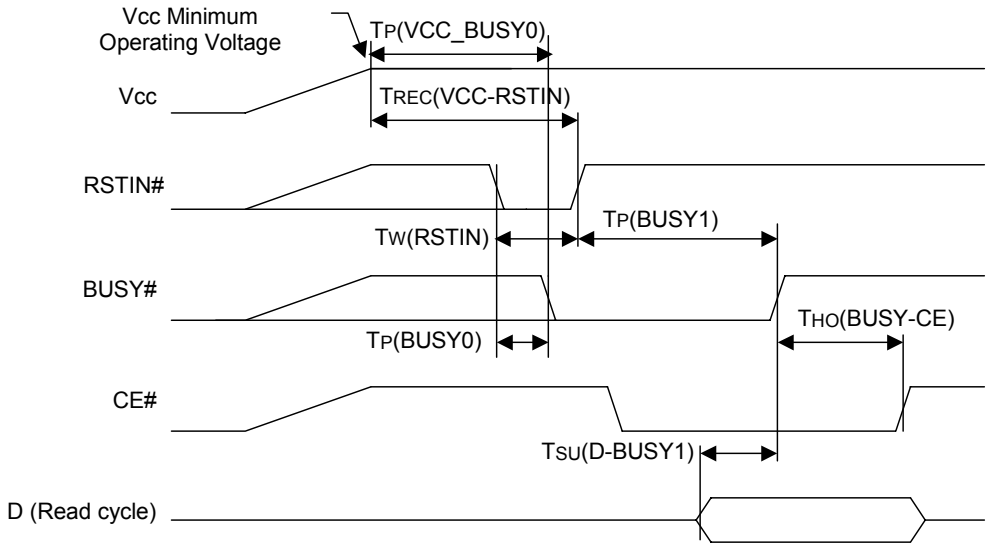


Figure 16: Reset Timing

Table 12: Power Up Timing Definitions

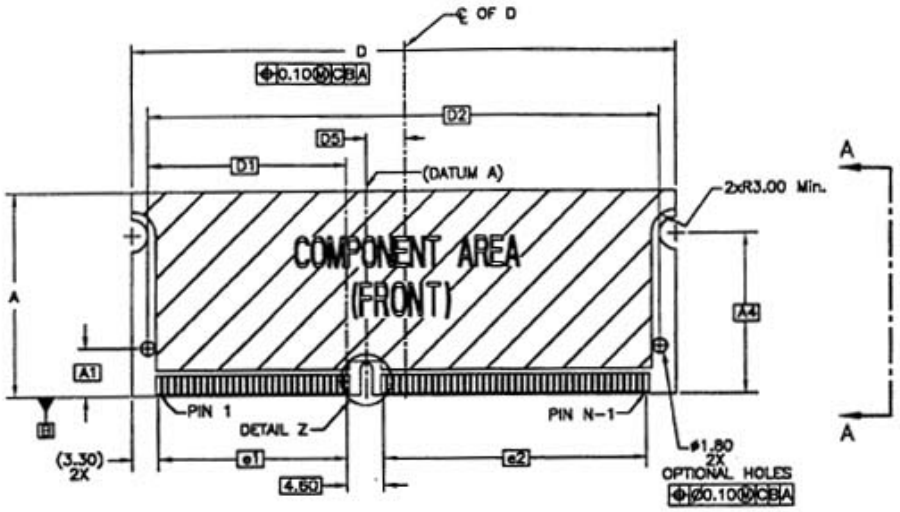
Symbol)	Description	Min	Max	Units
TREC (VCC-RSTIN)[1]	VCC stable to RSTIN# ↑	500		µs
Tp (VCC-BUSY0)[1]	VCC stable to BUSY# ↓		500	µs
TW (RSTIN)	RSTIN# asserted pulse width	30		ns
TP (BUSY0)	RSTIN# ↓ to BUSY# ↓		50	ns
TP (BUSY1)[2]	RSTIN# ↑ to BUSY# ↑		1.3	ms
THO (BUSY-CE)[3]	BUSY# ↑ to CE# ↑	0		ns
TSU (D-BUSY1)[3]	Data valid to BUSY# ↑	0		ns

1. Specified from the final positive crossing of Vcc above 2.7V.

2. If the assertion of RSTIN# occurs during a flash erase cycle, this time could be extended by up to 500µS.

3. Normal read/write cycle timing applies. This parameter applies only when the cycle is extended until the negation of the BUSY# signal.

10.5 Mechanical Dimensions



Symbol	Min	Nom	Max
A	31.60	31.75	31.9
A1	6.00 BSC		
A2	3.20		
A3	4.00		
A4	20.00 BSC		
D	67.45	67.60	67.75
D1	24.50 BSC		
D2	63.60 BSC		
D3	2.50 BSC		
D4	2.10 BSC		
D5	4.80 BSC		
E*			10.20
e1	23.20 BSC		
e2	32.80 BSC		
N	144		

11. Ordering Information

Order Number: **MD2241-Dxxx-V3-T**

where:

MD2241	DiskOnChip DIMM Plus
Dxxx	Capacity in Mbyte: 32, 64, 96, 128
V3	Power supply: 3.3V
T	Temperature Range Blank: Commercial temperature range: 0°C to +70°C X: Extended temperature range: -40°C to +85°C

Refer to Table 13 for the combinations currently available and the associated order numbers.

Table 13: Available Combinations

Order Number	Capacity (Mbyte)	Temperature Range
MD2241-D32-V3	32	Commercial
MD2241-D64-V3	64	Commercial
MD2241-D96-V3	96	Commercial
MD2241-D128-V3	128	Commercial
MD2241-D32-V3-X	32	Extended
MD2241-D64-V3-X	64	Extended
MD2241-D96-V3-X	96	Extended
MD2241-D128-V3-X	128	Extended

Appendix A: Example Code

This appendix provides example code to verify basic DiskOnChip DIMM Plus operations in the system, mainly useful at first integration stages.

```
/*----------------------------------------------------------------------------*/
/*                          Identify DiskOnChip DIMM Plus                     */
/*                                                                            */
/* The target of this sequence is to make sure that DiskOnChip DIMM Plus      */
/* is alive and responds to basic commands.                                   */
/*                                                                            */
/* Returns: TRUE if DiskOnChip DIMM Plus responds, otherwise FALSE.           */
/*----------------------------------------------------------------------------*/
/* Release from Power-Down mode (just in case) by performing 3 consecutive reads */
/* from anywhere + 1 from 0x1fff                                              */
    for(i = 0;( i < 4 ); i++ )
    read from offset 0x1fff
/* If DiskOnChip DIMM Plus was in Power-Down mode, it is now in Normal mode   */
/* If DiskOnChip DIMM Plus was in any other mode, it will remain so.          */
/* Set DiskOnChip DIMM Plus to Reset mode                                     */
    Write 0x1c to offset 0x1006  /* to DiskOnChip Control Register            */
    Write 0xe3 to offset 0x1076   /* to DiskOnChip Control Confirmation Register */

/* Set DiskOnChip DIMM Plus to Normal mode                                    */
    Write 0x1d to offset 0x1006  /* to DiskOnChip Control Register            */
    Write 0xe2 to offset 0x1076   /* to DiskOnChip Control Confirmation Register */
/* Verify that DiskOnChip is in Normal mode.                                  */
    Read from offset 0x1006 into temp
    if (temp&0x01) != 1 return (FALSE)
/* Check Chip ID                                                              */
    Read from offset 0x1000 into temp
    if temp!=0x40 return(FALSE)

/* Check toggle bit                                                           */
/* The toggle bit should toggle on each consecutive read.                     */
    Read from offset 0x1046 into temp1
    Read from offset 0x1046 into temp2
    Read from offset 0x1046 into temp3
```

```
    If ((temp1&0x04) = (temp1&0x04)) return (FALSE)
    If ((temp2&0x04) = (temp2&0x04)) return (FALSE)
    If (temp3&0x04) != (temp3&0x04) return (FALSE)

/* Check Alias Resolution Register                                    */
    Write 0x16 to offset 0x1004
    Read from offset 0x1004 into temp
    If temp != 0x16 return (FALSE)
    Write 0x03 to offset 0x1004
    Read from offset 0x1004 into temp
    if temp != 0x03 return (FALSE)
Return (True) /* If True, then DiskOnChip DIMM Plus is alive and responding */
```

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