



# TN8, TS8 and TYNx08 Series

SENSITIVE & STANDARD

8A SCRs

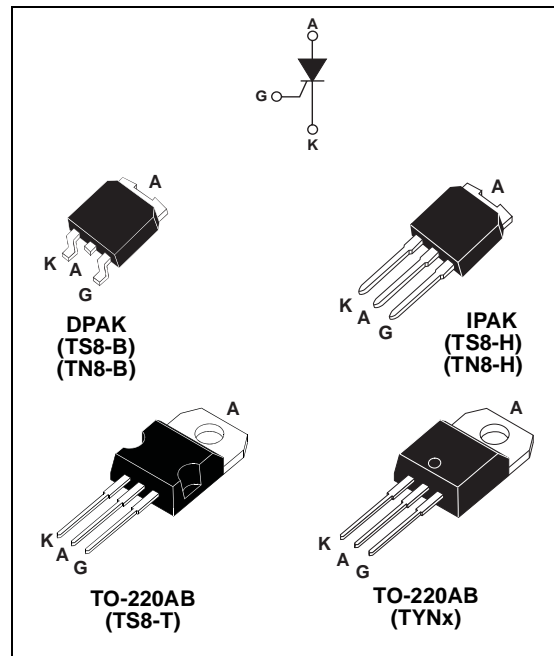
## MAIN FEATURES:

Symbol	Value	Unit
$I_{T(RMS)}$	8	A
$V_{DRM}/V_{RRM}$	600 to 1000	V
$I_{GT}$	0.2 to 15	mA

## DESCRIPTION

Available either in sensitive (TS8) or standard (TN8 / TYN) gate triggering levels, the 8A SCR series is suitable to fit all modes of control, found in applications such as overvoltage crowbar protection, motor control circuits in power tools and kitchen aids, inrush current limiting circuits, capacitive discharge ignition and voltage regulation circuits...

Available in through-hole or surface-mount packages, they provide an optimized performance in a limited space area.



## ABSOLUTE RATINGS (limiting values)

Symbol	Parameter			Value		Unit
				TS8/TN8	TYN	
$I_{T(RMS)}$	RMS on-state current (180° conduction angle)		$T_c = 110^\circ\text{C}$	8		A
$I_{T(AV)}$	Average on-state current (180° conduction angle)		$T_c = 110^\circ\text{C}$	5		A
$I_{TSM}$	Non repetitive surge peak on-state current	$t_p = 8.3 \text{ ms}$	$T_j = 25^\circ\text{C}$	73	100	A
		$t_p = 10 \text{ ms}$		70	95	
$I_t^2$	$I_t^2$ Value for fusing	$t_p = 10 \text{ ms}$	$T_j = 25^\circ\text{C}$	24.5	45	$\text{A}^2\text{s}$
$di/dt$	Critical rate of rise of on-state current $I_G = 2 \times I_{GT}$ , $t_r \leq 100 \text{ ns}$	$F = 60 \text{ Hz}$	$T_j = 125^\circ\text{C}$	50		$\text{A}/\mu\text{s}$
$I_{GM}$	Peak gate current	$t_p = 20 \mu\text{s}$	$T_j = 125^\circ\text{C}$	4		A
$P_{G(AV)}$	Average gate power dissipation		$T_j = 125^\circ\text{C}$	1		W
$T_{stg}$ $T_j$	Storage junction temperature range Operating junction temperature range			- 40 to + 150 - 40 to + 125		$^\circ\text{C}$
$V_{RGM}$	Maximum peak reverse gate voltage (for TN8 & TYN only)			5		V

## TN8, TS8 and TYNx08 Series

### ELECTRICAL CHARACTERISTICS (T<sub>j</sub> = 25°C, unless otherwise specified)

#### ■ SENSITIVE

Symbol	Test Conditions		TS820	Unit	
I <sub>GT</sub>	V <sub>D</sub> = 12 V    R <sub>L</sub> = 140 Ω	MAX.	200	μA	
V <sub>GT</sub>		MAX.	0.8	V	
V <sub>GD</sub>	V <sub>D</sub> = V <sub>DRM</sub> R <sub>L</sub> = 3.3 kΩ    R <sub>GK</sub> = 220 Ω    T <sub>j</sub> = 125°C	MIN.	0.1	V	
V <sub>RG</sub>	I <sub>RG</sub> = 10 μA	MIN.	8	V	
I <sub>H</sub>	I <sub>T</sub> = 50 mA    R <sub>GK</sub> = 1 kΩ	MAX.	5	mA	
I <sub>L</sub>	I <sub>G</sub> = 1 mA    R <sub>GK</sub> = 1 kΩ	MAX.	6	mA	
dV/dt	V <sub>D</sub> = 65 % V <sub>DRM</sub> R <sub>GK</sub> = 220 Ω    T <sub>j</sub> = 125°C	MIN.	5	V/μs	
V <sub>TM</sub>	I <sub>TM</sub> = 16 A    t <sub>p</sub> = 380 μs    T <sub>j</sub> = 25°C	MAX.	1.6	V	
V <sub>t0</sub>	Threshold voltage    T <sub>j</sub> = 125°C	MAX.	0.85	V	
R <sub>d</sub>	Dynamic resistance    T <sub>j</sub> = 125°C	MAX.	46	mΩ	
I <sub>DRM</sub>	V <sub>DRM</sub> = V <sub>RRM</sub> R <sub>GK</sub> = 220 Ω	T <sub>j</sub> = 25°C	MAX.	5	μA
I <sub>RRM</sub>		T <sub>j</sub> = 125°C		1	mA

#### ■ STANDARD

Symbol	Test Conditions		TN805	TN815	TYNx08	Unit	
I <sub>GT</sub>	V <sub>D</sub> = 12 V    R <sub>L</sub> = 33 Ω	MIN.	0.5	2	2	mA	
		MAX.	5	15	15		
V <sub>GT</sub>		MAX.	1.3			V	
V <sub>GD</sub>	V <sub>D</sub> = V <sub>DRM</sub> R <sub>L</sub> = 3.3 kΩ    T <sub>j</sub> = 125°C	MIN.	0.2			V	
I <sub>H</sub>	I <sub>T</sub> = 100 mA    Gate open	MAX.	25	40	30	mA	
I <sub>L</sub>	I <sub>G</sub> = 1.2 I <sub>GT</sub>	MAX.	30	50	70	mA	
dV/dt	V <sub>D</sub> = 67 % V <sub>DRM</sub> Gate open    T <sub>j</sub> = 125°C	MIN.	50	150	150	V/μs	
V <sub>TM</sub>	I <sub>TM</sub> = 16 A    t <sub>p</sub> = 380 μs    T <sub>j</sub> = 25°C	MAX.	1.6			V	
V <sub>t0</sub>	Threshold voltage    T <sub>j</sub> = 125°C	MAX.	0.85			V	
R <sub>d</sub>	Dynamic resistance    T <sub>j</sub> = 125°C	MAX.	46			mΩ	
I <sub>DRM</sub>	V <sub>DRM</sub> = V <sub>RRM</sub>	T <sub>j</sub> = 25°C	MAX.			5	μA
I <sub>RRM</sub>		T <sub>j</sub> = 125°C				2	mA

### THERMAL RESISTANCES

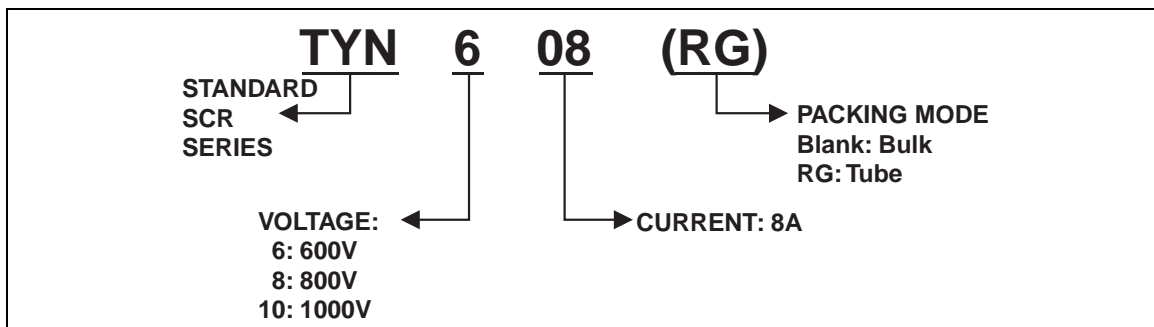
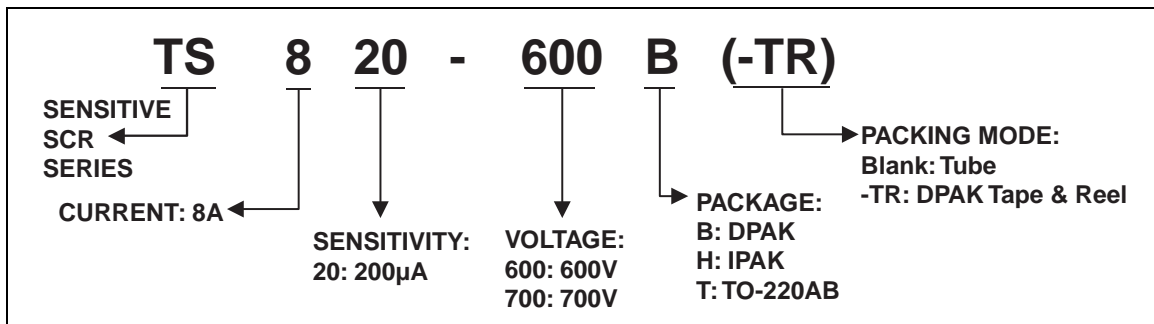
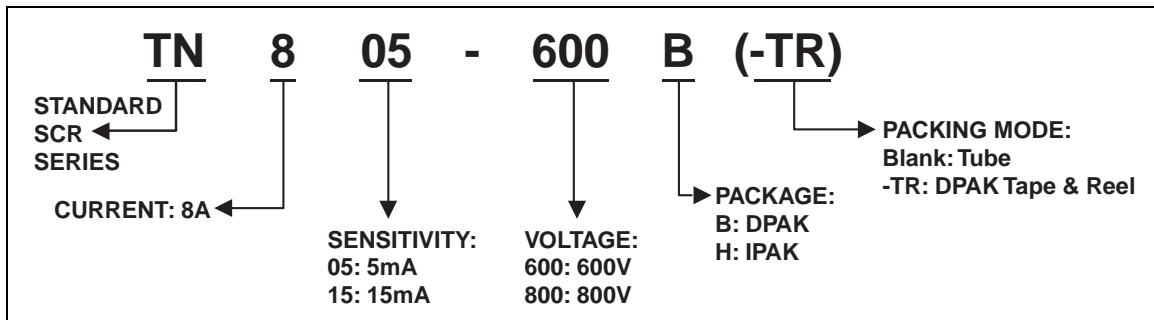
Symbol	Parameter	Value	Unit	
R <sub>th(j-c)</sub>	Junction to case (DC)	20	°C/W	
R <sub>th(j-a)</sub>	Junction to ambient (DC)	TO-220AB	60	°C/W
		IPAK	100	
		S = 0.5 cm <sup>2</sup> DPAK	70	

S= copper surface under tab

**PRODUCT SELECTOR**

Part Number	Voltage (xxx)				Sensitivity	Package
	600 V	700 V	800 V	1000 V		
TN805-xxxB	X		X		5 mA	DDPAK
TN805-xxxH	X		X		5 mA	I-PAK
TN815-xxxB	X		X		15 mA	DDPAK
TN815-xxxH	X		X		15 mA	I-PAK
TS820-xxxB	X	X			0.2 mA	DDPAK
TS820-xxxH	X	X			0.2 mA	I-PAK
TS820-xxxT	X	X			0.2 mA	TO-220AB
TYNx08	X		X	X	15 mA	TO-220AB

**ORDERING INFORMATION**



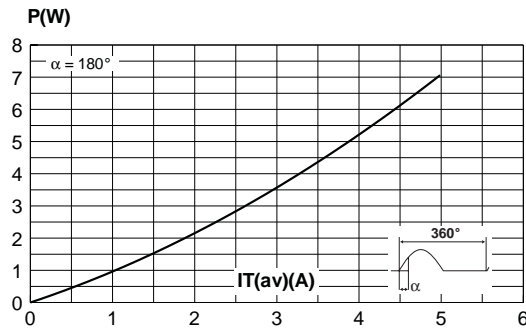
## TN8, TS8 and TYNx08 Series

### OTHER INFORMATION

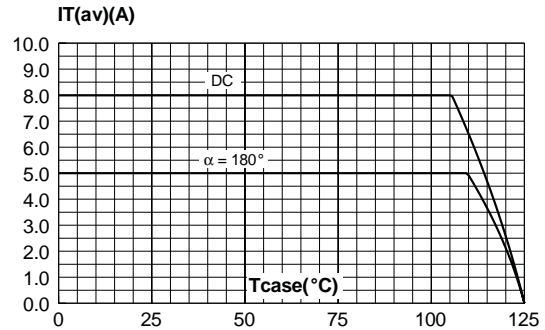
Part Number	Marking	Weight	Base Quantity	Packing mode
TN805-x00B	TN805x00	0.3 g	75	Tube
TN805-x00B-TR	TN805x00	0.3 g	2500	Tape & reel
TN805-x00H	TN805x00	0.4 g	75	Tube
TN815-x00B	TN815x00	0.3 g	75	Tube
TN815-x00B-TR	TN815x00	0.3 g	2500	Tape & reel
TN815-x00H	TN815x00	0.4 g	75	Tube
TS820-x00B	TS820x00	0.3 g	75	Tube
TS820-x00B-TR	TS820x00	0.3 g	2500	Tape & reel
TS820-x00H	TS820x00	0.4 g	75	Tube
TS820-x00T	TS820x00T	2.3 g	50	Tube
TYNx08	TYNx08	2.3 g	250	Bulk
TYNx08RG	TYNx08	2.3 g	50	Tube

Note: x = voltage

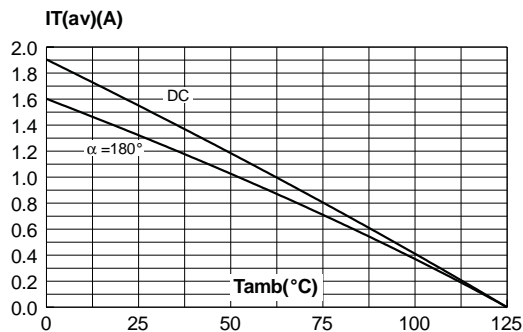
**Fig. 1:** Maximum average power dissipation versus average on-state current.



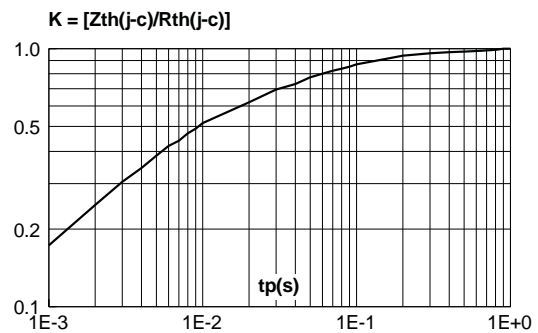
**Fig. 2-1:** Average and D.C. on-state current versus case temperature.



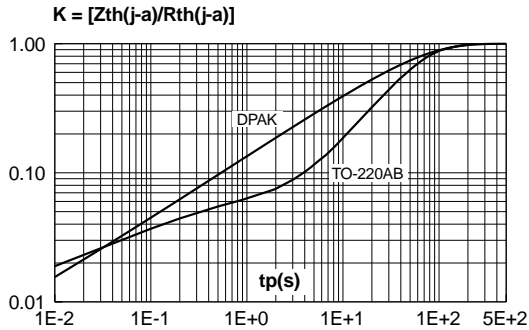
**Fig. 2-2:** Average and D.C. on-state current versus ambient temperature (device mounted on FR4 with recommended pad layout) (DPAK).



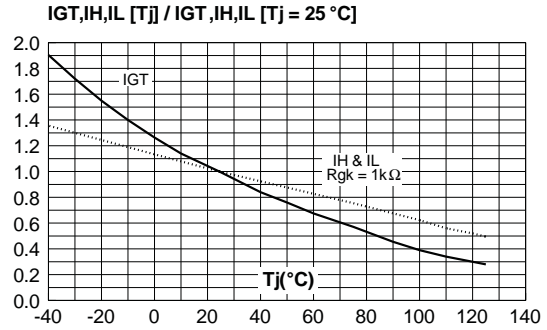
**Fig. 3-1:** Relative variation of thermal impedance junction to case versus pulse duration.



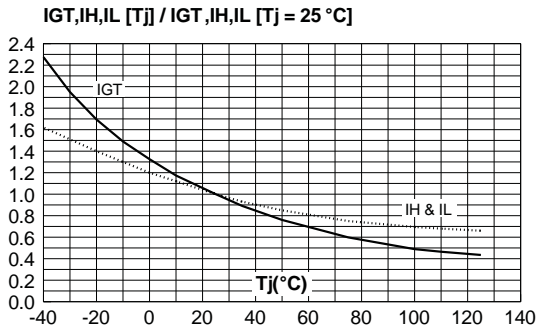
**Fig. 3-2:** Relative variation of thermal impedance junction to ambient versus pulse duration (recommended pad layout, FR4 PC board for DPAK).



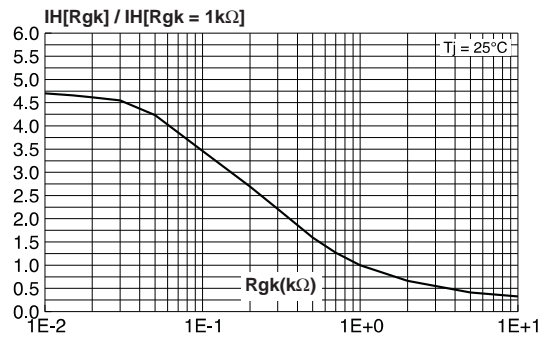
**Fig. 4-1:** Relative variation of gate trigger current and holding current versus junction temperature for TS8 series.



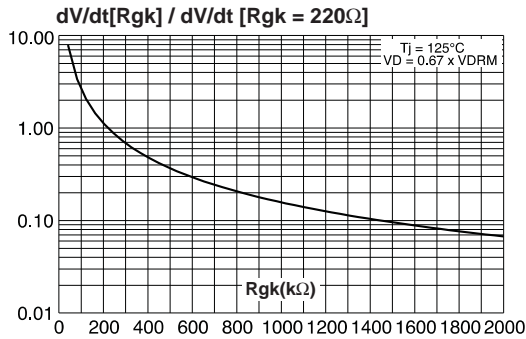
**Fig. 4-2:** Relative variation of gate trigger current and holding current versus junction temperature for TN8 & TYN series.



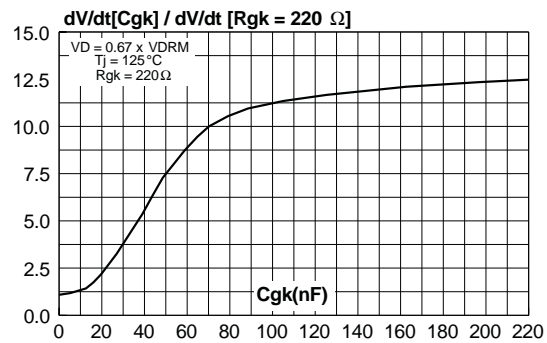
**Fig. 5:** Relative variation of holding current versus gate-cathode resistance (typical values) for TS8 series.



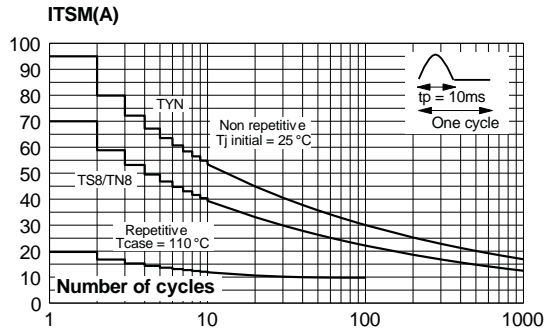
**Fig. 6:** Relative variation of dV/dt immunity versus gate-cathode resistance (typical values) for TS8 series.



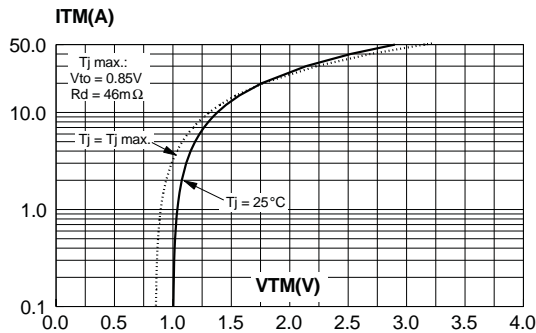
**Fig. 7:** Relative variation of dV/dt immunity versus gate-cathode capacitance (typical values) for TS8 series.



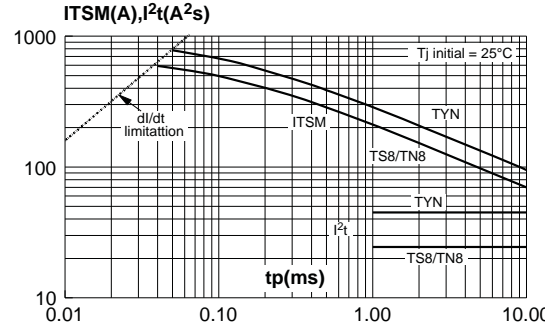
**Fig. 8:** Surge peak on-state current versus number of cycles. TS8/TN8/TYN.



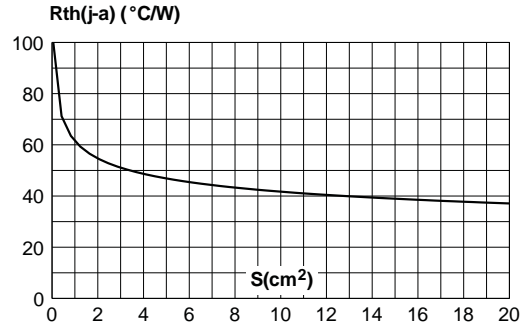
**Fig. 10:** On-state characteristics (maximum values).



**Fig. 9:** Non-repetitive surge peak on-state current for a sinusoidal pulse with width  $t_p < 10\text{ms}$ , and corresponding values of  $I^2t$ .

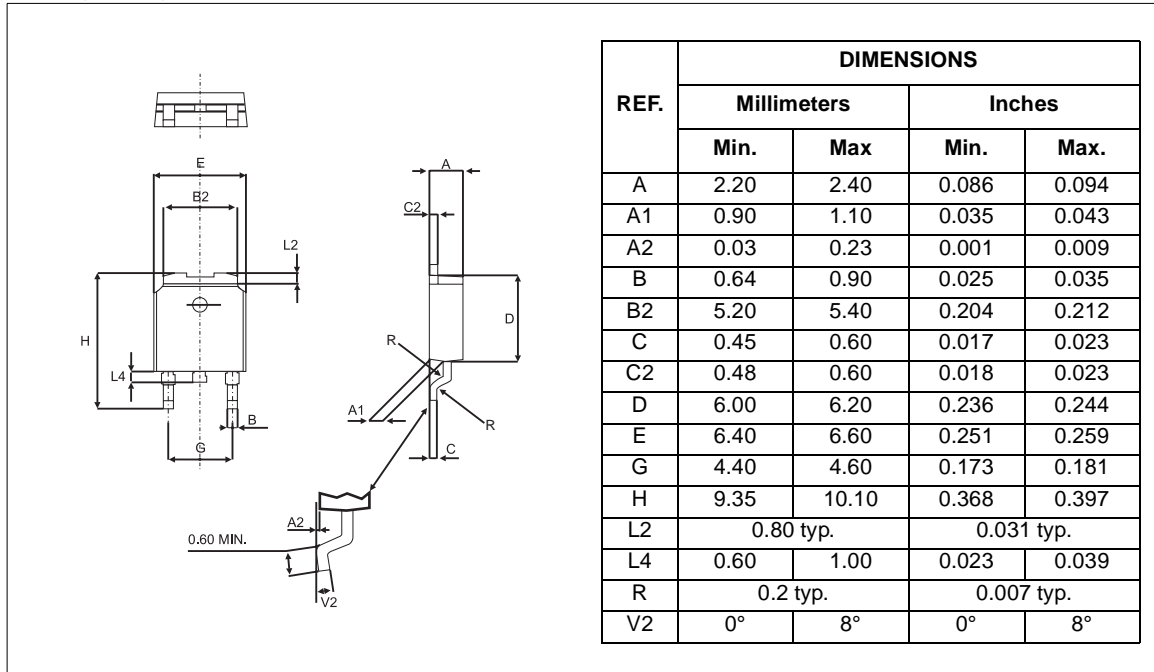


**Fig. 11:** Thermal resistance junction to ambient versus copper surface under tab (Epoxy printed circuit board FR4, copper thickness:  $35\ \mu\text{m}$ ) (DPAK).



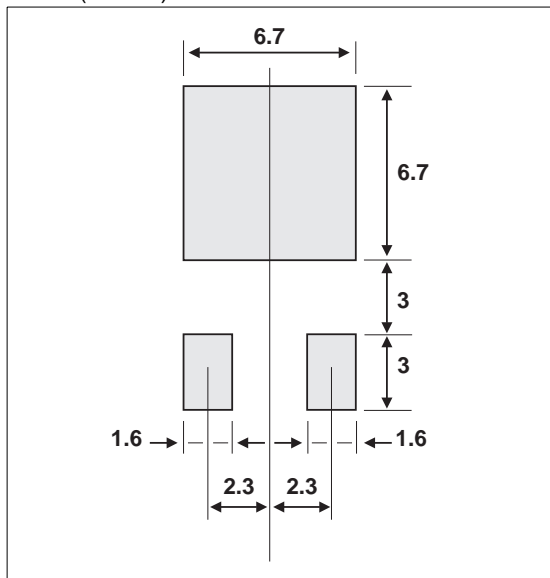
**PACKAGE MECHANICAL DATA**

DPAK (Plastic)



**FOOTPRINT DIMENSIONS (in millimeters)**

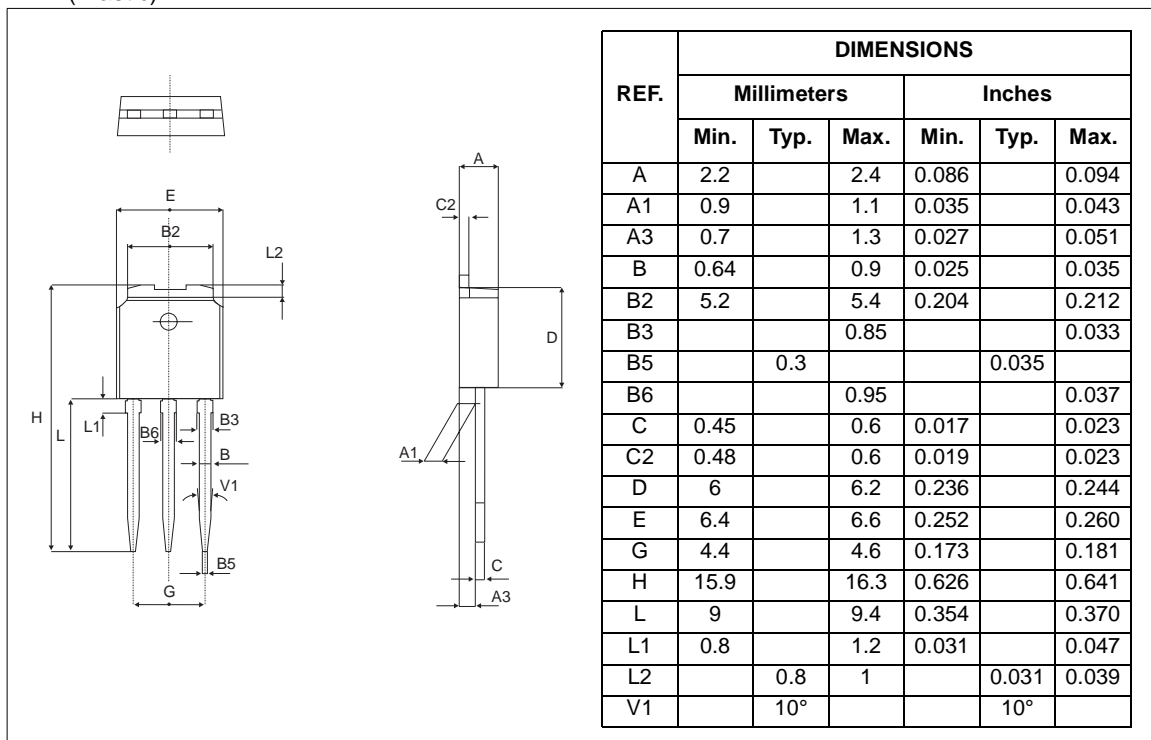
DPAK (Plastic)



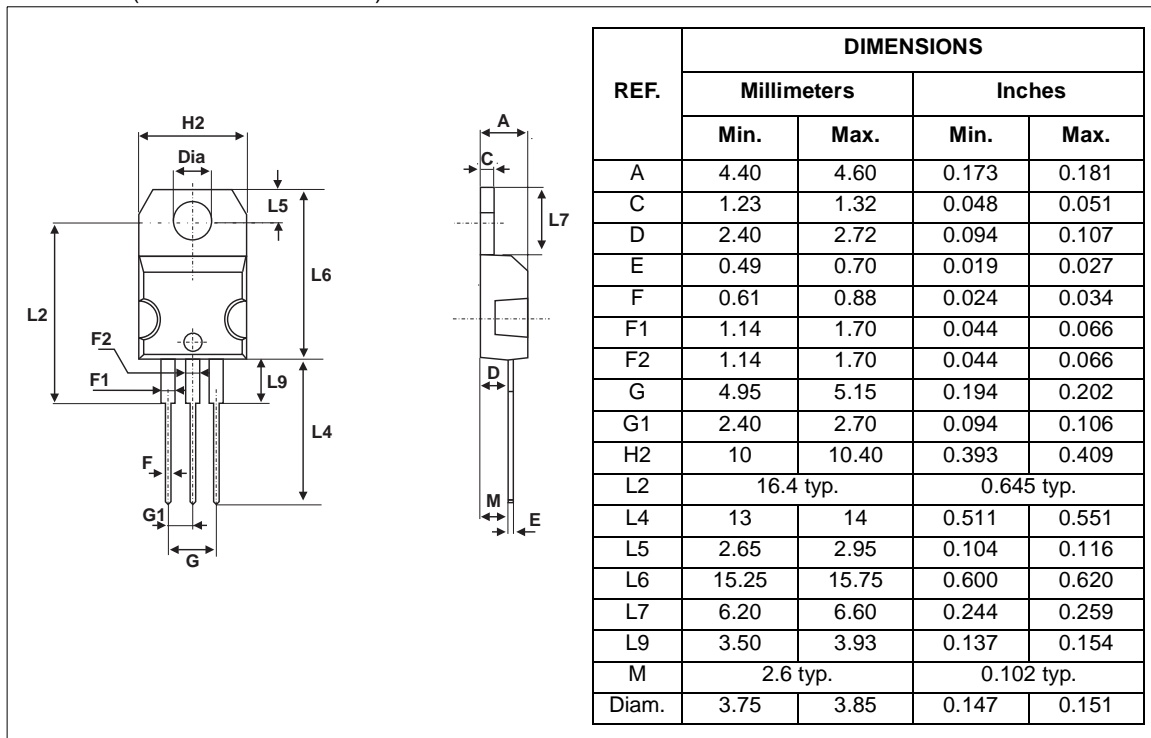
# TN8, TS8 and TYNx08 Series

## PACKAGE MECHANICAL DATA

IPAK (Plastic)



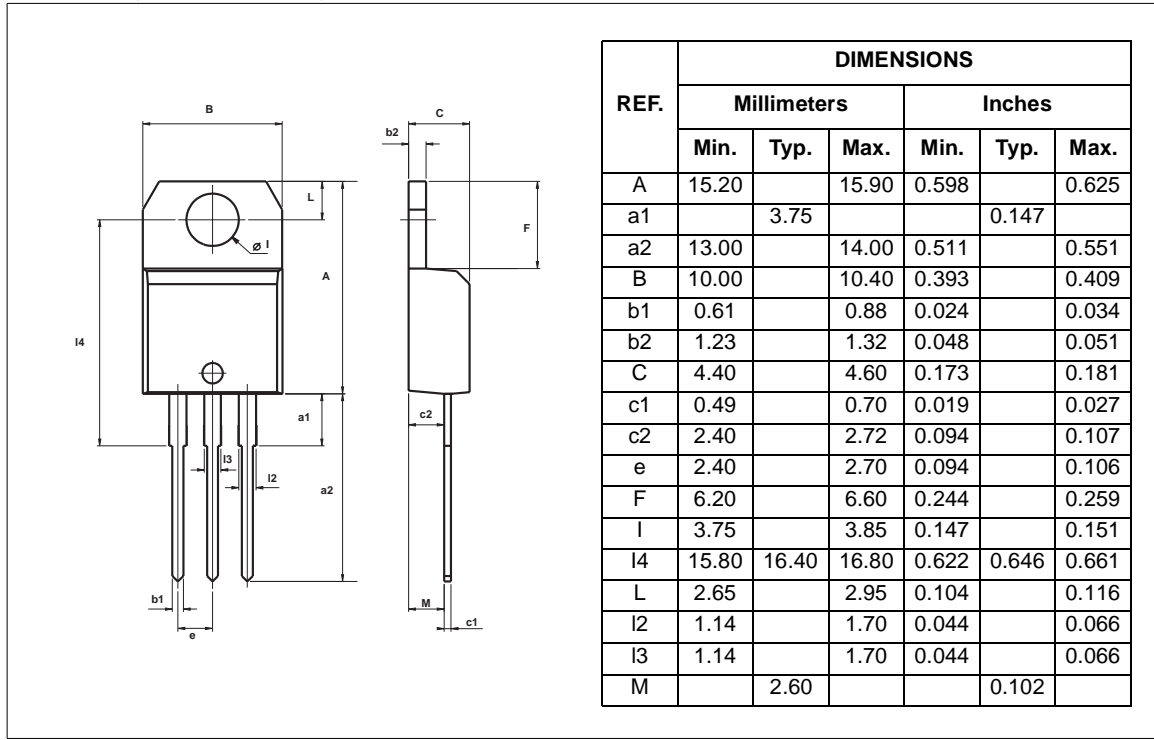
TO-220AB (Plastic - with notches)





**PACKAGE MECHANICAL DATA**

TO-220AB (Without notches)



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