



# TS615

## DUAL WIDE BAND OPERATIONAL AMPLIFIER WITH HIGH OUTPUT CURRENT

- **LOW NOISE** : 2.5nV/√Hz
- **HIGH OUTPUT CURRENT** : 420mA
- **VERY LOW HARMONIC AND INTERMODULATION DISTORTION**
- **HIGH SLEW RATE** : 410V/μs
- **-3dB BANDWIDTH** : 40MHz@gain=12dB on 25Ω load single ended.
- **21.2Vp-p DIFFERENTIAL OUTPUT SWING** on 50Ω load, 12V power supply
- **CURRENT FEEDBACK STRUCTURE**
- **5V to 12V POWER SUPPLY**
- **SPECIFIED FOR 20Ω and 50Ω DIFFERENTIAL LOAD**
- **POWER DOWN FUNCTION WITH A SHORT CIRCUITED OUTPUT** to keep the matching with the line in sleep mode

### DESCRIPTION

The TS615 is a dual operational amplifier featuring a high output current 410mA. These drivers can be configured differentially for driving signals in telecommunication systems using multiple carriers. The TS615 is ideally suited for xDSL (High Speed Asymmetrical Digital Subscriber Line) applications. This circuit is capable of driving a 10Ω or 25Ω load at ±2.5V, 5V, ±6V or +12V power supply. The TS615 will be able to reach a -3dB bandwidth of 40MHz on 25Ω load with a 12dB gain. This device is designed for the high slew rates to support low harmonic distortion and intermodulation. The TS615 is fitted out with Power Down function to decrease the consumption. During this sleep state the device displays a short circuit output in order to keep the impedance matching with the line. The TS615 is housed in TSSOP14 Exposed-Pad plastic package for a very low thermal resistance.

### APPLICATION

- Line driver for xDSL
- Multiple Video Line Driver

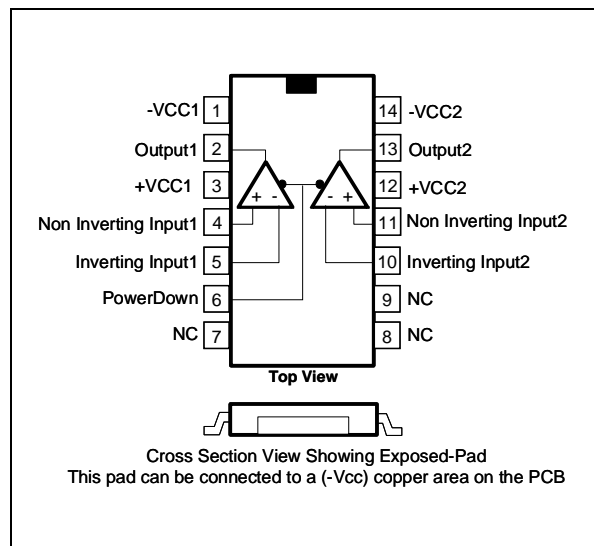


### ORDER CODE

Part Number	Temperature Range	Package
TS615IPWT	-40, +85°C	PW

PW= Thin Shrink Small Outline Package with Exposed-Pad (TSSOP Exposed-Pad) only available in Tape & Reel (PWT)

### PIN CONNECTIONS (top view)



**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage <sup>1)</sup>	$\pm 7$	V
$V_{id}$	Differential Input Voltage <sup>2)</sup>	$\pm 2$	V
$V_{in}$	Input Voltage Range <sup>3)</sup>	$\pm 6$	V
$T_{oper}$	Operating Free Air Temperature Range	-40 to + 85	°C
$T_{std}$	Storage Temperature	-65 to +150	°C
$T_j$	Maximum Junction Temperature	150	°C
$R_{thjc}$	Thermal Resistance Junction to Case	4	°C/W
$R_{thja}$	Thermal Resistance Junction to Ambient Area	40	°C/W
$P_{max.}$	Maximum Power Dissipation (@25°C)	3.1	W
ESD except pins 4, 5, 10, 11	CDM : Charged Device Model	1.5	kV
	HBM : Human Body Model	2	kV
	MM : Machine Model	200	V
ESD only pins 4, 5, 10, 11	CDM : Charged Device Model	1	kV
	HBM : Human Body Model	1	kV
	MM : Machine Model	100	V
	Output Short Circuit	4)	

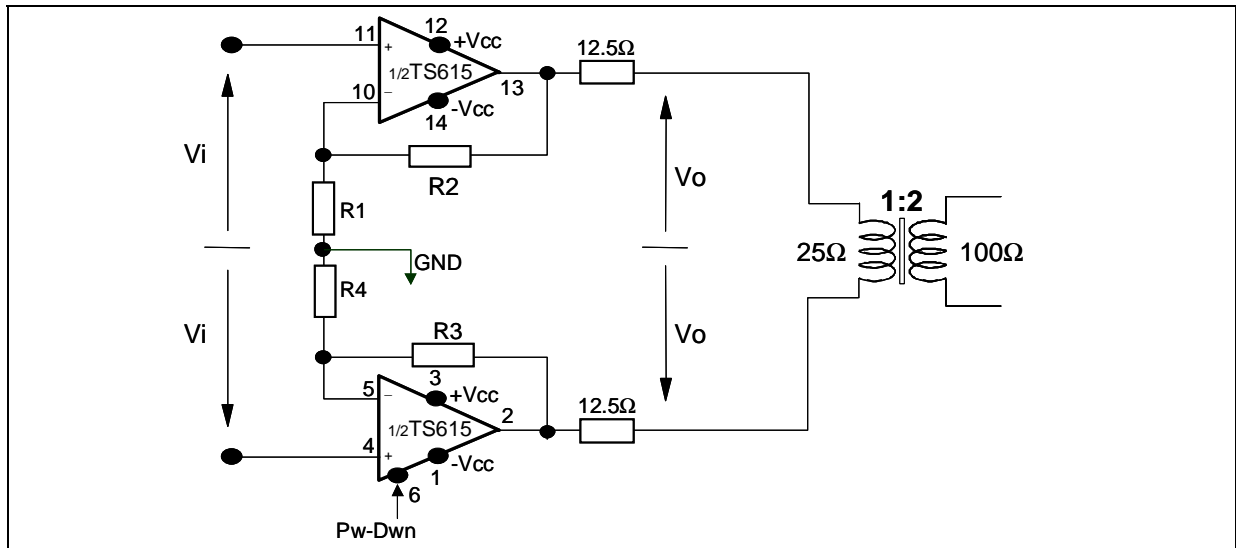
1. All voltage values, except differential voltage are with respect to network terminal.
2. Differential voltage are non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of input and output voltage must never exceed  $V_{CC} + 0.3V$ .
4. An output current limitation protects the circuit from transient currents. Short-circuits can cause excessive heating. Destructive dissipation can result from short circuit on amplifiers.

**OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit
$V_{CC}$	Power Supply Voltage	$\pm 2.5$ to $\pm 6$	V
$V_{icm}$	Common Mode Input Voltage	$-V_{CC} + 1.5V$ to $+V_{CC} - 1.5V$	V

**TYPICAL APPLICATION:**

Differential Line Driver for xDSL Applications



**ELECTRICAL CHARACTERISTICS**

$V_{CC} = \pm 6\text{Volts}$ ,  $R_{fb}=910\Omega$ ,  $T_{amb} = 25^\circ\text{C}$  (unless otherwise specified)

**Note:** as described on page 24 (table 71), the TS615 requires a 620 $\Omega$  feedback resistor for an optimised bandwidth with a gain of 12B for a 12V power supply. Nevertheless, due to production test constraints, the TS615 is tested with the same feedback resistor for 12V and 5V power supplies (910 $\Omega$ ).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
<b>DC PERFORMANCE</b>						
$V_{io}$	Input Offset Voltage	$T_{amb}$		1.25	3.5	mV
		$T_{min.} < T_{amb} < T_{max.}$		2.1		
$\Delta V_{io}$	Differential Input Offset Voltage	$T_{amb} = 25^\circ\text{C}$			2.5	mV
$I_{ib+}$	Positive Input Bias Current	$T_{amb}$		6	30	$\mu\text{A}$
		$T_{min.} < T_{amb} < T_{max.}$		7.8		
$I_{ib-}$	Negative Input Bias Current	$T_{amb}$		3	15	$\mu\text{A}$
		$T_{min.} < T_{amb} < T_{max.}$		3.2		
$Z_{IN+}$	Input(+) Impedance			82		k $\Omega$
$Z_{IN-}$	Input(-) Impedance			54		$\Omega$
$C_{IN+}$	Input(+) Capacitance			1		pF
CMR	Common Mode Rejection Ratio $20 \log (\Delta V_{ic}/\Delta V_{io})$	$\Delta V_{ic} = \pm 4.5\text{V}$	58	63		dB
		$T_{min.} < T_{amb} < T_{max.}$		61		
SVR	Supply Voltage Rejection Ratio $20 \log (\Delta V_{cc}/\Delta V_{io})$	$\Delta V_{cc} = \pm 2.5\text{V to } \pm 6\text{V}$	72	79		dB
		$T_{min.} < T_{amb} < T_{max.}$		78		
$I_{CC}$	Total Supply Current per Operator	No load		14	17	mA
<b>DYNAMIC PERFORMANCE and OUTPUT CHARACTERISTIC</b>						
$R_{OL}$	Open Loop Transimpedance	$V_{out} = 7\text{Vp-p}$ , $R_L = 25\Omega$	5	21		M $\Omega$
		$T_{min.} < T_{amb.} < T_{max.}$		8.9		
BW	-3dB Bandwidth	Small Signal $V_{out} < 20\text{mVp}$ $A_V = 12\text{dB}$ , $R_L = 25\Omega$	25	40		MHz
	Full Power Bandwidth	Large Signal $V_{out} = 3\text{Vp}$ $A_V = 12\text{dB}$ , $R_L = 25\Omega$		26		
	Gain Flatness @ 0.1dB	Small Signal $V_{out} < 20\text{mVp}$ $A_V = 12\text{dB}$ , $R_L = 25\Omega$		7		
$T_r$	Rise Time	$V_{out} = 6\text{Vp-p}$ , $A_V = 12\text{dB}$ , $R_L = 25\Omega$		10.6		ns
$T_f$	Fall Time	$V_{out} = 6\text{Vp-p}$ , $A_V = 12\text{dB}$ , $R_L = 25\Omega$		12.2		ns
$T_s$	Settling Time	$V_{out} = 6\text{Vp-p}$ , $A_V = 12\text{dB}$ , $R_L = 25\Omega$		50		ns
SR	Slew Rate	$V_{out} = 6\text{Vp-p}$ , $A_V = 12\text{dB}$ , $R_L = 25\Omega$	330	410		V/ $\mu\text{s}$
$V_{OH}$	High Level Output Voltage	$R_L = 25\Omega$ Connected to GND	4.8	5.1		V
$V_{OL}$	Low Level Output Voltage	$R_L = 25\Omega$ Connected to GND		-5.5	-5.2	V
$I_{out}$	Output Sink Current	$V_{out} = -4\text{Vp}$	-350	-530		mA
		$T_{min.} < T_{amb} < T_{max.}$		-440		
	Output Source Current	$V_{out} = +4\text{Vp}$	330	420		
		$T_{min.} < T_{amb} < T_{max.}$		365		

**Note:** as described on page 24 (table 71), the TS615 requires a 620Ω feedback resistor for an optimised bandwidth with a gain of 12B for a 12V power supply. Nevertheless, due to production test constraints, the TS615 is tested with the same feedback resistor for 12V and 5V power supplies (910Ω).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
<b>NOISE AND DISTORTION</b>						
eN	Equivalent Input Noise Voltage	F = 100kHz		2.5		nV/√Hz
iNp	Equivalent Input Noise Current (+)	F = 100kHz		15		pA/√Hz
iNn	Equivalent Input Noise Current (-)	F = 100kHz		21		pA/√Hz
HD2	2nd Harmonic distortion (differential configuration)	V <sub>out</sub> = 14Vp-p, A <sub>v</sub> = 12dB F = 110kHz, R <sub>L</sub> = 50Ω diff.		-87		dBc
HD3	3rd Harmonic distortion (differential configuration)	V <sub>out</sub> = 14Vp-p, A <sub>v</sub> = 12dB F = 110kHz, R <sub>L</sub> = 50Ω diff.		-83		dBc
IM2	2nd Order Intermodulation Product (differential configuration)	F1 = 100kHz, F2 = 110kHz V <sub>out</sub> = 16Vp-p, A <sub>v</sub> = 12dB R <sub>L</sub> = 50Ω diff.		-76		dBc
		F1 = 370kHz, F2 = 400kHz V <sub>out</sub> = 16Vp-p, A <sub>v</sub> = 12dB R <sub>L</sub> = 50Ω diff.		-75		
IM3	3rd Order Intermodulation Product (differential configuration)	F1 = 100kHz, F2 = 110kHz V <sub>out</sub> = 16Vp-p, A <sub>v</sub> = 12dB R <sub>L</sub> = 50Ω diff.		-88		dBc
		F1 = 370kHz, F2 = 400kHz V <sub>out</sub> = 16Vp-p, A <sub>v</sub> = 12dB R <sub>L</sub> = 50Ω diff.		-87		

**ELECTRICAL CHARACTERISTICS**
 $V_{CC} = \pm 2.5\text{Volts}$ ,  $R_{fb} = 910\Omega$ ,  $T_{amb} = 25^\circ\text{C}$  (unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
<b>DC PERFORMANCE</b>						
$V_{io}$	Input Offset Voltage	$T_{amb}$		0.5	2.5	mV
		$T_{min.} < T_{amb} < T_{max.}$		1.2		
$\Delta V_{io}$	Differential Input Offset Voltage	$T_{amb} = 25^\circ\text{C}$			2.5	mV
$I_{ib+}$	Positive Input Bias Current	$T_{amb}$		5	30	$\mu\text{A}$
		$T_{min.} < T_{amb} < T_{max.}$		8		
$I_{ib-}$	Negative Input Bias Current	$T_{amb}$		0.8	11	$\mu\text{A}$
		$T_{min.} < T_{amb} < T_{max.}$		1.24		
$Z_{IN+}$	Input(+) Impedance			71		$\text{k}\Omega$
$Z_{IN-}$	Input(-) Impedance			62		$\Omega$
$C_{IN+}$	Input(+) Capacitance			1.5		pF
CMR	Common Mode Rejection Ratio $20 \log (\Delta V_{ic} / \Delta V_{io})$	$\Delta V_{ic} = \pm 1\text{V}$	55	60		dB
		$T_{min.} < T_{amb.} < T_{max.}$		58		
SVR	Supply Voltage Rejection Ratio $20 \log (\Delta V_{cc} / \Delta V_{io})$	$\Delta V_{cc} = \pm 2\text{V to } \pm 2.5\text{V}$	63	77		dB
		$T_{min.} < T_{amb.} < T_{max.}$		76		
$I_{CC}$	Total Supply Current per Operator	No load		11.9	15	mA
<b>DYNAMIC PERFORMANCE and OUTPUT CHARACTERISTICS</b>						
$R_{OL}$	Open Loop Transimpedance	$V_{out} = 2\text{Vp-p}$ , $R_L = 10\Omega$	2	5.4		$\text{M}\Omega$
		$T_{min.} < T_{amb.} < T_{max.}$		2.1		
BW	-3dB Bandwidth	Small Signal $V_{out} < 20\text{mVp}$ $A_V = 12\text{dB}$ , $R_L = 10\Omega$	20	30		MHz
	Full Power Bandwidth	Large Signal $V_{out} = 1.4\text{Vp}$ $A_V = 12\text{dB}$ , $R_L = 10\Omega$		20		
	Gain Flatness @ 0.1dB	Small Signal $V_{out} < 20\text{mVp}$ $A_V = 12\text{dB}$ , $R_L = 10\Omega$		5.7		MHz
$T_r$	Rise Time	$V_{out} = 2.8\text{Vp-p}$ , $A_V = 12\text{dB}$ $R_L = 10\Omega$		11		ns
$T_f$	Fall Time	$V_{out} = 2.8\text{Vp-p}$ , $A_V = 12\text{dB}$ $R_L = 10\Omega$		11.5		ns
$T_s$	Settling Time	$V_{out} = 2.2\text{Vp-p}$ , $A_V = 12\text{dB}$ $R_L = 10\Omega$		39		ns
SR	Slew Rate	$V_{out} = 2.2\text{Vp-p}$ , $A_V = 12\text{dB}$ $R_L = 10\Omega$	100	130		$\text{V}/\mu\text{s}$
$V_{OH}$	High Level Output Voltage	$R_L = 10\Omega$ Connected to GND	1.5	1.75		V
$V_{OL}$	Low Level Output Voltage	$R_L = 10\Omega$ Connected to GND		-2.05	-1.8	V
$I_{out}$	Output Sink Current	$V_{out} = -1.25\text{Vp}$	-350	-470		mA
		$T_{min.} < T_{amb} < T_{max.}$		-450		
	Output Source Current	$V_{out} = +1.25\text{Vp}$	200	270		
		$T_{min.} < T_{amb} < T_{max.}$		245		

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
<b>NOISE AND DISTORTION</b>						
eN	Equivalent Input Noise Voltage	F = 100kHz		2.5		nV/√Hz
iNp	Equivalent Input Noise Current (+)	F = 100kHz		15		pA/√Hz
iNn	Equivalent Input Noise Current (-)	F = 100kHz		21		pA/√Hz
HD2	2nd Harmonic distortion (differential configuration)	V <sub>out</sub> = 6Vp-p, A <sub>V</sub> = 12dB F = 110kHz, R <sub>L</sub> = 20Ω diff.		-97		dBc
HD3	3rd Harmonic distortion (differential configuration)	V <sub>out</sub> = 6Vp-p, A <sub>V</sub> = 12dB F = 110kHz, R <sub>L</sub> = 20Ω diff.		-98		dBc
IM2	2nd Order Intermodulation Product (differential configuration)	F1 = 100kHz, F2 = 110kHz V <sub>out</sub> = 6Vp-p, A <sub>V</sub> = 12dB R <sub>L</sub> = 20Ω diff.		-86		dBc
		F1 = 370kHz, F2 = 400kHz V <sub>out</sub> = 6Vp-p, A <sub>V</sub> = 12dB R <sub>L</sub> = 20Ω diff.		-88		
IM3	3rd Order Intermodulation Product (differential configuration)	F1 = 100kHz, F2 = 110kHz V <sub>out</sub> = 6Vp-p, A <sub>V</sub> = 12dB R <sub>L</sub> = 20Ω diff.		-90		dBc
		F1 = 370kHz, F2 = 400kHz V <sub>out</sub> = 6Vp-p, A <sub>V</sub> = 12dB R <sub>L</sub> = 20Ω diff.		-85		

**POWER DOWN MODE FEATURES** (The Power Down command is a MOS input featuring a high input impedance)

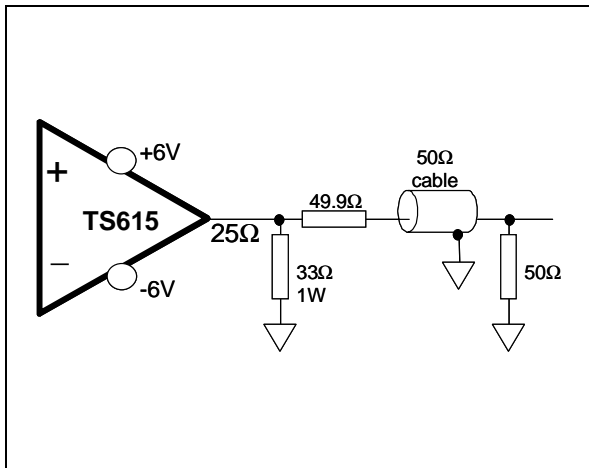
V<sub>CC</sub> = ±2.5Volts, 5Volts, ±6Volts or 12Volts, T<sub>amb</sub> = 25°C

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>pdw</sub>	Pin (6) Threshold Voltage for Power Down Mode				V
	Low Level	-V <sub>CC</sub>		-V <sub>CC</sub> +0.8	
	High Level	-V <sub>CC</sub> +2		+V <sub>CC</sub>	
I <sub>CC</sub> <sub>pdw</sub>	Power Down Mode Total Current Consumption@ V <sub>CC</sub> =5V		69	80	μA
	Power Down Mode Total Current Consumption@ V <sub>CC</sub> =12V		148	180	μA
R <sub>pdw</sub>	Power Down Mode Output Impedance @ V <sub>CC</sub> =5V		19	23	Ω
	Power Down Mode Output Impedance @ V <sub>CC</sub> =12V		15.3	19	Ω
C <sub>pdw</sub>	Power Down Mode Output Capacitance		63		pF

POWER DOWN CONTROL		CIRCUIT STATUS	
V <sub>pdw</sub> =Low Level		Active	
V <sub>pdw</sub> =High Level		Standby	

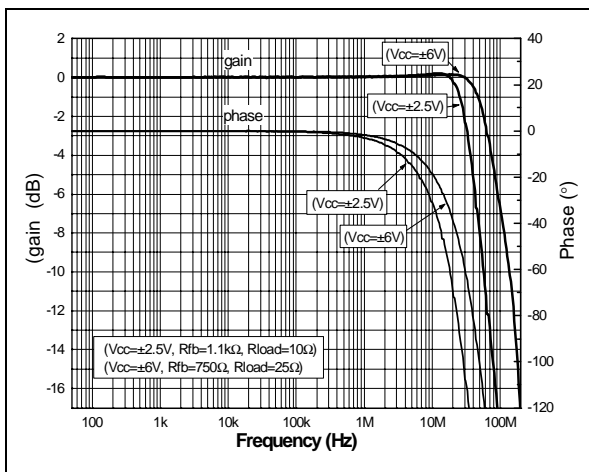
**Figure 1 : Load Configuration**

Load:  $R_L=25\Omega$ ,  $V_{CC}=\pm 6V$



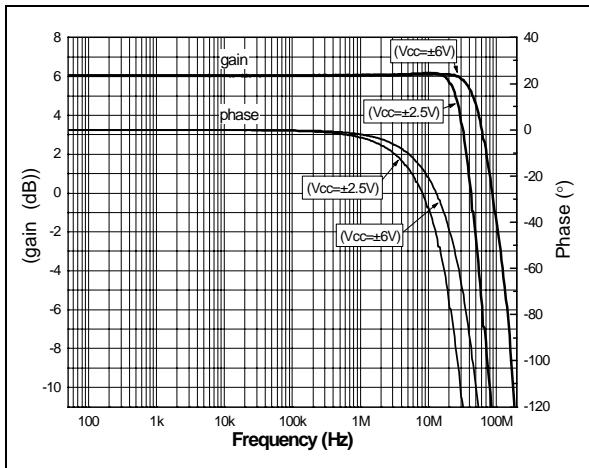
**Figure 2 : Closed Loop Gain vs. Frequency**

$A_V=+1$



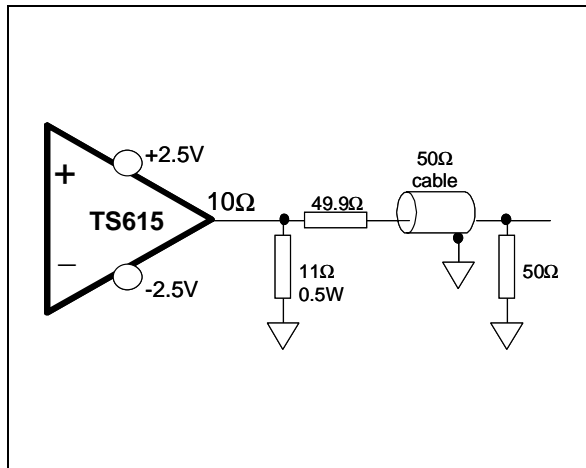
**Figure 3 : Closed Loop Gain vs. Frequency**

$A_V=+2$



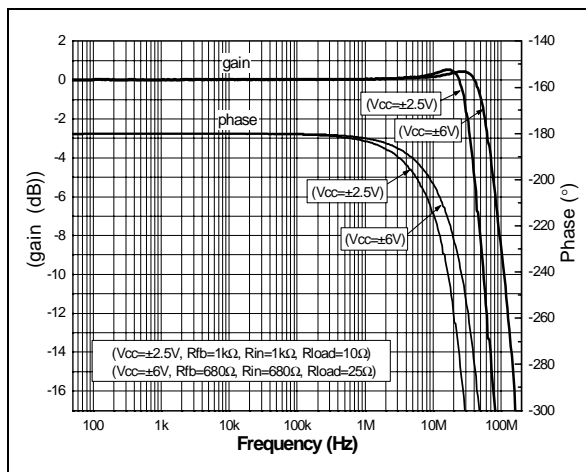
**Figure 4 : Load Configuration**

Load:  $R_L=10\Omega$ ,  $V_{CC}=\pm 2.5V$



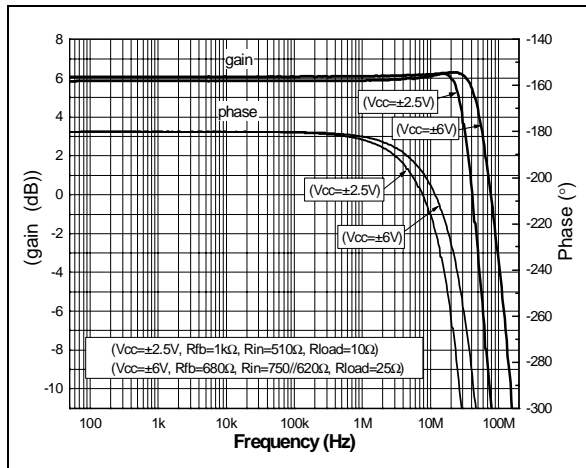
**Figure 5 : Closed Loop Gain vs. Frequency**

$A_V=-1$

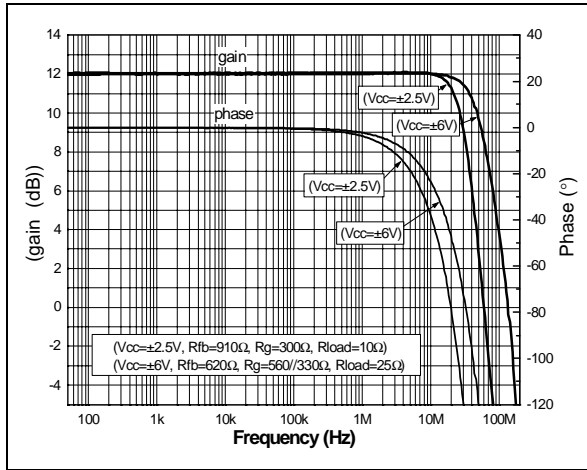


**Figure 6 : Closed Loop Gain vs. Frequency**

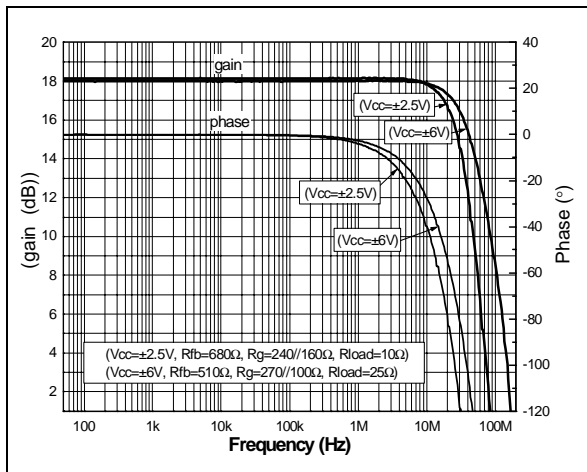
$A_V=-2$



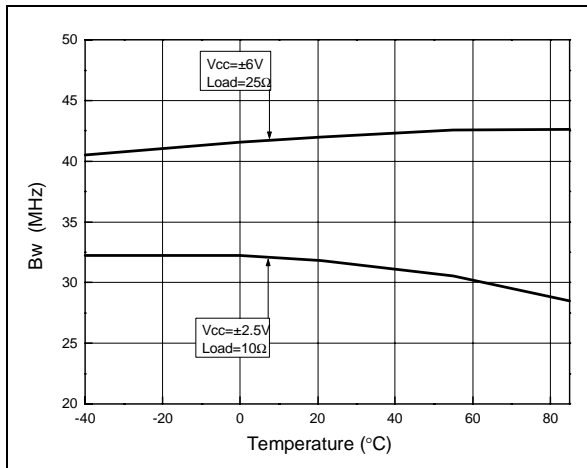
**Figure 7 : Closed Loop Gain vs. Frequency**  
 $A_V=+4$



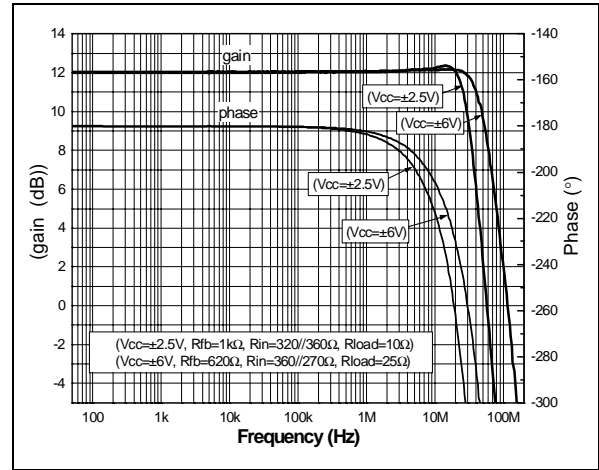
**Figure 8 : Closed Loop Gain vs. Frequency**  
 $A_V=+8$



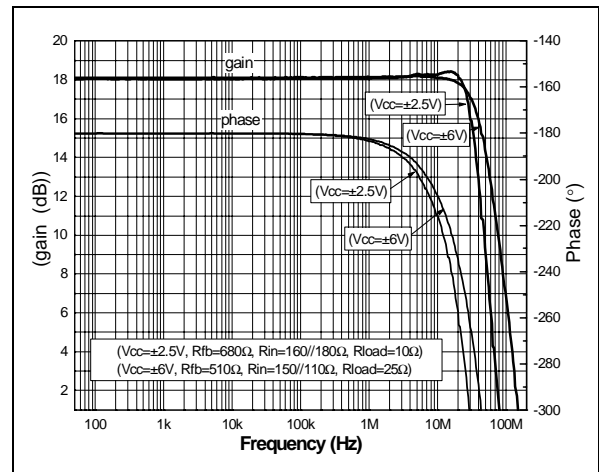
**Figure 9 : Bandwidth vs. Temperature**  
 $A_V=+4, R_{fb}=910\Omega$



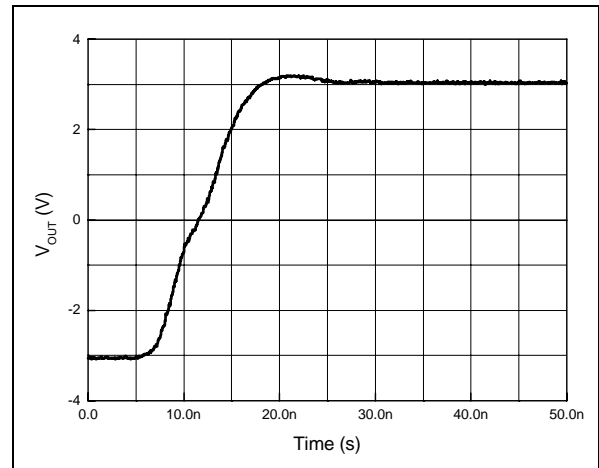
**Figure 10 : Closed Loop Gain vs. Frequency**  
 $A_V=-4$



**Figure 11 : Closed Loop Gain vs. Frequency**  
 $A_V=-8$

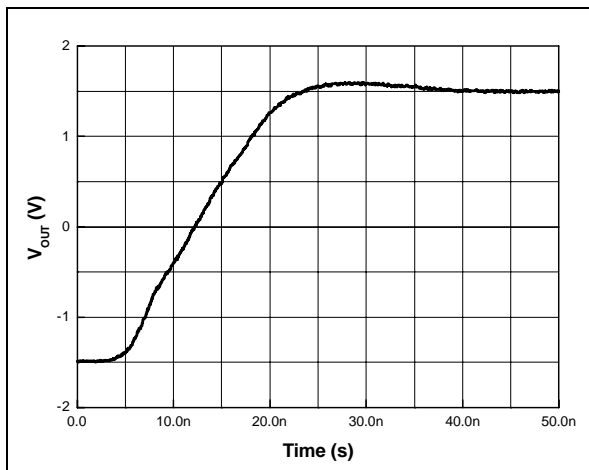


**Figure 12 : Positive Slew Rate**  
 $A_V=+4, R_{fb}=620\Omega, V_{CC}=\pm 6V, R_L=25\Omega$

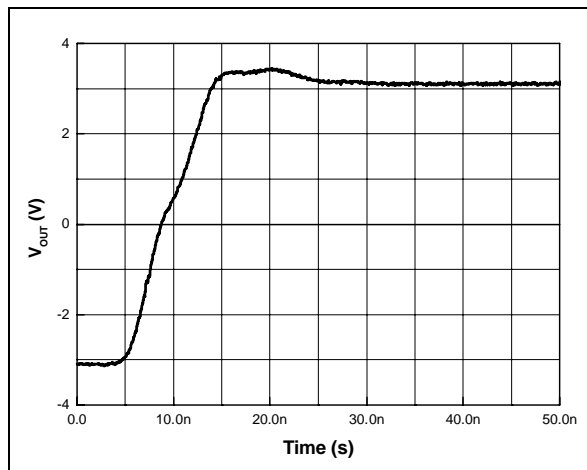




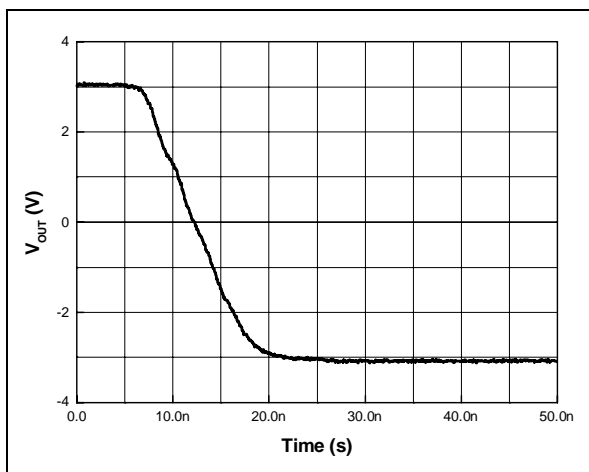
**Figure 13 : Positive Slew Rate**  
 $A_V=+4$ ,  $R_{fb}=910\Omega$ ,  $V_{CC}=\pm 2.5V$ ,  $R_L=10\Omega$



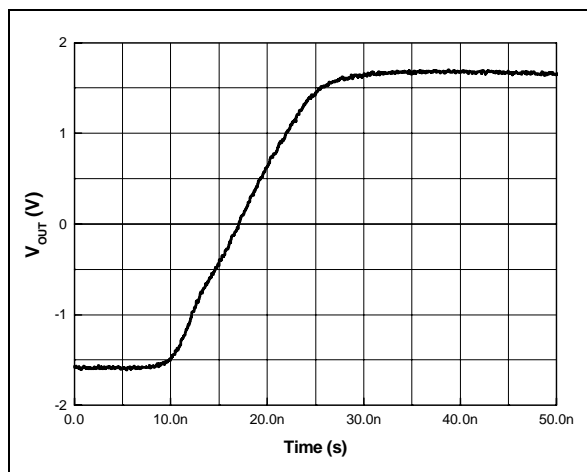
**Figure 16 : Positive Slew Rate**  
 $A_V= - 4$ ,  $R_{fb}=620\Omega$ ,  $V_{CC}=\pm 6V$ ,  $R_L=25\Omega$



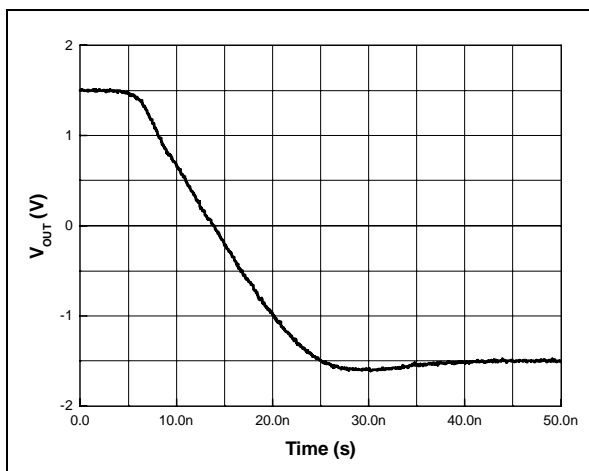
**Figure 14 : Negative Slew Rate**  
 $A_V=+4$ ,  $R_{fb}=620\Omega$ ,  $V_{CC}=\pm 6V$ ,  $R_L=25\Omega$



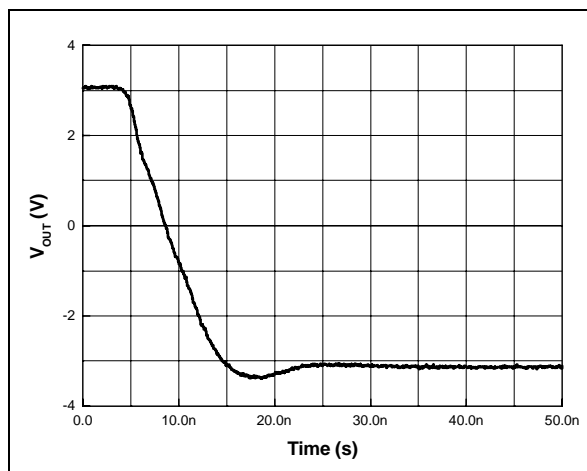
**Figure 17 : Positive Slew Rate**  
 $A_V= - 4$ ,  $R_{fb}=910\Omega$ ,  $V_{CC}=\pm 2.5V$ ,  $R_L=10\Omega$



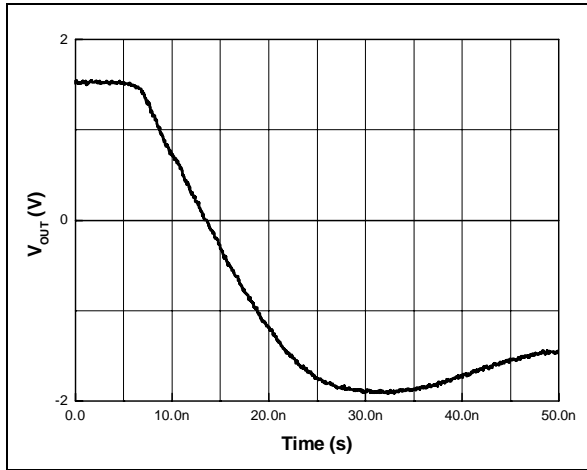
**Figure 15 : Negative Slew Rate**  
 $A_V=+4$ ,  $R_{fb}=910\Omega$ ,  $V_{CC}=\pm 2.5V$ ,  $R_L=10\Omega$



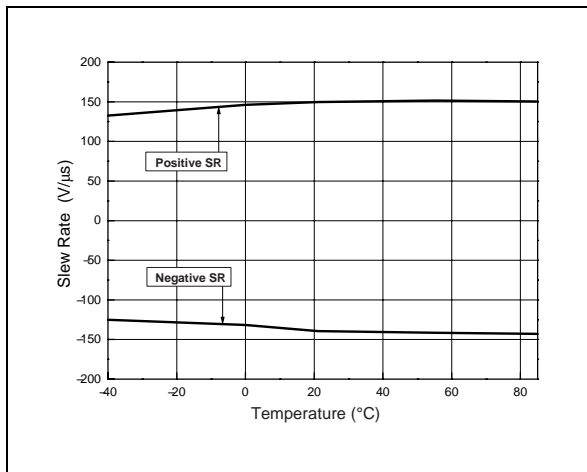
**Figure 18 : Negative Slew Rate**  
 $A_V= - 4$ ,  $R_{fb}=620\Omega$ ,  $V_{CC}=\pm 6V$ ,  $R_L=25\Omega$



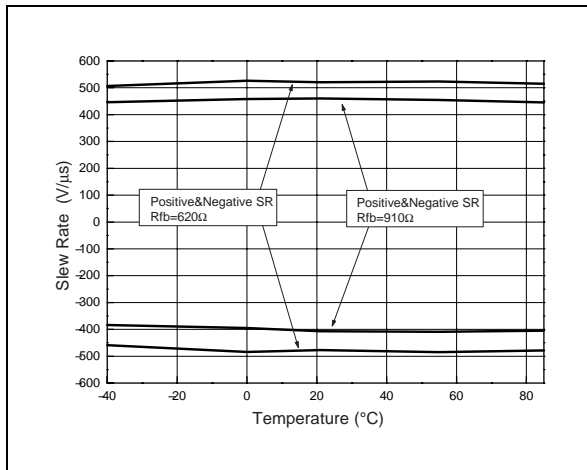
**Figure 19 : Negative Slew Rate**  
 $A_V = -4$ ,  $R_{fb} = 910\Omega$ ,  $V_{CC} = \pm 2.5V$ ,  $R_L = 10\Omega$



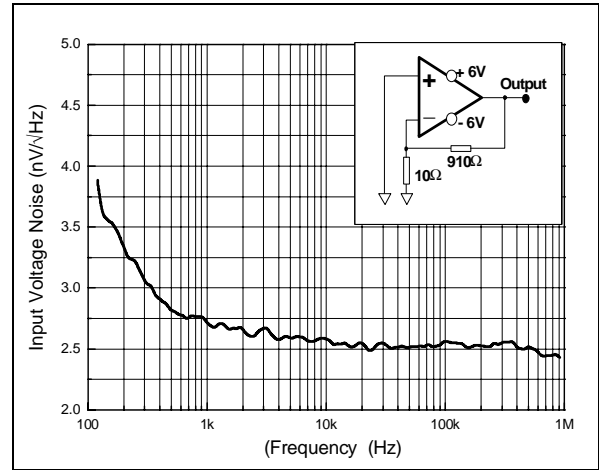
**Figure 20 : Slew Rate vs. Temperature**  
 $A_V = +4$ ,  $R_{fb} = 910\Omega$ ,  $V_{CC} = \pm 2.5V$ ,  $R_L = 10\Omega$



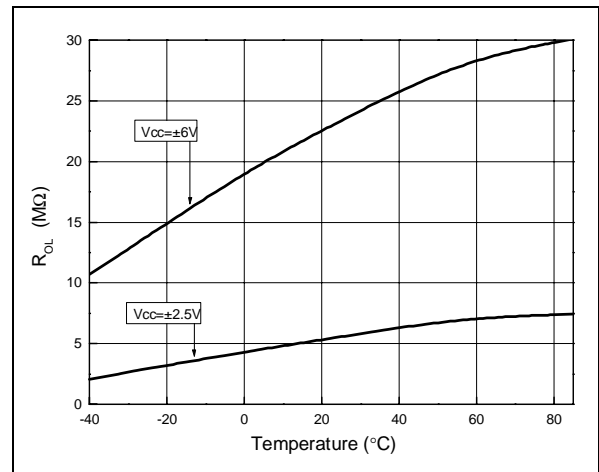
**Figure 21 : Slew Rate vs. Temperature**  
 $A_V = +4$ ,  $R_{fb} = 910\Omega$ ,  $V_{CC} = \pm 6V$ ,  $R_L = 25\Omega$



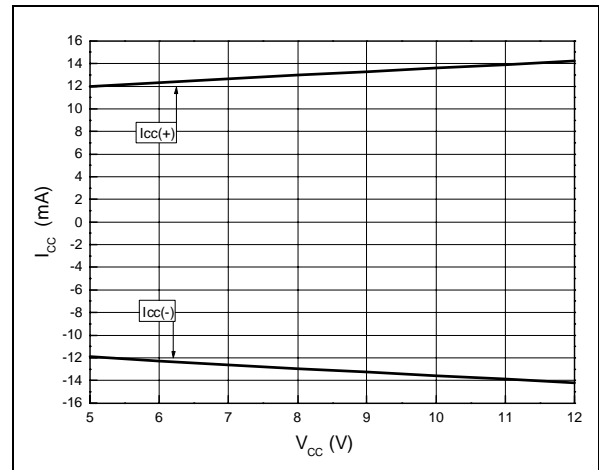
**Figure 22 : Input Voltage Noise Level**  
 $A_V = +92$ ,  $R_{fb} = 910\Omega$ , Input+ connected to Gnd via  $10\Omega$



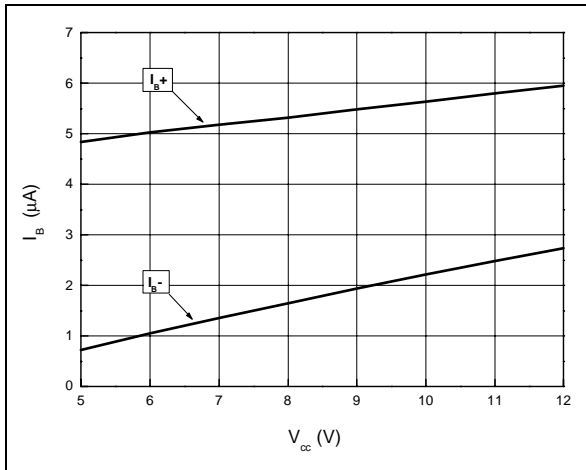
**Figure 23 : Transimpedance vs. Temperature**  
 Open Loop



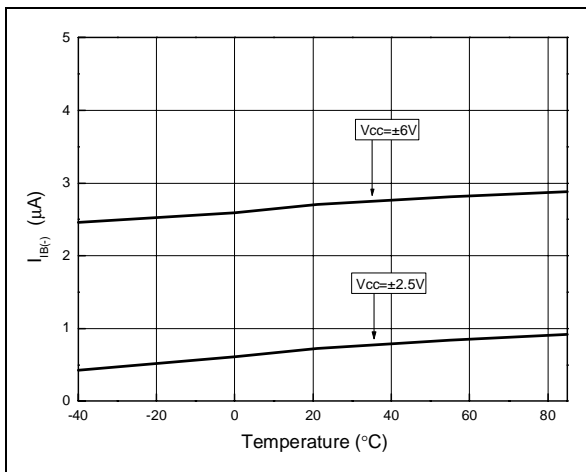
**Figure 24 : I<sub>CC</sub> vs. Power Supply**  
 Open loop, no load



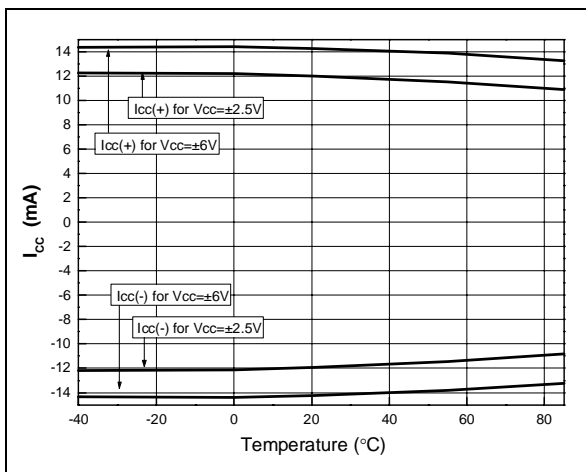
**Figure 25 :  $I_{B}$  vs. Power Supply**  
Open loop, no load



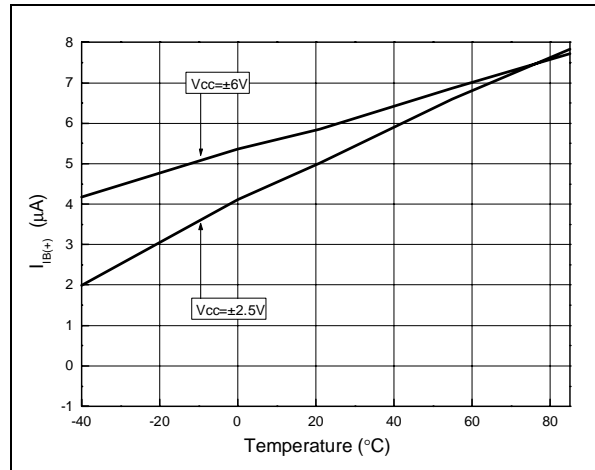
**Figure 26 :  $I_{B(-)}$  vs. Temperature**  
Open loop, no load



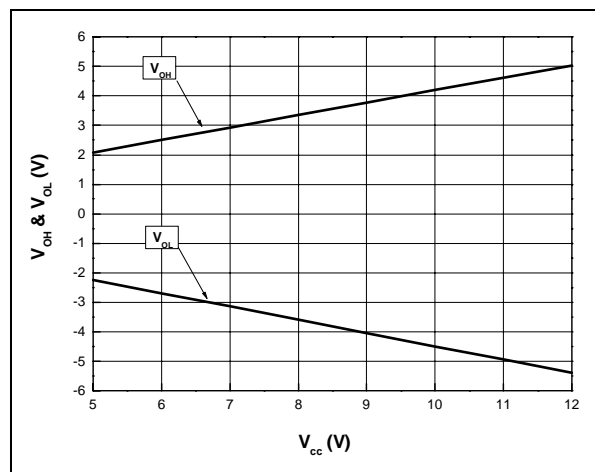
**Figure 27 :  $I_{CC}$  vs. Temperature**  
Open loop, no load



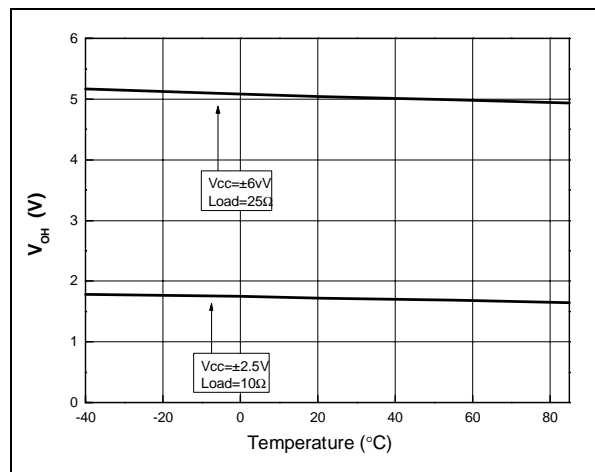
**Figure 28 :  $I_{B(+)}$  vs. Temperature**  
Open loop, no load



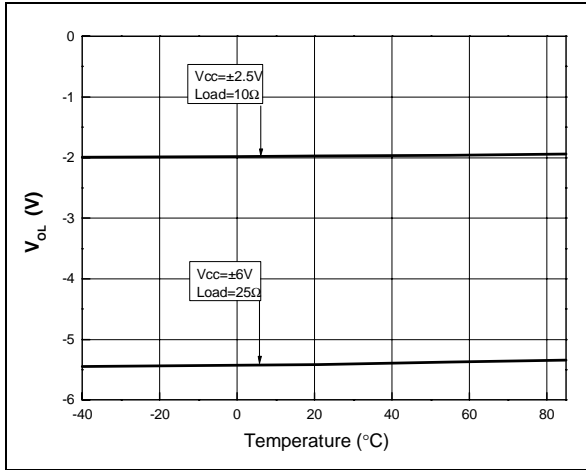
**Figure 29 :  $V_{OH}$  &  $V_{OL}$  vs. Power Supply**  
Open loop,  $R_L = 25\Omega$



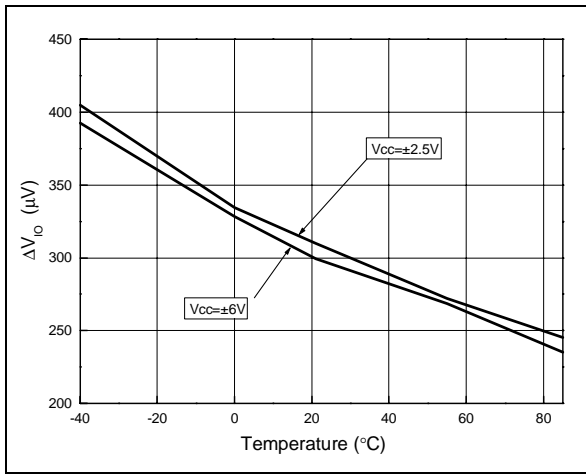
**Figure 30 :  $V_{OH}$  vs. Temperature**  
Open loop



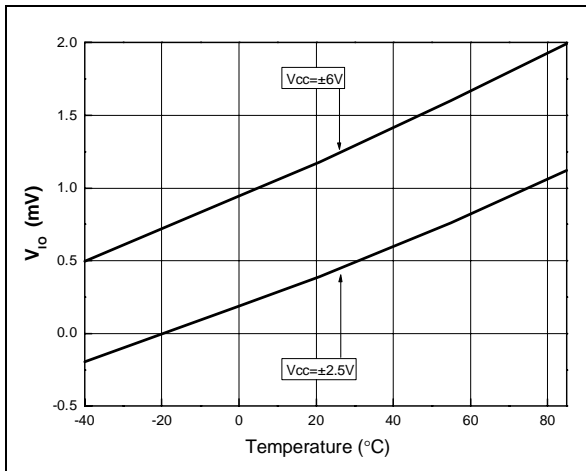
**Figure 31 :  $V_{oL}$  vs. Temperature**  
Open loop



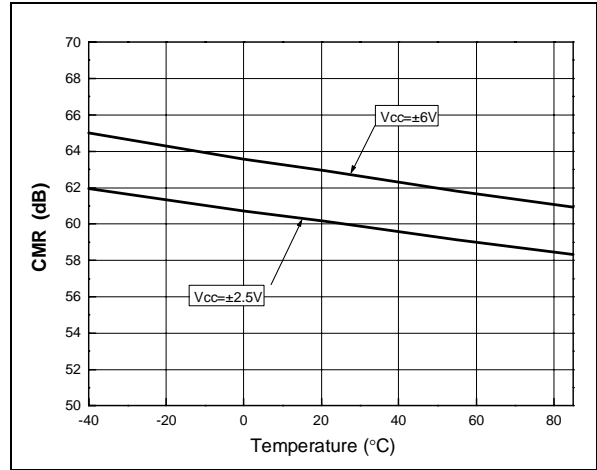
**Figure 32 : Differential  $V_{io}$  vs. Temperature**  
Open loop, no load



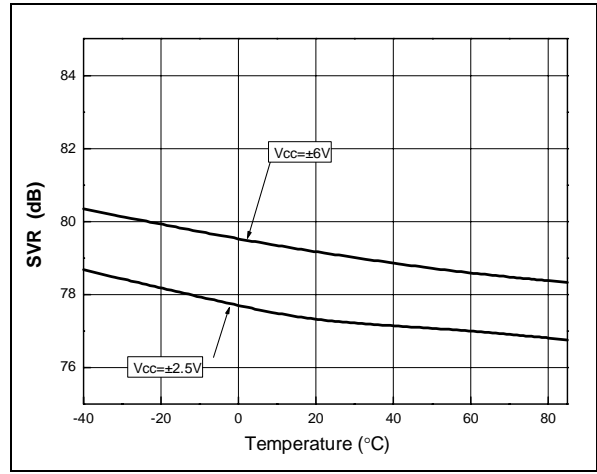
**Figure 33 :  $V_{io}$  vs. Temperature**  
Open loop, no load



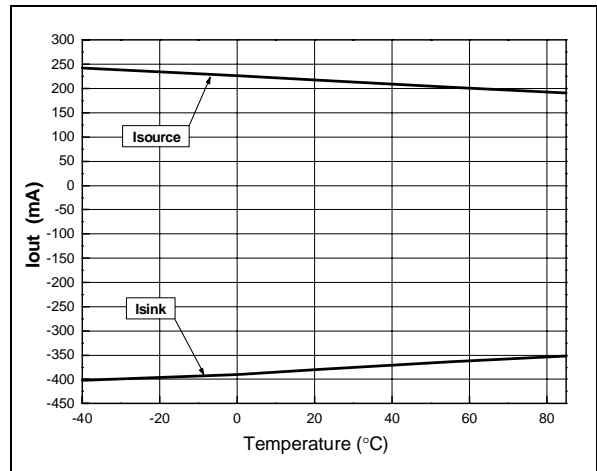
**Figure 34 : CMR vs. Temperature**  
Open loop, no load



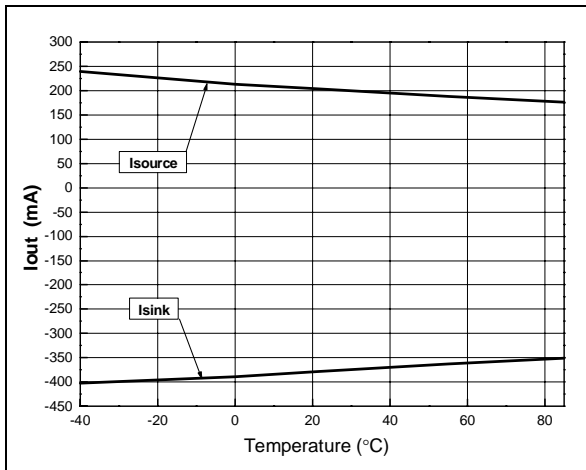
**Figure 35 : SVR vs. Temperature**  
Open loop, no load



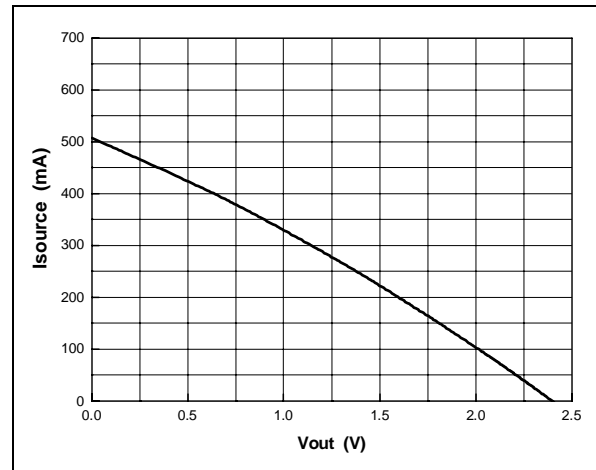
**Figure 36 :  $i_{out}$  vs. Temperature**  
Open loop,  $V_{CC}=\pm 6V$ ,  $R_L=10\Omega$



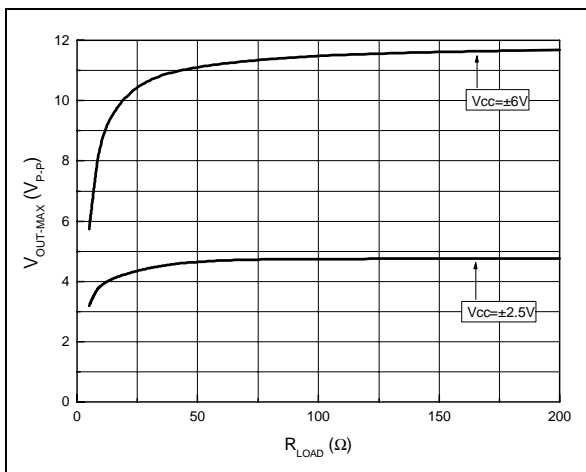
**Figure 37 : Iout vs. Temperature**  
Open loop,  $V_{CC}=\pm 2.5V$ ,  $R_L=25\Omega$



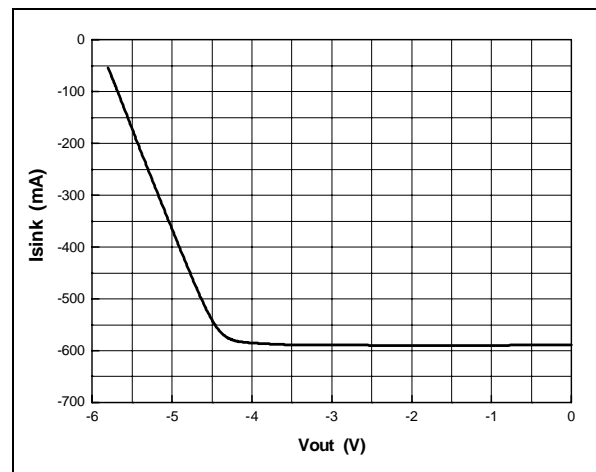
**Figure 40 : Isource vs. Output Amplitude.**  
 $V_{CC}=\pm 2.5V$ , Open Loop, no Load



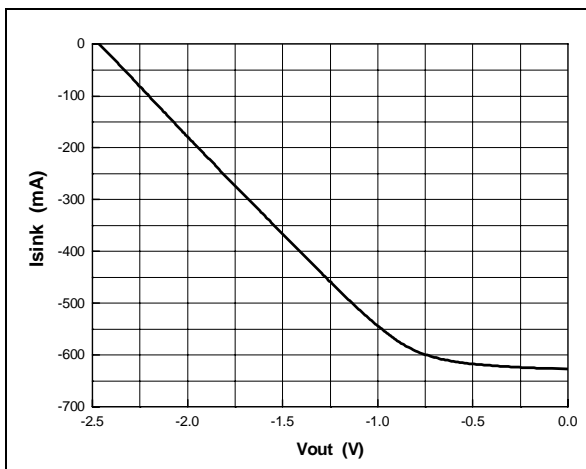
**Figure 38 : Maximum Output Amplitude vs. Load**  
 $A_V=+4$ ,  $R_{fb}=620\Omega$ ,  $V_{CC}=\pm 6V$



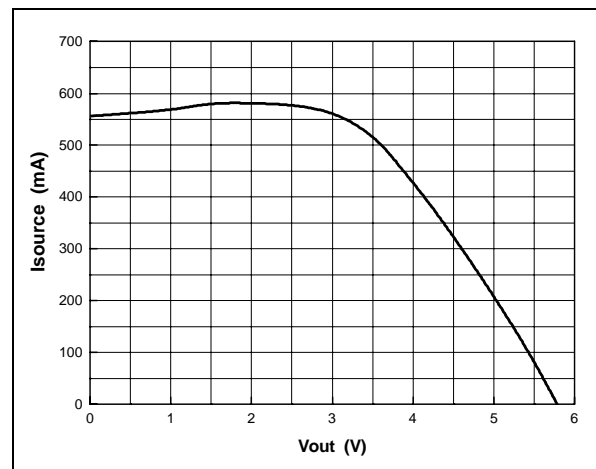
**Figure 41 : Isink vs. Output Amplitude**  
 $V_{CC}=\pm 6V$ , Open Loop, no Load



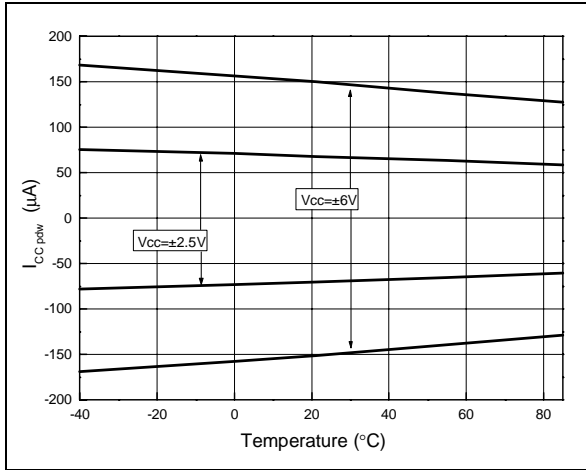
**Figure 39 : Isink vs. Output Amplitude.**  
 $V_{CC}=\pm 2.5V$ , Open Loop, no Load



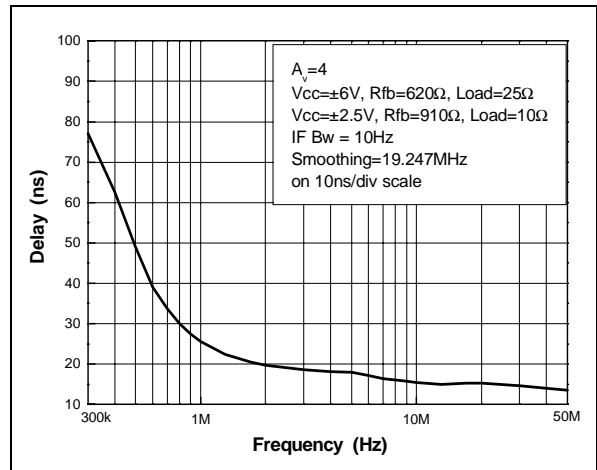
**Figure 42 : Isource vs. Output Amplitude**  
 $V_{CC}=\pm 6V$ , Open Loop, no Load



**Figure 43 : I<sub>CC</sub> (Power Down) vs. Temperature**  
 No load, Open Loop



**Figure 44 : Group Delay**  
 $V_{CC} = \pm 6\text{V}$ ,  $V_{CC} = \pm 2.5\text{V}$



**INTERMODULATION DISTORTION PRODUCT**

A non-ideal output of the amplifier can be described by the following development :

$$V_{out} = C_0 + C_1 V_{in} + C_2 V_{in}^2 + \dots C_n V_{in}^n$$

due to a non-linearity in the input-output amplitude transfer. In the case of the input is  $V_{in}=A \sin \omega t$ ,  $C_0$  is the DC component,  $C_1(V_{in})$  is the fundamental,  $C_n$  is the amplitude of the harmonics of the output signal  $V_{out}$ .

A one-frequency (one-tone) input signal contributes to a harmonic distortion. A two-tones input signal contributes to a harmonic distortion and intermodulation product.

This intermodulation product or intermodulation distortion study of a two-tones input signal is the first step of the amplifier characterization of driving capability in the case of a multi-tone signal.

In this case :

$$+ C_2(A \sin \omega_1 t + B \sin \omega_2 t)^2$$

$$\dots + C_n(A \sin \omega_1 t + B \sin \omega_2 t)^n$$

$$V_{in} = A \sin \omega_1 t + B \sin \omega_2 t$$

$$V_{out} = C_0 + C_1(A \sin \omega_1 t + B \sin \omega_2 t)$$

and :

$$+ C_1(A \sin \omega_1 t + B \sin \omega_2 t)$$

$$- \frac{C_2}{2}(A^2 \cos 2\omega_1 t + B^2 \cos 2\omega_2 t)$$

$$+ 2C_2AB(\cos(\omega_1 - \omega_2)t - \cos(\omega_1 + \omega_2)t)$$

$$+ \left(3 \frac{C_3}{4}\right) \neq$$

$$+ (C_3 A^3 \sin 3\omega_1 t + B^3 \sin 3\omega_2 t)$$

$$+ \frac{3C_3 A^2 B}{2} \left( \sin(2\omega_1 - \omega_2)t - \frac{1}{2} \sin(2\omega_1 + \omega_2)t \right)$$

$$+ \frac{3C_3 A B^2}{2} \left( \sin(-\omega_1 + 2\omega_2)t - \frac{1}{2} \sin(\omega_1 + 2\omega_2)t \right)$$

$$\dots + C_n(V_{in})^n$$

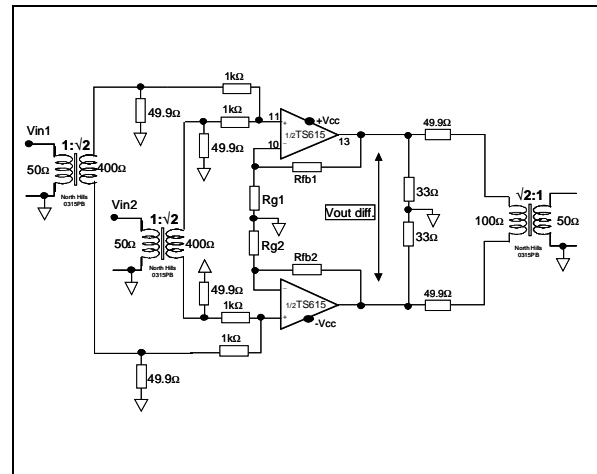
$$V_{out} = C_0 + C_2 \left( \frac{A^2 + B^2}{2} \right)$$

$$\left( A^3 \sin \omega_1 t + B^3 \sin \omega_2 t + 2A^2 B \sin \omega_1 t + 2AB^2 \sin \omega_2 t \right)$$

In this expression, we recognize the second order intermodulation IM2 by the frequencies  $(\omega_1 - \omega_2)$  and  $(\omega_1 + \omega_2)$  and the third order intermodulation IM3 by the frequencies  $(2\omega_1 - \omega_2)$ ,  $(2\omega_1 + \omega_2)$ ,  $(-\omega_1 + 2\omega_2)$  and  $(\omega_1 + 2\omega_2)$ .

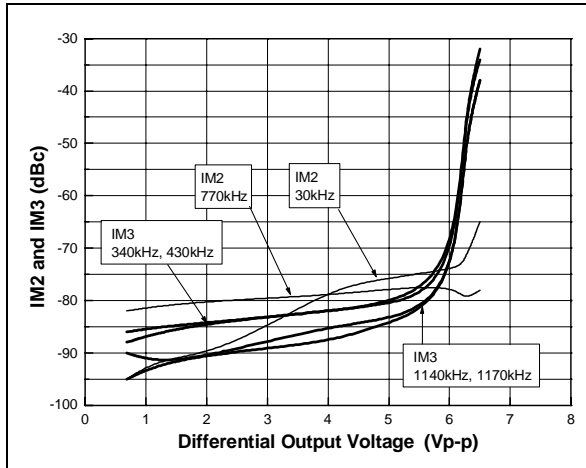
The measurement of the intermodulation product of the driver is achieved by using the driver as a mixer by a summing amplifier configuration. By this way, the non-linearity problem of an external mixing device is avoided.

**Figure 45 : Non-inverting Summing Amplifier**

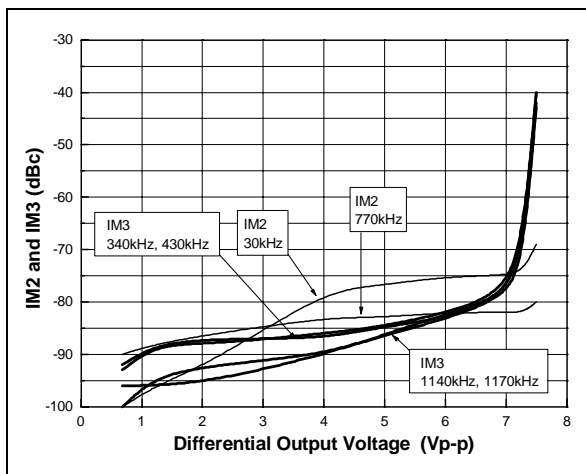


The following graphs show the IM2 and the IM3 of the amplifier in different configuration. The two-tones input signal is achieved by the multi-source generator Marconi 2026. Each tone has the same amplitude. The measurement is achieved by the spectrum analyzer HP3585A.

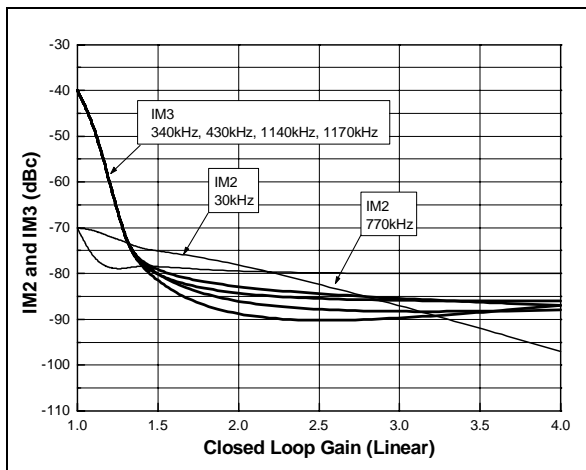
**Figure 46 : Intermodulation vs. Output Amplitude**  
 370kHz & 400kHz,  $A_V=+1.5$ ,  $R_{fb}=1k\Omega$ ,  $R_L=14\Omega$  diff.,  $V_{CC}=\pm 2.5V$



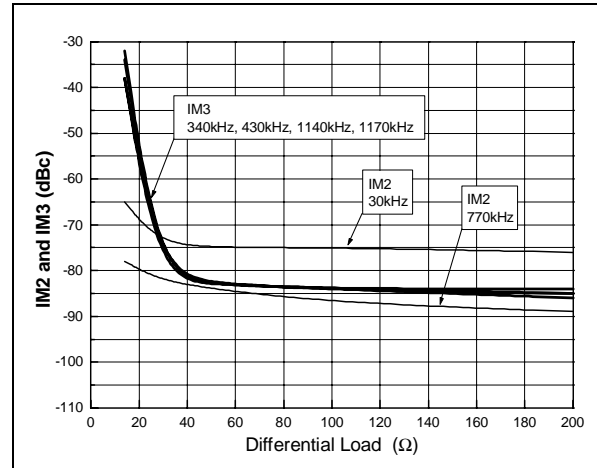
**Figure 47 : Intermodulation vs. Output Amplitude**  
 370kHz & 400kHz,  $A_V=+1.5$ ,  $R_{fb}=1k\Omega$ ,  $R_L=28\Omega$  diff.,  $V_{CC}=\pm 2.5V$



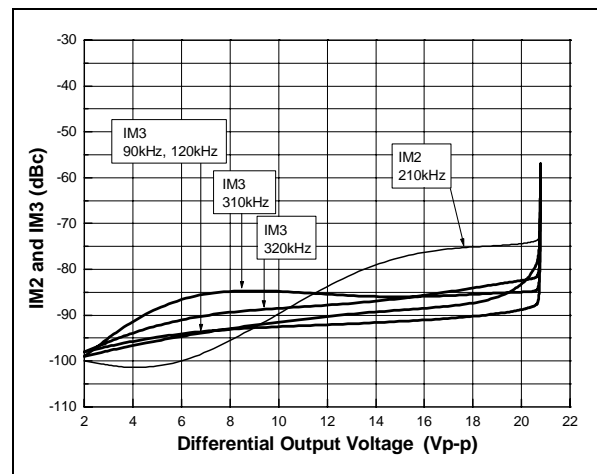
**Figure 48 : Intermodulation vs. Gain**  
 370kHz & 400kHz,  $R_L=20\Omega$  diff.,  $V_{out}=6V_{pp}$ ,  $V_{CC}=\pm 2.5V$



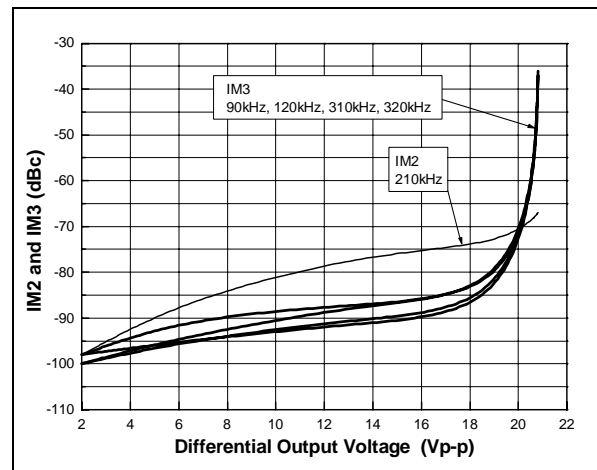
**Figure 49 : Intermodulation vs. Load**  
 370kHz & 400kHz,  $A_V=+1.5$ ,  $R_{fb}=1k\Omega$ ,  $V_{out}=6.5V_{pp}$ ,  $V_{CC}=\pm 2.5V$



**Figure 50 : Intermodulation vs. Output Amplitude**  
 100kHz & 110kHz,  $A_V=+4$ ,  $R_{fb}=620\Omega$ ,  $R_L=200\Omega$  diff.,  $V_{CC}=\pm 6V$

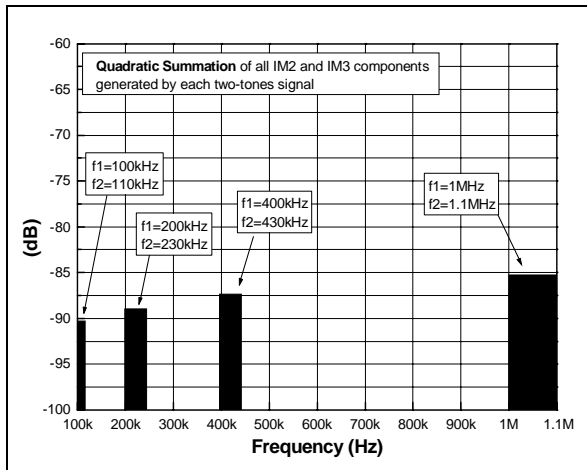


**Figure 51 : Intermodulation vs. Output Amplitude**  
 100kHz & 110kHz,  $A_V=+4$ ,  $R_{fb}=620\Omega$ ,  $R_L=50\Omega$  diff.,  $V_{CC}=\pm 6V$

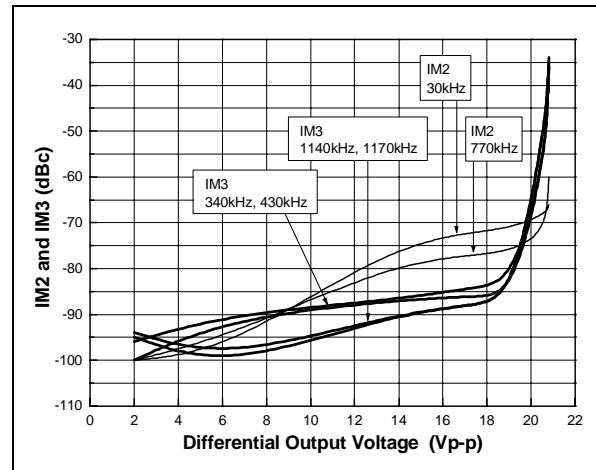




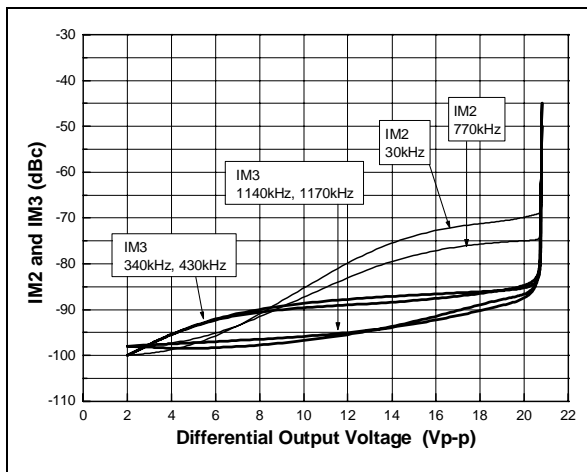
**Figure 52 : Intermodulation vs. Frequency Range**  
 $A_V=+4$ ,  $R_{fb}=620\Omega$ ,  $R_L=50\Omega$  diff.,  $V_{out}=16V_{pp}$ ,  $V_{CC}=\pm 6V$



**Figure 54 : Intermodulation vs. Output Amplitude**  
 370kHz & 400kHz,  $A_V=+4$ ,  $R_{fb}=620\Omega$ ,  $R_L=50\Omega$  diff.,  $V_{CC}=\pm 6V$



**Figure 53 : Intermodulation vs. Output Amplitude**  
 370kHz & 400kHz,  $A_V=+4$ ,  $R_{fb}=620\Omega$ ,  $R_L=200\Omega$  diff.,  $V_{CC}=\pm 6V$



**PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS**

In this range of frequency, printed circuit board parasites can affect the closed-loop performance.

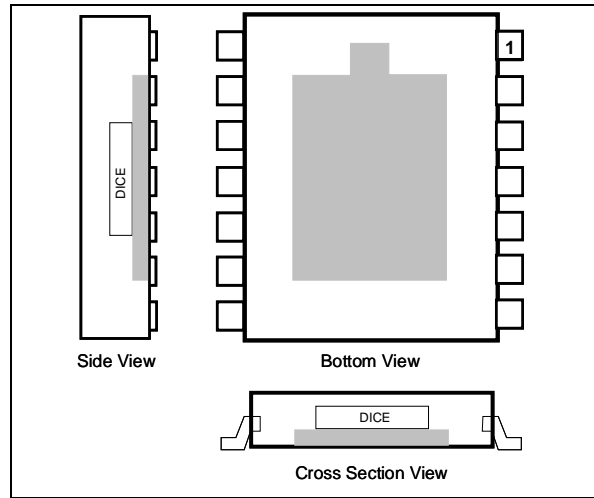
The implementation of a proper ground plane in both sides of the PCB is mandatory to provide low inductance and low resistance common return. Most important for controlling the gain flatness and the bandwidth are stray capacitances at the output and inverting input. For minimizing the coupling, the space between signal lines and ground plane will be increased. Connections of the feedback components must be as short as possible in order to decrease the associated inductance which affect high frequency gain errors. It is very important to choose external components as small as possible such as surface mounted devices, SMD, in order to minimize the size of all the DC and AC connections.

**THERMAL INFORMATION**

The TS615 is housed in an Exposed-Pad plastic package. As described on the figure 56, this package uses a lead frame upon which the dice is mounted. This lead frame is exposed as a thermal pad on the underside of the package. The thermal contact is direct with the dice. This thermal path provide an excellent thermal performance.

The thermal pad is electrically isolated from all pins in the package. It should be soldered to a copper area of the PCB underneath the package. Through these thermal paths within this copper area, heat can be conducted away from the package. In this case, the copper area should be connected to (-V<sub>CC</sub>).

**Figure 55 : Exposed-Pad Package**



**Figure 56 : Evaluation Board**

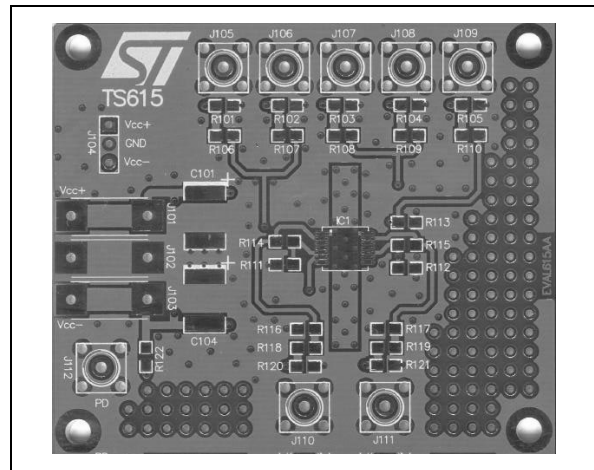


Figure 57 : Schematic Diagram

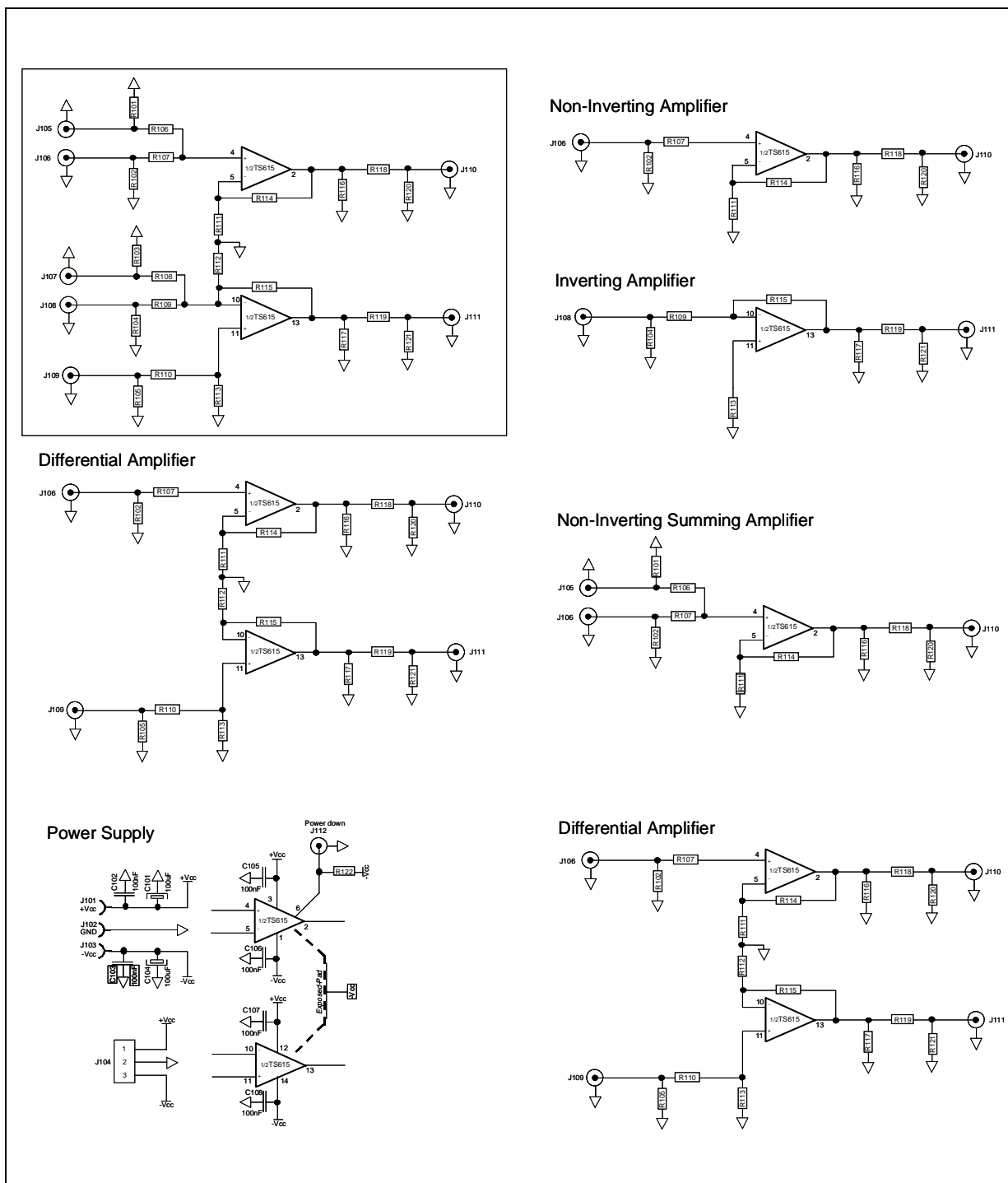


Figure 58 : Component Locations - Top Side

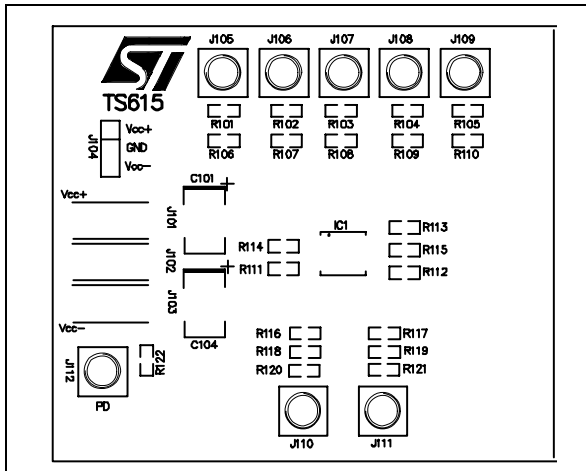


Figure 60 : Top Side Board Layout

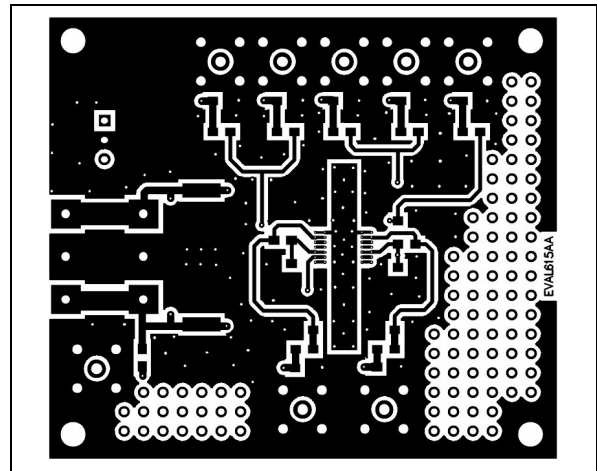


Figure 59 : Component Locations - Bottom Side

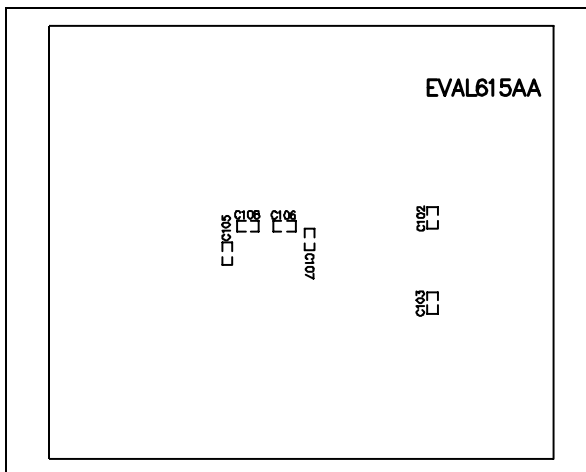
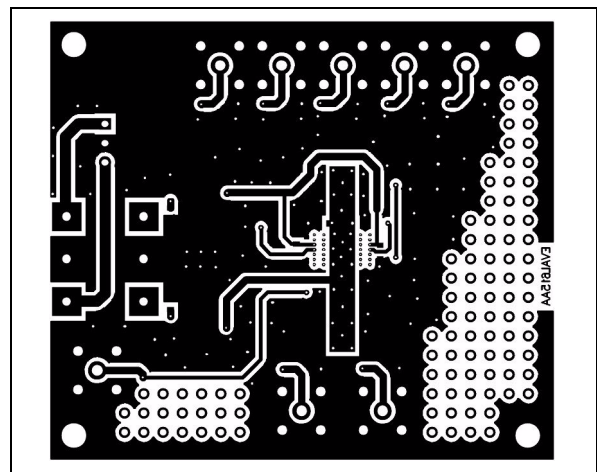
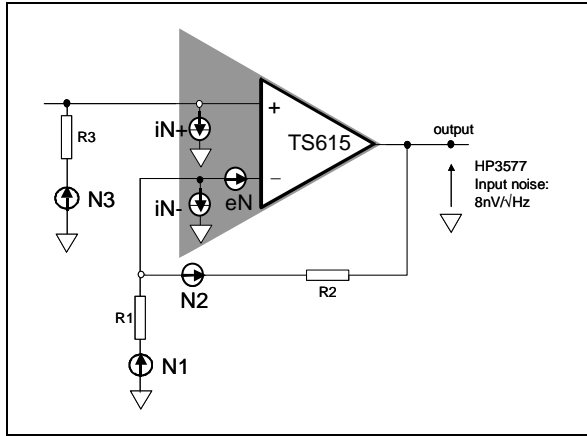


Figure 61 : Bottom Side Board Layout



**NOISE MEASUREMENT**

**Figure 62 : Noise Model**



eN : input voltage noise of the amplifier  
 iNn : negative input current noise of the amplifier  
 iNp : positive input current noise of the amplifier  
 The closed loop gain is :

$$A_V = g = 1 + \frac{R_{fb}}{R_g}$$

The six noise sources are :

$$V_2 = iNn \times R_2$$

$$V_5 = \sqrt{4kTR_2}$$

$$V_1 = eN \times \left(1 + \frac{R_2}{R_1}\right)$$

$$V_3 = iNp \times R_3 \times \left(1 + \frac{R_2}{R_1}\right)$$

$$V_4 = \frac{R_2}{R_1} \times \sqrt{4kTR_1}$$

$$V_6 = \left(1 + \frac{R_2}{R_1}\right) \sqrt{4kTR_3}$$

Assuming the thermal noise of a resistance R as:

$$\sqrt{4kTR\Delta F}$$

with ΔF the specified bandwidth.

On 1Hz bandwidth the thermal noise is reduced to

$$\sqrt{4kTR}$$

k is the Boltzmann's constant equals to 1,374.10<sup>-23</sup>J/°K. T is the temperature (°K).

The output noise eNo is calculated using the Superposition Theorem. But it is not the sum of all noise sources. The output noise is the square root of the sum of the square of each noise source.

$$eNo = \sqrt{V_1^2 + V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}, (eq1)$$

$$eNo^2 = eN^2 \times g^2 + iNn^2 \times R_2^2 + iNp^2 \times R_3^2 \times g^2 + \left(\frac{R_2}{R_1}\right)^2 \times 4kTR_1 + 4kTR_2 + \left(1 + \frac{R_2}{R_1}\right)^2 \times 4kTR_3, (eq2)$$

The input noise of the instrumentation must be extracted from the measured noise value. The real output noise value of the driver is:

$$eNo = \sqrt{(\text{Measured})^2 - (\text{instrumentation})^2}, (eq3)$$

The input noise is called the Equivalent Input Noise as it is not directly measured but it is evaluated from the measurement of the output divided by the closed loop gain (eNo/g).

After simplification of the fourth and the fifth term of (eq2) we obtain:

$$eNo^2 = eN^2 \times g^2 + iNn^2 \times R_2^2 + iNp^2 \times R_3^2 \times g^2 + g \times 4kTR_2 + \left(1 + \frac{R_2}{R_1}\right)^2 \times 4kTR_3, (eq4)$$

**Measurement of eN:**

We assume a short-circuit on the non-inverting input (R3=0). (eq4) comes:

$$eNo = \sqrt{eN^2 \times g^2 + iNn^2 \times R_2^2 + g \times 4kTR_2}, (eq5)$$

In order to easily extract the value of eN, the resistance R2 will be chosen as low as possible. In the other hand, the gain must be large enough.

R1=10Ω, R2=910Ω, R3=0, Gain=92

Equivalent Input Noise: 2.57nV/√Hz

**Input Voltage Noise: eN=2.5nV/√Hz**

**Measurement of iNn:**

R3=0 and the output noise equation is still the (eq5). This time the gain must be decreased to decrease the thermal noise contribution.

R1=100Ω, R2=910Ω, R3=0, Gain=10.1

Equivalent Input Noise: 3.40nV/√Hz

**Negative Input Current Noise: iNn =21pA/√Hz**

**Measurement of iNp:**

To extract iNp from (eq3), a resistance R3 is connected to the non-inverting input. The value of R3 must be chosen in order to keep its thermal noise contribution as low as possible against the iNp contribution.

R1=100Ω, R2=910Ω, R3=100Ω, Gain=10.1

Equivalent Input Noise: 3.93nV/√Hz

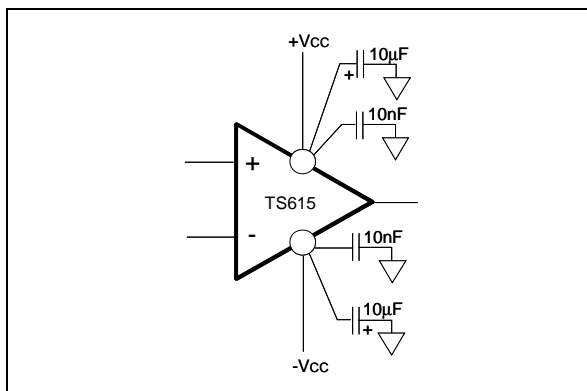
**Positive Input Current Noise: iNp=15pA/√Hz**

Conditions: frequency=100kHz, V<sub>CC</sub>=±2.5V  
 Instrumentation: Spectrum Analyzer HP3585A  
 (input noise of the HP3585A: 8nV/√Hz)

**POWER SUPPLY BYPASSING**

A proper power supply bypassing comes very important for optimizing the performance in high frequency range. Bypass capacitors should be placed as close as possible to the IC pins to improve high frequency bypassing. A capacitor greater than 1μF is necessary to minimize the distortion. For a better quality bypassing a capacitor of 10nF is added following the same condition of implementation. These bypass capacitors must be incorporated for the negative and the positive supply.

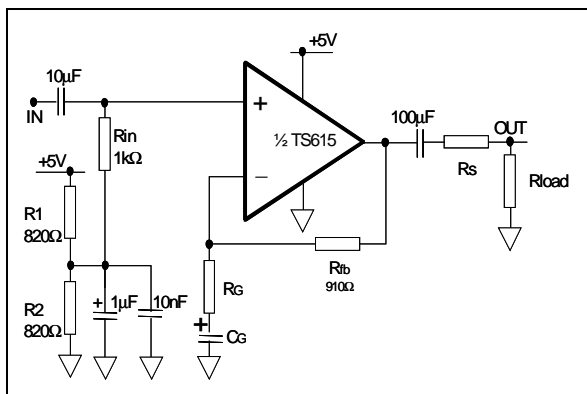
**Figure 63 :** Circuit for Power Supply Bypassing



**SINGLE POWER SUPPLY**

The following figure show the case of a 5V single power supply configuration

**Figure 64 :** Circuit for +5V single supply



The TS615 operates from 12V down to 5V power supplies. This is achieved with a dual power supply of ±6V and ±2.5V or a single power supply of 12V and 5V referenced to the ground. In the case of this asymmetrical supplying, a new biasing is

necessary to assume a positive output dynamic range between 0V and +V<sub>CC</sub> supply rails. Considering the values of V<sub>OH</sub> and V<sub>OL</sub>, the amplifier will provide an output dynamic from +0.5V to 10.6V on 25Ω load for a 12V supplying, from 0.45V to 3.8V on 10Ω load for a 5V supplying.

The amplifier must be biased with a mid supply (nominally +V<sub>CC</sub>/2), in order to maintain the DC component of the signal at this value. Several options are possible to provide this bias supply (such as a virtual ground using an operational amplifier), or a two-resistance divider which is the cheapest solution. A high resistance value is required to limit the current consumption. On the other hand, the current must be high enough to bias the non-inverting input of the amplifier. If we consider this bias current (30μA max.) as the 1% of the current through the resistance divider to keep a stable mid supply, two resistances of 2.2kΩ can be used in the case of a 12V power supply and two resistances of 820Ω can be used in the case of a 5V power supply.

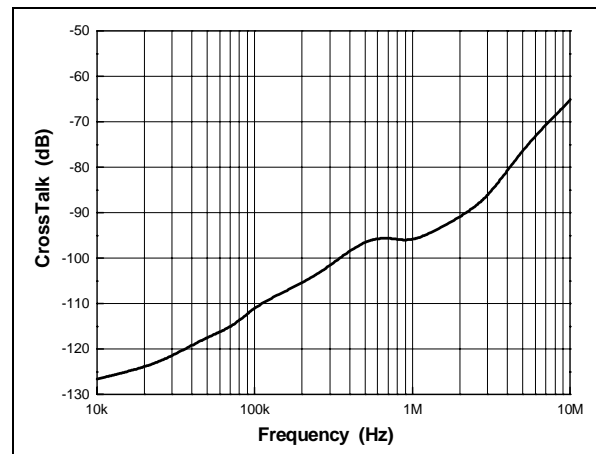
The input provides a high pass filter with a break frequency below 10Hz which is necessary to remove the original 0 volt DC component of the input signal, and to fix it at +V<sub>CC</sub>/2.

**CHANNEL SEPARATION - CROSSTALK**

The following figure show the crosstalk from an amplifier to a second amplifier. This phenomenon, accentuated in high frequencies, is unavoidable and intrinsic of the circuit.

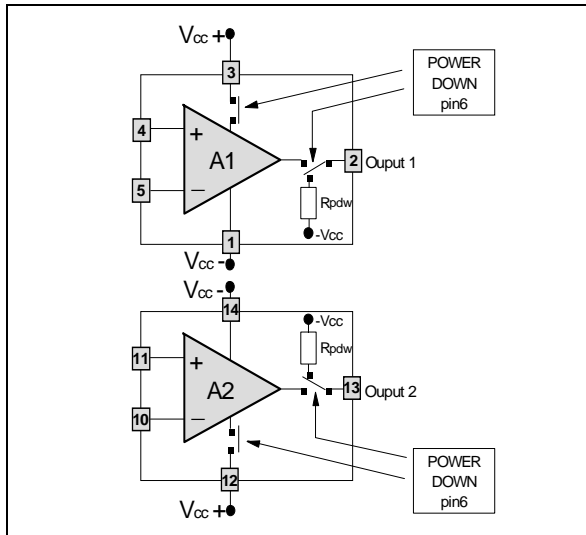
Nevertheless, the PCB layout has also an effect on the crosstalk level. Capacitive coupling between signal wires, distance between critical signal nodes, power supply bypassing, are the most significant points.

**Figure 65 :** Crosstalk vs. Frequency  
 $A_V=+4$ ,  $R_{fb}=620\Omega$ ,  $V_{CC}=\pm 6V$ ,  $V_{out}=2Vp$



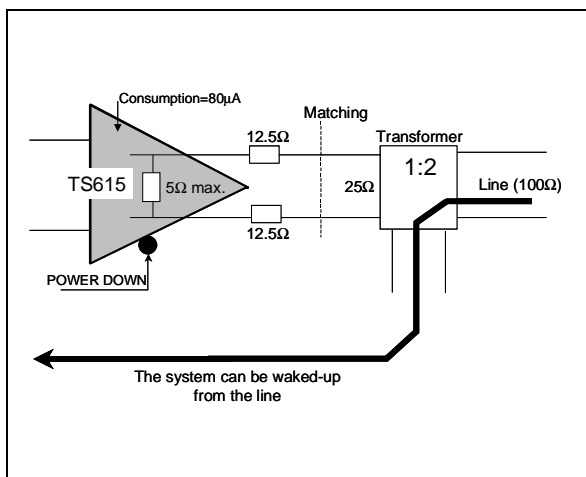
**POWER DOWN MODE BEHAVIOUR**

**Figure 66 : Equivalent Schematic**

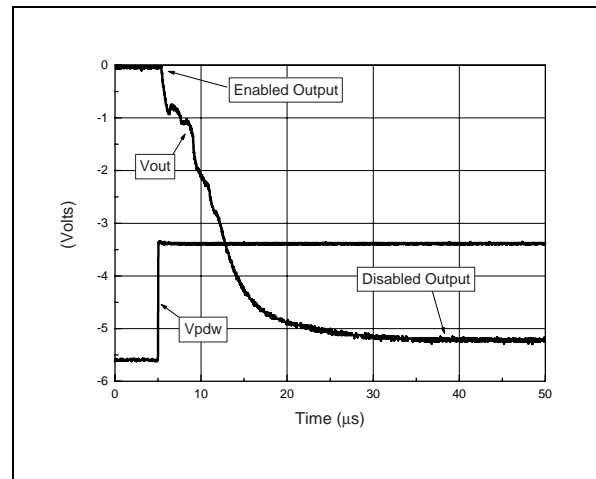


Please note that the short circuited output in power down mode is referenced to (-V<sub>CC</sub>). No problem appears when used in differential mode. Nevertheless, when used in single ended on a load referenced to GND, the (-V<sub>CC</sub>) level contributes to a current consumption through the load. As described on the Figure 68, the interest of featuring an output short circuit in power down mode is to keep the best impedance matching between the system and the twisted pair telephone line when the modem is in sleep mode. By this way, the modem can be waked-up with a signal from the line without any damage of this signal. This concept is particularly intended for the ADSL over voice modems, where the modem in sleep mode, must be waked-up by the phone call.

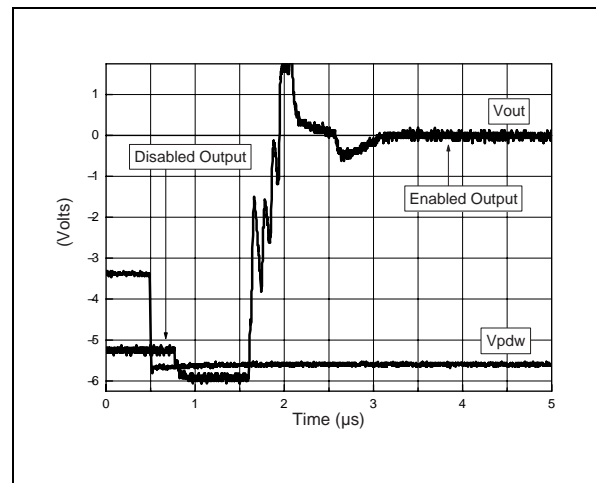
**Figure 67 : Matching in Sleep Mode**



**Figure 68 : Standby Mode. Time On>Off**

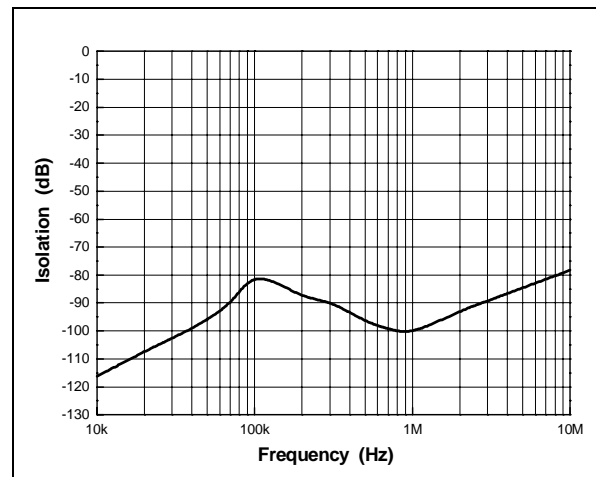


**Figure 69 : Standby Mode. Time Off>On**



**Figure 70 : Standby Mode. Input/Output Isolation vs. Frequency**

$A_V=+4$ ,  $R_{fb}=620\Omega$ ,  $V_{CC}=\pm 6V$ ,  $V_{out}=3Vp$



**CHOICE OF THE FEEDBACK CIRCUIT**

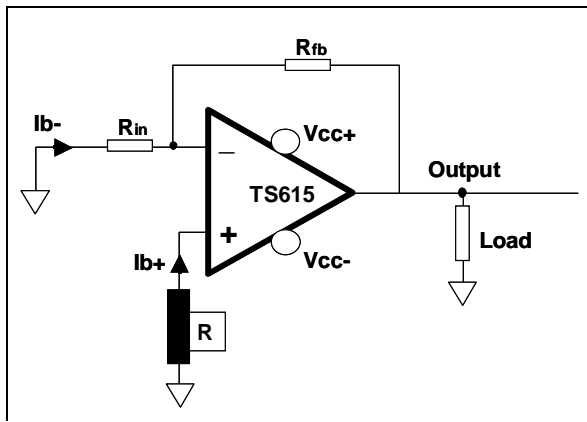
**Table 71** : Closed-Loop Gain - Feedback Components

V <sub>cc</sub> (V)	Gain	R <sub>fb</sub> (Ω)
±6	+1	750
	+2	680
	+4	620
	+8	510
	-1	680
	-2	680
	-4	620
	-8	510
±2.5	+1	1.1k
	+2	1k
	+4	910
	+8	680
	-1	1k
	-2	1k
	-4	910
	-8	680

**INVERTING AMPLIFIER BIASING**

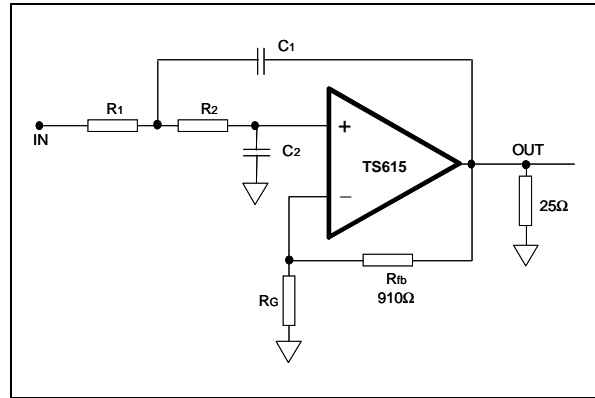
In this case a resistance is necessary to achieve a good input biasing, as R on (fig.30). This resistance is calculated by assuming the negative and positive input bias current. The aim is to make the compensation of the offset bias current which could affect the input offset voltage and the output DC component. Assuming I<sub>b-</sub>, I<sub>b+</sub>, R<sub>in</sub>, R<sub>fb</sub> and a zero volt output, the resistance R comes: R = R<sub>in</sub> // R<sub>fb</sub>.

**Figure 72** : Compensation of the Input Bias Current



**ACTIVE FILTERING**

**Figure 73** : Low-Pass Active Filtering. Sallen-Key



The resistors R<sub>fb</sub> and R<sub>G</sub> give directly the gain of the filter as a classical non-inverting amplification configuration :

$$A_V = g = 1 + \frac{R_{fb}}{R_g}$$

Assuming the following expression as the response of the system:

$$T_{j\omega} = \frac{V_{out_{j\omega}}}{V_{in_{j\omega}}} = \frac{g}{1 + 2\zeta \frac{j\omega}{\omega_c} + \frac{(j\omega)^2}{\omega_c^2}}$$

the cutoff frequency is not gain dependent and it comes:

$$\omega_c = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

the damping factor comes:

$$\zeta = \frac{1}{2} \omega_c (C_1 R_1 + C_1 R_2 + C_2 R_1 - C_1 R_1 g)$$

The higher the gain the more sensitive the damping factor is. When the gain is higher than 1 it is preferable to use some very stable resistors and capacitors values.

In the case of R<sub>1</sub>=R<sub>2</sub>:

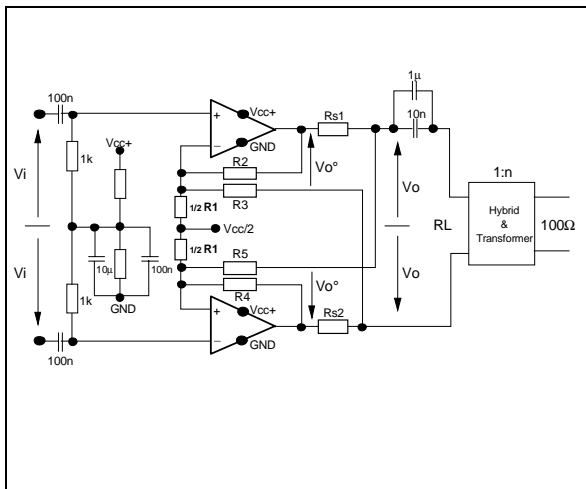
$$\zeta = \frac{2C_2 - C_1 \frac{R_{fb}}{R_g}}{2\sqrt{C_1 C_2}}$$



**INCREASING THE LINE LEVEL BY USING AN ACTIVE IMPEDANCE MATCHING**

With a passive matching, the output signal amplitude of the driver must be twice the amplitude on the load. To go beyond this limitation an active matching impedance can be used. With this technique, it is possible to keep a good impedance matching with an amplitude on the load higher than the half of the output driver amplitude. This concept is shown in figure 74 for a differential line.

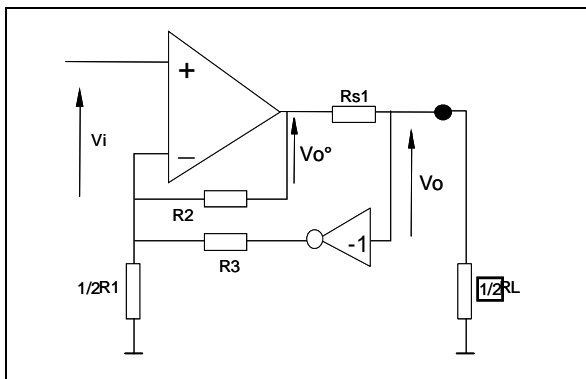
**Figure 74 :** TS615 as a differential line driver with an active impedance matching



**Component Calculation**

Let us consider the equivalent circuit for a single ended configuration, Figure75.

**Figure 75 :** Single ended equivalent circuit



Let us consider the unloaded system. Assuming the currents through R1, R2 and R3 as respectively:

$$\frac{2Vi}{R1}, \frac{(Vi - Vo^\circ)}{R2} \text{ and } \frac{(Vi + Vo)}{R3}$$

As  $Vo^\circ$  equals  $Vo$  without load, the gain in this case becomes :

$$G = \frac{Vo(\text{no load})}{Vi} = \frac{1 + \frac{2R2}{R1} + \frac{R2}{R3}}{1 - \frac{R2}{R3}}$$

The gain, for the loaded system will be (eq1):

$$GL = \frac{Vo(\text{with load})}{Vi} = \frac{1}{2} \frac{1 + \frac{2R2}{R1} + \frac{R2}{R3}}{1 - \frac{R2}{R3}}, (\text{eq1})$$

As shown in figure76, this system is an ideal generator with a synthesized impedance as the internal impedance of the system. From this, the output voltage becomes:

$$Vo = (ViG) - (RoI_{out}), (\text{eq2})$$

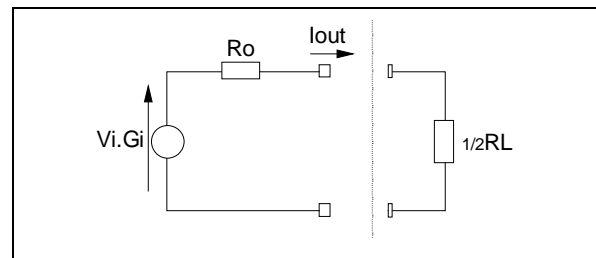
with  $Ro$  the synthesized impedance and  $I_{out}$  the output current. On the other hand  $Vo$  can be expressed as:

$$Vo = \frac{Vi \left( 1 + \frac{2R2}{R1} + \frac{R2}{R3} \right)}{1 - \frac{R2}{R3}} - \frac{Rs1 I_{out}}{1 - \frac{R2}{R3}}, (\text{eq3})$$

By identification of both equations (eq2) and (eq3), the synthesized impedance is, with  $Rs1=Rs2=Rs$ :

$$Ro = \frac{Rs}{1 - \frac{R2}{R3}}, (\text{eq4})$$

**Figure 76 :** Equivalent schematic.  $Ro$  is the synthesized impedance



Unlike the level  $V_o^\circ$  required for a passive impedance,  $V_o^\circ$  will be smaller than  $2V_o$  in our case. Let us write  $V_o^\circ = kV_o$  with  $k$  the matching factor varying between 1 and 2. Assuming that the current through  $R_3$  is negligible, it comes the following resistance divider:

$$R_o = \frac{kV_o R_L}{R_L + 2R_s}$$

After choosing the  $k$  factor,  $R_s$  will equal to  $1/2 R_L(k-1)$ .

A good impedance matching assumes:

$$R_o = \frac{1}{2} R_L, (eq5)$$

From (eq4) and (eq5) it becomes:

$$\frac{R_2}{R_3} = 1 - \frac{2R_s}{R_L}, (eq6)$$

By fixing an arbitrary value of  $R_2$ , (eq6) gives:

$$R_3 = \frac{R_2}{1 - \frac{2R_s}{R_L}}$$

Finally, the values of  $R_2$  and  $R_3$  allow us to extract  $R_1$  from (eq1), and it comes:

$$R_1 = \frac{2R_2}{2\left(1 - \frac{R_2}{R_3}\right)GL - 1 - \frac{R_2}{R_3}}, (eq7)$$

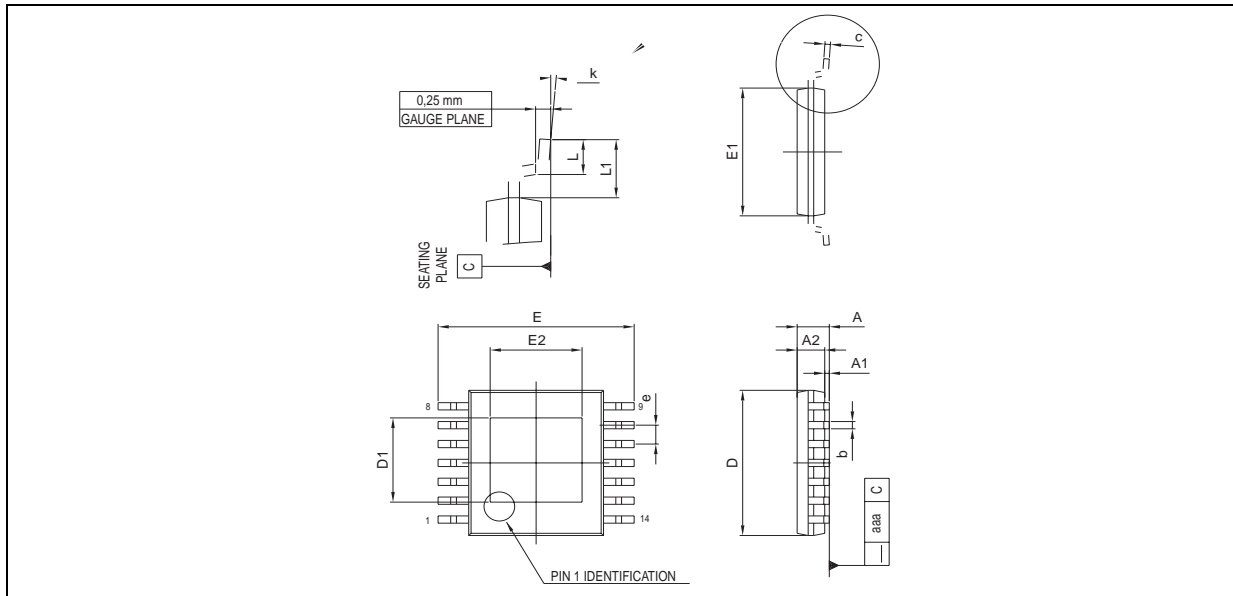
with  $GL$  the required gain.

**Figure 77** : Components Calculation for Impedance Matching Implementation

GL (gain for the loaded system)	GL is fixed for the application requirements $GL = V_o/V_i = 0.5(1 + 2R_2/R_1 + R_2/R_3)/(1 - R_2/R_3)$
R1	$2R_2/[2(1 - R_2/R_3)GL - 1 - R_2/R_3]$
R2 (=R4)	Arbitrary fixed
R3 (=R5)	$R_2/(1 - R_s/0.5R_L)$
$R_s$	$0.5R_L(k-1)$
Load viewed by each driver	$kR_L/2$

**PACKAGE MECHANICAL DATA**

14 PINS - THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP Exposed-Pad)



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.200			0.047
A1			0.150			0.006
A2	0.800	1.000	1.050	0.031	0.039	0.041
b	0.190		0.300	0.007		0.012
c	0.090		0.200	0.004		0.008
D	4.900	5.000	5.100	0.193	0.197	0.201
D1		3.000			1.18	
E	6.200	6.400	6.600	0.244	0.252	0.260
E1	4.300	4.400	4.500	0.169	0.173	0.177
E2		3.000			1.18	
e		0.650			0.026	
L	0.450	0.600	0.750	0.018	0.024	0.030
L1		1.000			0.039	
k	0d		8d	0d		8d
aaa			0.100			0.004

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2002 STMicroelectronics - Printed in Italy - All Rights Reserved  
**STMicroelectronics GROUP OF COMPANIES**

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco  
 Singapore - Spain - Sweden - Switzerland - United Kingdom

© <http://www.st.com>

