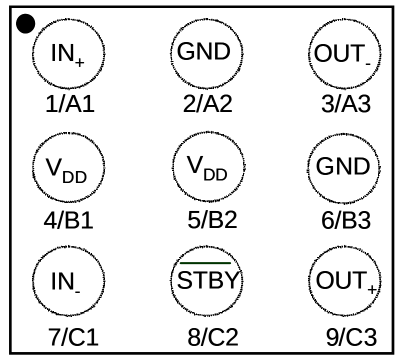
2W Filter-free Class D Audio Power Amplifier

PRELIMINARY DATA

- **Operating from Vcc=2.5V to 5.5V**
- **Standby mode active low**
- **Output power: 1.2W @5V or 0.45W @ 3.0V into 8Ω with 1% THD max.**
- **Adjustable gain via external resistors**
- **Low current consumption 2mA**
- **Efficiency: 87% typ.**
- **SIgnal to noise ratio: 85dB typ.**
- **PSRR: 63dB typ. with 6dB gain**
- **PWM base frequency: 250kHz**
- **Low pop & click noise**
- **Thermal shutdown protection**
- **Available in flip-chip 9 x 300um**

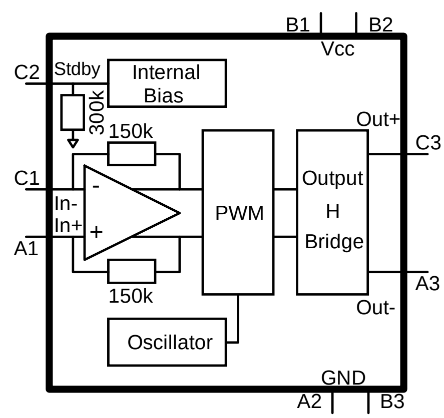
Pin Connections (top view)

TS4962



IN+: positive differential input
IN-: negative differential input
VDD: analog power supply
GND: power supply ground
STBY: standby pin (active low)
OUT+: positive differential output
OUT-: negative differential output

Block Diagram



Description

The TS4962 is a differential class-D B.T.L. power amplifier. Able to drive up to 1.2W into a 8 Ω load at 5V, it achieves outstanding efficiency (87% typ.) compared to classical AB-class audio amps.

Gain of the device can be controlled via two external gain setting resistors.

A POP & CLICK reduction circuitry provides low on/off switch noise while allowing the device to start within 5ms.

A standby function (active low) allows to lower the current consumption to 10nA typ.

The TS4962 is available in a flip-chip package of 9 bumps of 300um diameter.

Applications

- **Cellular Phone**
- **PDA**
- **Notebook PC**

Order Code

Part Number	Temperature Range	Package	Packaging	Marking
TS4962IJT	-40, +85°C	Flip-Chip	Tape & Reel	A62
TS4962EIJT	-40, +85°C	Lead -Free Flip-Chip	Tape & Reel	A62
TS4962EKIJT	-40, +85°C	Lead Free + Back Coating	Tape & Reel	A62

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

1 Absolute Maximum Ratings

Table 1: Key parameters and their absolute maximum ratings

Symbol	Parameter	Value	Unit
VCC	Supply voltage [1]	6	V
V_i	Input Voltage [2]	G_{ND} to V_{CC}	V
T_{oper}	Operating Free Air Temperature Range	-40 to + 85	°C
T_{stg}	Storage Temperature	-65 to +150	°C
T_j	Maximum Junction Temperature	150	°C
R_{thja}	Thermal Resistance Junction to Ambient [3]	200	°C/W
Pd	Power Dissipation	Internally Limited[4]	
ESD	Human Body Model	tbd	kV
ESD	Machine Model	tbd	V
Latch-up	Latch-up Immunity	tbd	mA
V_{STB}	Standby pin voltage maximum voltage [5]	G_{ND} to V_{CC}	V
	Lead Temperature (soldering, 10sec)	260	°C

1) All voltages values are measured with respect to the ground pin.

2) The magnitude of input signal must never exceed V_{CC} + 0.3V / G_{ND} - 0.3V

3) Device is protected in case of over temperature by a thermal shutdown active @ 150°C.

4) Exceeding the power derating curves during a long period, involves abnormal operating condition.

5) The magnitude of standby signal must never exceed V_{CC} + 0.3V / G_{ND} - 0.3V

Table 2: Operating Conditions

Symbol	Parameter	Value	Unit
VCC	Supply Voltage	2.5 to 5.5	V
V_{IC}	Common Mode Input Voltage Range	0.5 to Vcc-0.8	V
VSTB	Standby Voltage Input : [1] Device ON Device OFF	$1.4 \le V_{STB} \le V_{CC}$ $G_{ND} \le V_{STB} \le 0.4$ [2]	V
RL	Load Resistor	≥ 4	Ω
R_{thja}	Thermal Resistance Junction to Ambient [3]	90	°C/W

1) Without any signal on V_{STB}, the device will be in standby

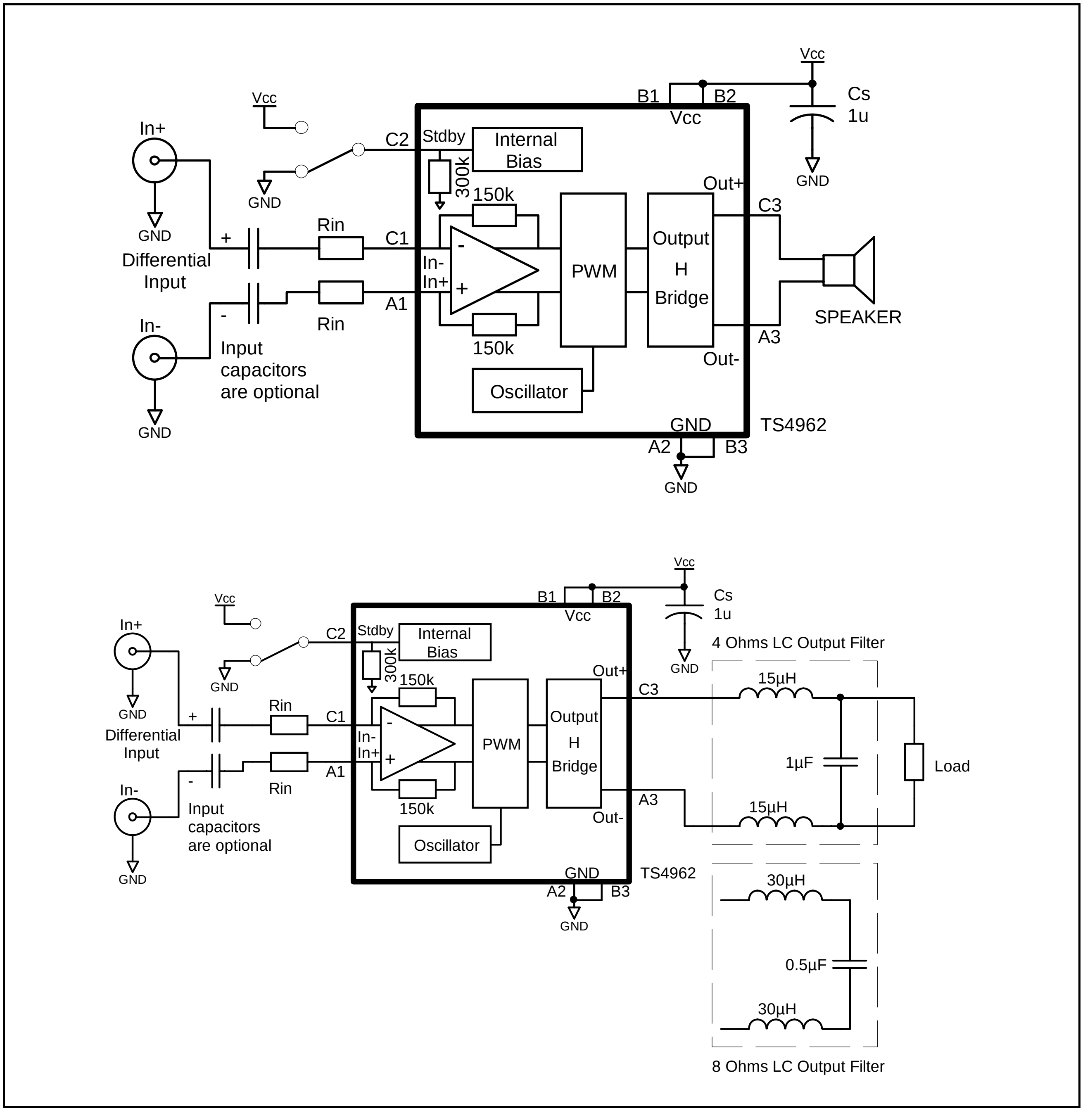
2) Minimum current consumption shall be obtained when V_{STB} = GND.

3) With heat sink surface = 125mm^2.

2 Application Components Information

Components	Functional Description
Cs	Bypass supply capacitor. To install as close as possible of the TS4962 to minimize high frequency ripple. A 100nF ceramic capacitor should be add to enhance the power supply filtering in high frequency.
Rin	Input resistor to program the TS4962 gain (Gain = 300/Rin with rin in kΩ)
Input Capacitor	Thanks to common mode feedback, these input capacitors are optional. However, we can add then to form with Rin a 1st oerder high pass filter with -3dB cut-off frequency = 1/(2*pi*Rin*Cin)

Figure 1: Typical application



3 Electrical Characteristics

Table 3: V_{CC} = +5V, GND = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		2.3		mA
$I_{STANDBY}$	Standby Current [1] No input signal, V_{STBY} = GND		10	1000	nA
Voo	Output Offset Voltage No input signal, R_L = 8Ω		3		mV
Po	Output Power, G=6dB THD = 2% Max, f = 1kHz, R_L = 4Ω THD = 1% Max, f = 1kHz, R_L = 8Ω		2 1.2		W
THD + N	Total Harmonic Distortion + Noise Po = 900 mW_{RMS}, G = 6dB, 20Hz < f < 20kHz, R_L = 8Ω + 15µH, BW < 30kHz		1		%
Efficiency	Efficiency Po = 2 W_{RMS}, R_L = 4Ω + ≥ 15µH Po =1.2 W_{RMS}, R_L = 8Ω+ ≥ 15µH		77 87		%
PSRR	Power Supply Rejection Ratio with inputs grounded [2] f = 217Hz, R_L = 8Ω, G=6dB, Vripple = $200mV_{pp}$		63		dB
CMRR	Common Mode Rejection Ratio, f = 217Hz, R_L = 8Ω, G = 6dB, ΔVic = $200mV_{pp}$		57		dB
Gain	Gain value (Rin in kΩ)	$\frac{240k\Omega}{Rin}$	$\frac{300k\Omega}{Rin}$	$\frac{360k\Omega}{Rin}$	dB
R_{STDBY}	Internal Resistance From Standby to GND	240	300	360	kΩ
F_{PWM}	Pulse Width Modulator Base Frequency		250		kHz
SNR	Signal to Noise ratio (A Weighting), Po = 1.2W, R_L = 8Ω		85		dB
T_{WU}	Wake-up time		5		ms
T_{STB}	Standby time		5		ms
V_N	Output Voltage Noise f = 20Hz to 20kHz, G = 6dB Unweighted R_L = 4Ω A weighted R_L = 4Ω Unweighted R_L = 8Ω A weighted R_L = 8Ω Unweighted R_L = 4Ω + 15µH A weighted R_L = 4Ω + 15µH Unweighted R_L = 4Ω + 30µH A weighted R_L = 4Ω + 30µH Unweighted R_L = 8Ω + 30µH A weighted R_L = 8Ω + 30µH Unweighted R_L = 4Ω + Filter A weighted R_L = 4Ω + Filter Unweighted R_L = 4Ω + Filter A weighted R_L = 4Ω + Filter		85 60 86 62 83 60 88 64 78 57 87 65 82 59 90 66		μV_{RMS}

1) Standby mode is actived when Vstdby is tied to GND.

2) Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is the surimposed sinus signal to Vcc @ f = 217Hz.

Table 4: V_{CC} = +4.2V, GND = 0V, T_{amb} = 25°C (unless otherwise specified) [1]

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		2.1		mA
$I_{STANDBY}$	Standby Current [2] No input signal, V_{STBY} = GND		10	1000	nA
Voo	Output Offset Voltage No input signal, R_L = 8Ω		3		mV
Po	Output Power, G=6dB THD = 2% Max, f = 1kHz, R_L = 4Ω THD = 1% Max, f = 1kHz, R_L = 8Ω		1.5 0.9		W
THD + N	Total Harmonic Distortion + Noise Po = 600 mW_{RMS}, G = 6dB, 20Hz < f < 20kHz, R_L = 8Ω + 15µH, BW < 30kHz		1		%
Efficiency	Efficiency Po = 1.5 W_{RMS}, R_L = 4Ω + ≥ 15µH Po = 0.9 W_{RMS}, R_L = 8Ω+ ≥ 15µH		78 87		%
PSRR	Power Supply Rejection Ratio with inputs grounded [3] f = 217Hz, R_L = 8Ω, G=6dB, Vripple = $200mV_{pp}$		63		dB
CMRR	Common Mode Rejection Ratio, f = 217Hz, R_L = 8Ω, G = 6dB, ΔVic = $200mV_{pp}$		57		dB
Gain	Gain value (Rin in kΩ)	$\frac{240k\Omega}{Rin}$	$\frac{300k\Omega}{Rin}$	$\frac{360k\Omega}{Rin}$	V/V
R_{STDBY}	Internal Resistance From Standby to GND	240	300	360	kΩ
F_{PWM}	Pulse Width Modulator Base Frequency		250		kHz
SNR	Signal to Noise ratio (A Weighting), Po = 0.9W, R_L = 8Ω		85		dB
T_{WU}	Wake-up time		5		ms
T_{STB}	Standby time		5		ms
V_N	Output Voltage Noise f = 20Hz to 20kHz, G = 6dB Unweighted R_L = 4Ω A weighted R_L = 4Ω Unweighted R_L = 8Ω A weighted R_L = 8Ω Unweighted R_L = 4Ω + 15µH A weighted R_L = 4Ω + 15µH Unweighted R_L = 4Ω + 30µH A weighted R_L = 4Ω + 30µH Unweighted R_L = 8Ω + 30µH A weighted R_L = 8Ω + 30µH Unweighted R_L = 4Ω + Filter A weighted R_L = 4Ω + Filter Unweighted R_L = 4Ω + Filter A weighted R_L = 4Ω + Filter		85 60 86 62 83 60 88 64 78 57 87 65 82 59 90 66		μV_{RMS}

1) All electrical values are guaranted with correlation measurements at 2.5V and 5V.

2) Standby mode is actived when Vstdby is tied to GND.

3) Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is the surimposed sinus signal to Vcc @ f = 217Hz.

Table 5: V_{CC} = +3.6V, GND = 0V, T_{amb} = 25°C (unless otherwise specified) [1]

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		2		mA
$I_{STANDBY}$	Standby Current [2] No input signal, V_{STBY} = GND		10	1000	nA
Voo	Output Offset Voltage No input signal, R_L = 8Ω		3		mV
Po	Output Power, G=6dB THD = 2% Max, f = 1kHz, R_L = 4Ω THD = 1% Max, f = 1kHz, R_L = 8Ω		1 0.6		W
THD + N	Total Harmonic Distortion + Noise Po = 500 mW_{RMS}, G = 6dB, 20Hz < f < 20kHz, R_L = 8Ω + 15µH, BW < 30kHz		1		%
Efficiency	Efficiency Po = 1 W_{RMS}, R_L = 4Ω + ≥ 15µH Po = 0.6 W_{RMS}, R_L = 8Ω+ ≥ 15µH		78 87		%
PSRR	Power Supply Rejection Ratio with inputs grounded [3] f = 217Hz, R_L = 8Ω, G=6dB, Vripple = $200mV_{pp}$		62		dB
CMRR	Common Mode Rejection Ratio, f = 217Hz, R_L = 8Ω, G = 6dB, ΔVic = $200mV_{pp}$		56		dB
Gain	Gain value (Rin in kΩ)	$\frac{240k\Omega}{Rin}$	$\frac{300k\Omega}{Rin}$	$\frac{360k\Omega}{Rin}$	V/V
R_{STDBY}	Internal Resistance From Standby to GND	240	300	360	kΩ
F_{PWM}	Pulse Width Modulator Base Frequency		250		kHz
SNR	Signal to Noise ratio (A Weighting), Po = 0.6W, R_L = 8Ω		83		dB
T_{WU}	Wake-up time		5		ms
T_{STB}	Standby time		5		ms
V_N	Output Voltage Noise f = 20Hz to 20kHz, G = 6dB Unweighted R_L = 4Ω A weighted R_L = 4Ω Unweighted R_L = 8Ω A weighted R_L = 8Ω Unweighted R_L = 4Ω + 15µH A weighted R_L = 4Ω + 15µH Unweighted R_L = 4Ω + 30µH A weighted R_L = 4Ω + 30µH Unweighted R_L = 8Ω + 30µH A weighted R_L = 8Ω + 30µH Unweighted R_L = 4Ω + Filter A weighted R_L = 4Ω + Filter Unweighted R_L = 4Ω + Filter A weighted R_L = 4Ω + Filter		83 57 83 61 81 58 87 62 77 56 85 63 80 57 85 61		μV_{RMS}

1) All electrical values are guaranted with correlation measurements at 2.5V and 5V.

2) Standby mode is actived when Vstdby is tied to GND.

3) Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is the surimposed sinus signal to Vcc @ f = 217Hz.

Table 6: V_{CC} = +3.0V, GND = 0V, T_{amb} = 25°C (unless otherwise specified) [1]

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		1.9		mA
$I_{STANDBY}$	Standby Current [2] No input signal, V_{STBY} = GND		10	1000	nA
Voo	Output Offset Voltage No input signal, R_L = 8Ω		3		mV
Po	Output Power, G=6dB THD = 2% Max, f = 1kHz, R_L = 4Ω THD = 1% Max, f = 1kHz, R_L = 8Ω		0.7 0.4		W
THD + N	Total Harmonic Distortion + Noise Po = 500 mW_{RMS}, G = 6dB, 20Hz < f < 20kHz, R_L = 8Ω + 15µH, BW < 30kHz		1		%
Efficiency	Efficiency Po = 0.7 W_{RMS}, R_L = 4Ω + ≥ 15µH Po = 0.4 W_{RMS}, R_L = 8Ω+ ≥ 15µH		78 87		%
PSRR	Power Supply Rejection Ratio with inputs grounded [3] f = 217Hz, R_L = 8Ω, G=6dB, Vripple = $200mV_{pp}$		60		dB
CMRR	Common Mode Rejection Ratio, f = 217Hz, R_L = 8Ω, G = 6dB, ΔVic = $200mV_{pp}$		54		dB
Gain	Gain value (Rin in kΩ)	$\frac{240k\Omega}{Rin}$	$\frac{300k\Omega}{Rin}$	$\frac{360k\Omega}{Rin}$	V/V
R_{STDBY}	Internal Resistance From Standby to GND	240	300	360	kΩ
F_{PWM}	Pulse Width Modulator Base Frequency		250		kHz
SNR	Signal to Noise ratio (A Weighting), Po = 0.4W, R_L = 8Ω		82		dB
T_{WU}	Wake-up time		5		ms
T_{STB}	Standby time		5		ms
V_N	Output Voltage Noise f = 20Hz to 20kHz, G = 6dB Unweighted R_L = 4Ω A weighted R_L = 4Ω Unweighted R_L = 8Ω A weighted R_L = 8Ω Unweighted R_L = 4Ω + 15µH A weighted R_L = 4Ω + 15µH Unweighted R_L = 4Ω + 30µH A weighted R_L = 4Ω + 30µH Unweighted R_L = 8Ω + 30µH A weighted R_L = 8Ω + 30µH Unweighted R_L = 4Ω + Filter A weighted R_L = 4Ω + Filter Unweighted R_L = 4Ω + Filter A weighted R_L = 4Ω + Filter		83 57 83 61 81 58 87 62 77 56 85 63 80 57 85 61		μV_{RMS}

1) All electrical values are guaranted with correlation measurements at 2.5V and 5V.

2) Standby mode is actived when Vstdby is tied to GND.

3) Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is the surimposed sinus signal to Vcc @ f = 217Hz.

Table 7: V_{CC} = +2.5V, GND = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current No input signal, no load		1.7		mA
$I_{STANDBY}$	Standby Current [1] No input signal, V_{STBY} = GND		10	1000	nA
Voo	Output Offset Voltage No input signal, $R_L = 8\Omega$		3		mV
Po	Output Power, G=6dB THD = 2% Max, f = 1kHz, $R_L = 4\Omega$ THD = 1% Max, f = 1kHz, $R_L = 8\Omega$		0.45 0.3		W
THD + N	Total Harmonic Distortion + Noise Po = 200 mW_{RMS}, G = 6dB, 20Hz < f < 20kHz, $R_L = 8\Omega$ + 15µH, BW < 30kHz		1		%
Efficiency	Efficiency Po = 0.45 W_{RMS}, $R_L = 4\Omega + \geq 15\mu H$ Po = 0.3 W_{RMS}, $R_L = 8\Omega + \geq 15\mu H$		78 87		%
PSRR	Power Supply Rejection Ratio with inputs grounded [2] f = 217Hz, $R_L = 8\Omega$, G=6dB, Vripple = $200mV_{pp}$		60		dB
CMRR	Common Mode Rejection Ratio, f = 217Hz, $R_L = 8\Omega$, G = 6dB, ΔVic = $200mV_{pp}$		54		dB
Gain	Gain value (Rin in kΩ)	$\frac{240k\Omega}{Rin}$	$\frac{300k\Omega}{Rin}$	$\frac{360k\Omega}{Rin}$	V/V
R_{STDBY}	Internal Resistance From Standby to GND	240	300	360	kΩ
F_{PWM}	Pulse Width Modulator Base Frequency		250		kHz
SNR	Signal to Noise ratio (A Weighting), Po = 0.4W, $R_L = 8\Omega$		80		dB
T_{WU}	Wake-up time		5		ms
T_{STB}	Standby time		5		ms
V_N	Output Voltage Noise f = 20Hz to 20kHz, G = 6dB Unweighted $R_L = 4\Omega$ A weighted $R_L = 4\Omega$ Unweighted $R_L = 8\Omega$ A weighted $R_L = 8\Omega$ Unweighted $R_L = 4\Omega$ + 15µH A weighted $R_L = 4\Omega$ + 15µH Unweighted $R_L = 4\Omega$ + 30µH A weighted $R_L = 4\Omega$ + 30µH Unweighted $R_L = 8\Omega$ + 30µH A weighted $R_L = 8\Omega$ + 30µH Unweighted $R_L = 4\Omega$ + Filter A weighted $R_L = 4\Omega$ + Filter Unweighted $R_L = 4\Omega$ + Filter A weighted $R_L = 4\Omega$ + Filter		85 60 86 62 76 56 82 60 67 53 78 57 74 54 78 59		μV_{RMS}

1) Standby mode is actived when Vstdby is tied to GND.

2) Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is the surimposed sinus signal to Vcc @ f = 217Hz.

Tip: *In the graphs that follow, the abbreviations are used:*
RL + nothing = pure resistive load
Filter = LC output filter (1µF+30µH for 4Ω and 0.5µF+60µH for 8Ω)

Figure 2: Test diagram for measurements

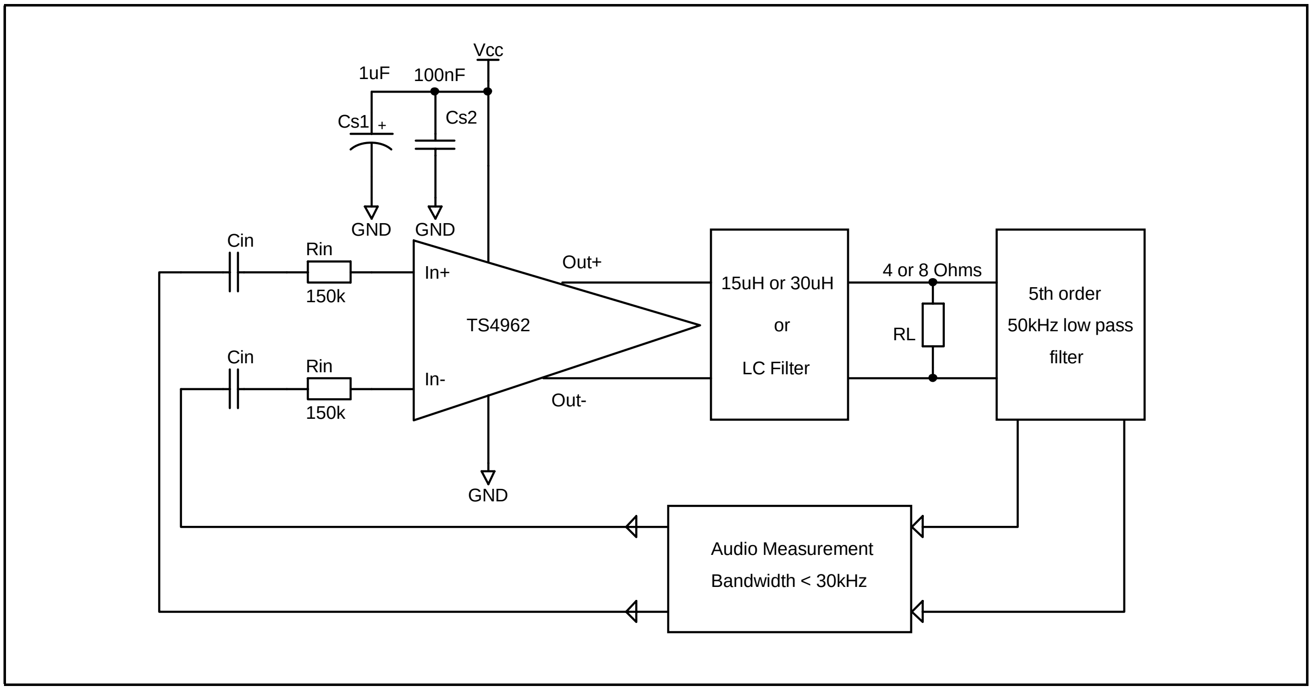


Figure 3: Current consumption vs power supply voltage

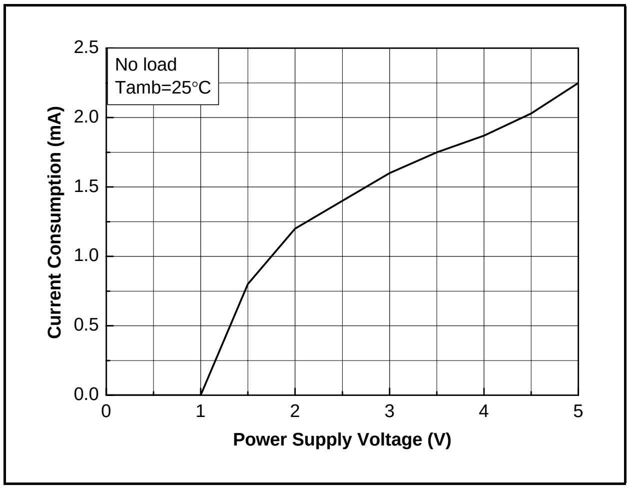


Figure 6: Output offset voltage vs common mode input voltage

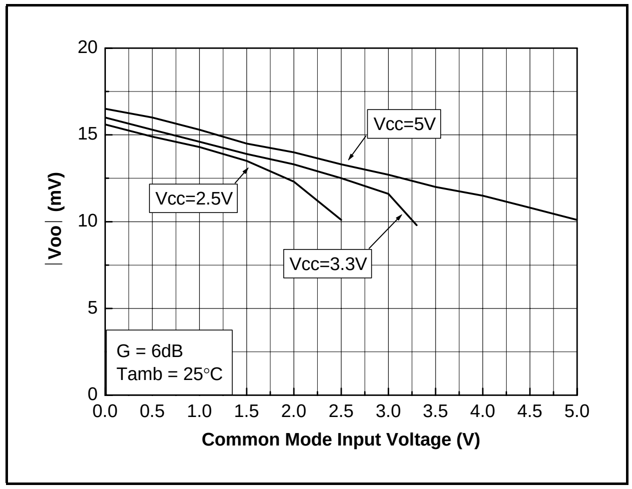


Figure 4: Current consumption vs standby voltage

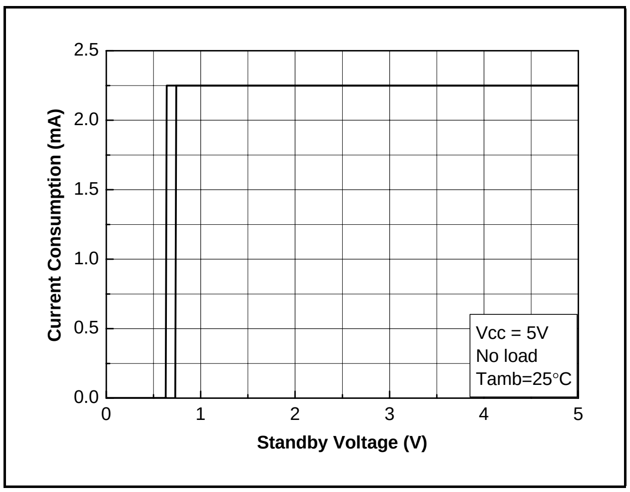


Figure 7: Efficiency vs output power

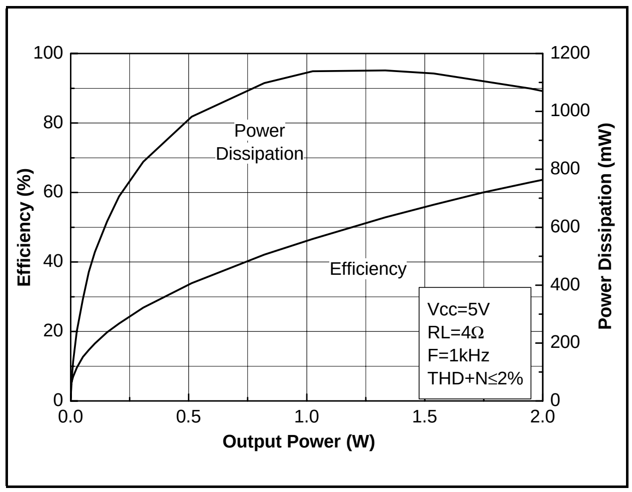


Figure 5: Current consumption vs standby voltage

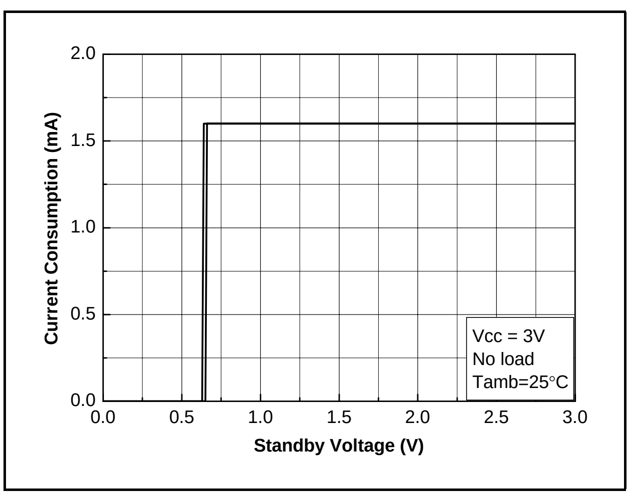


Figure 8: Efficiency vs output power

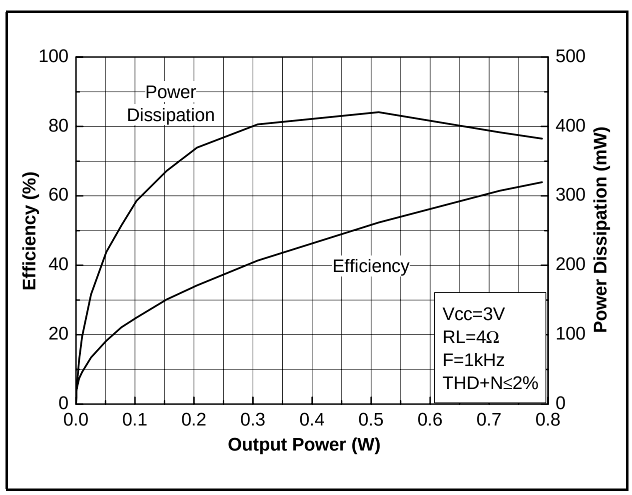


Figure 9: Efficiency vs output power

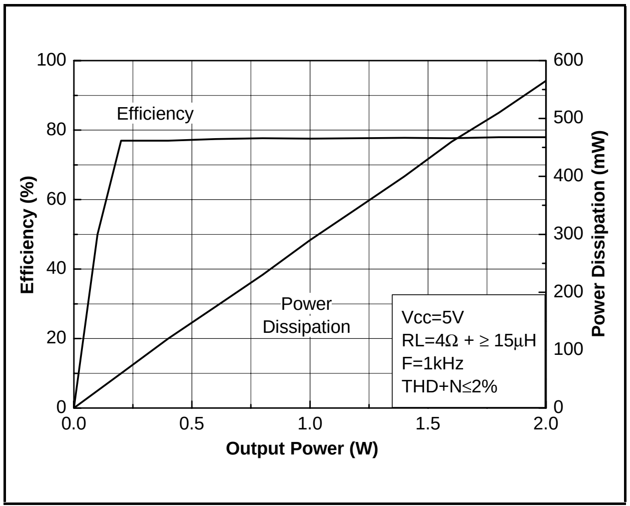


Figure 10: Efficiency vs output power

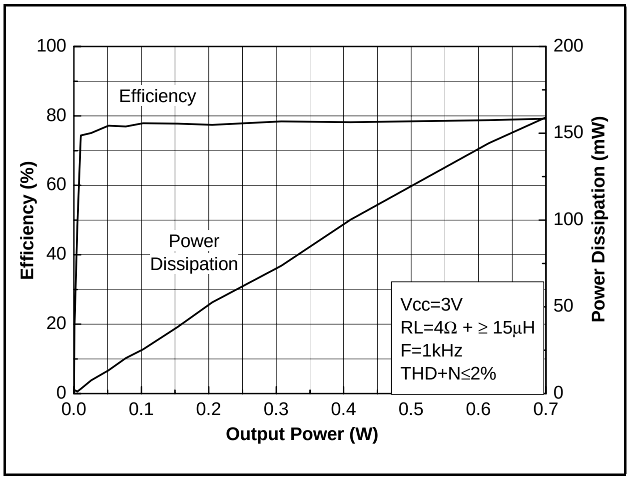


Figure 11: Efficiency vs output power

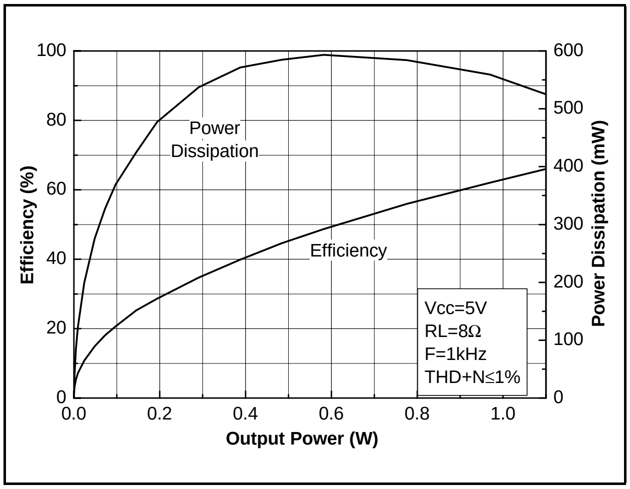


Figure 12: Efficiency vs output power

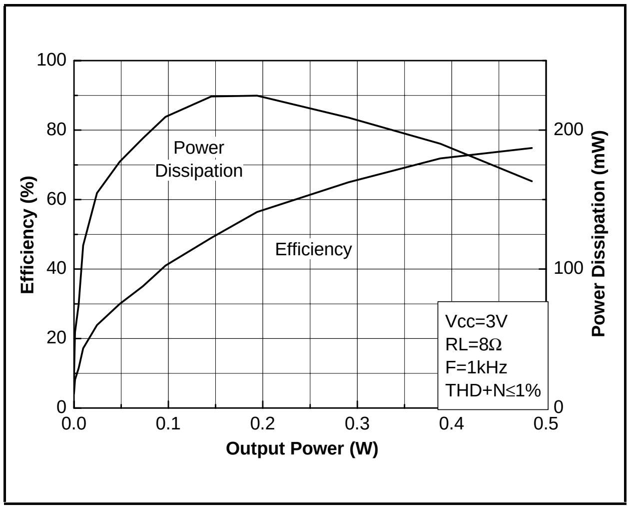


Figure 13: Efficiency vs output power

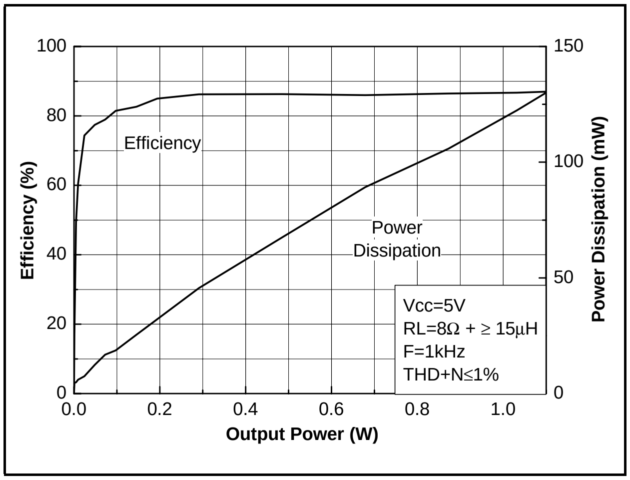


Figure 14: Efficiency vs output power

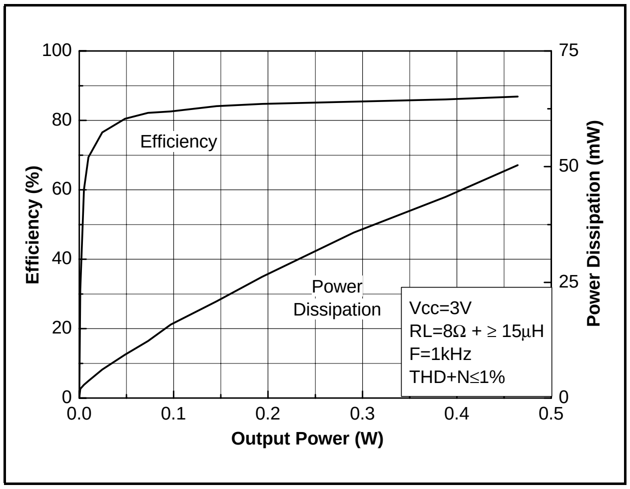


Figure 15: Output power vs power supply voltage

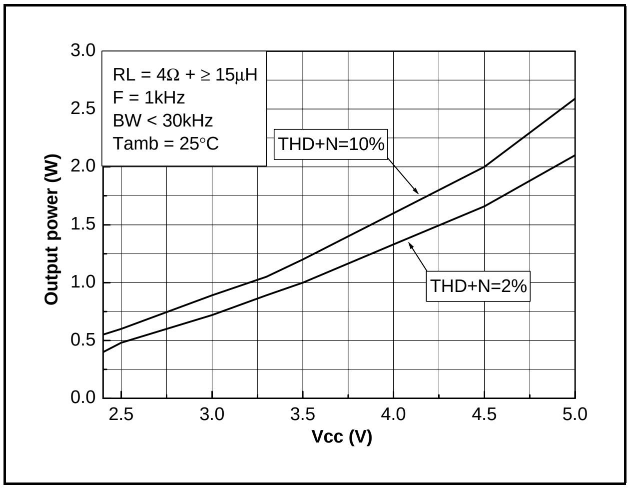


Figure 18: PSRR vs frequency

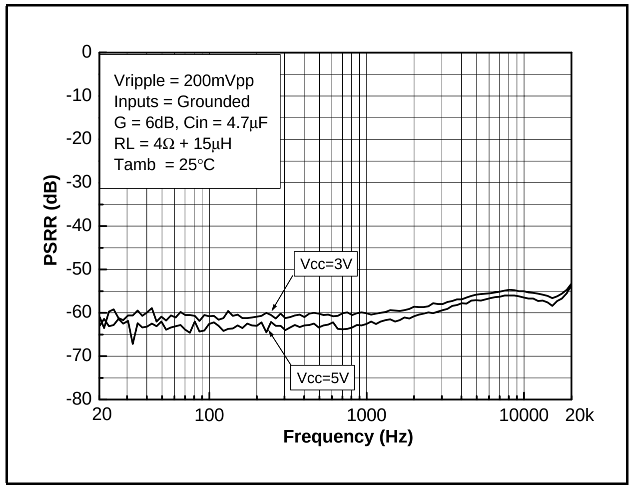


Figure 16: Output power vs power supply voltage

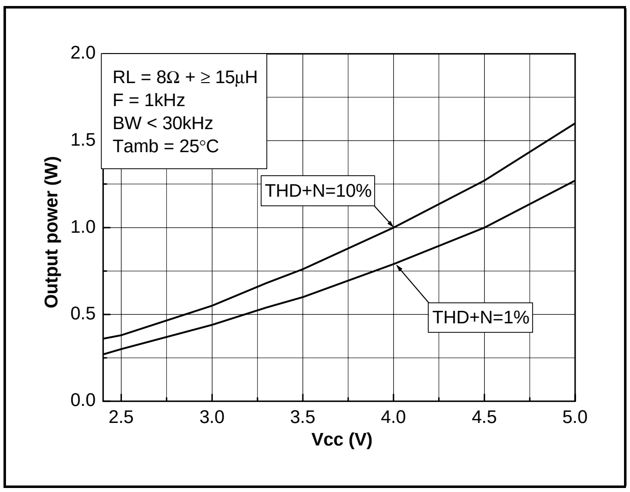


Figure 19: PSRR vs frequency

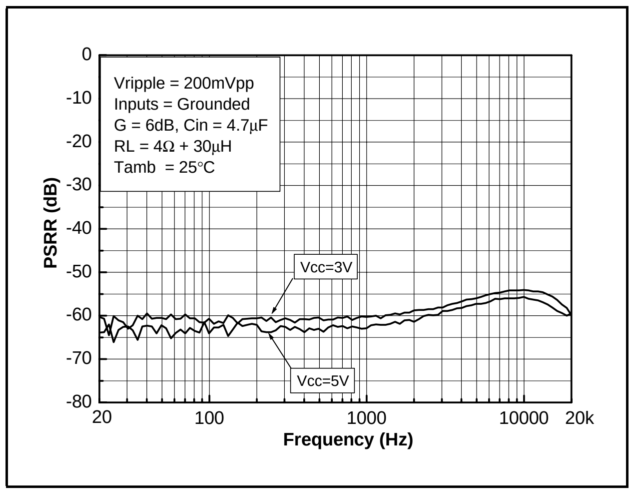


Figure 17: PSRR vs frequency

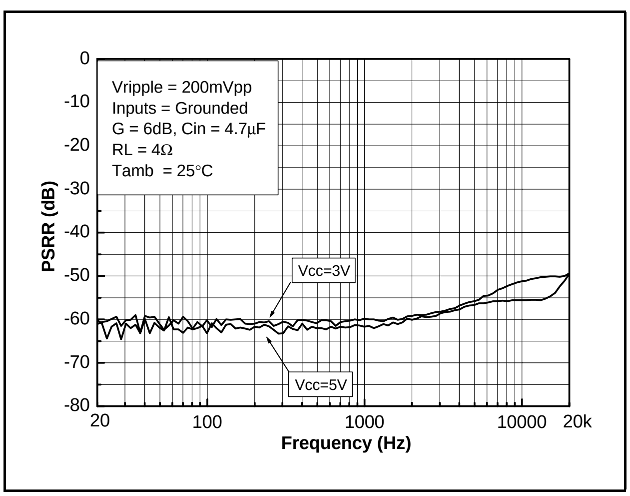


Figure 20: PSRR vs frequency

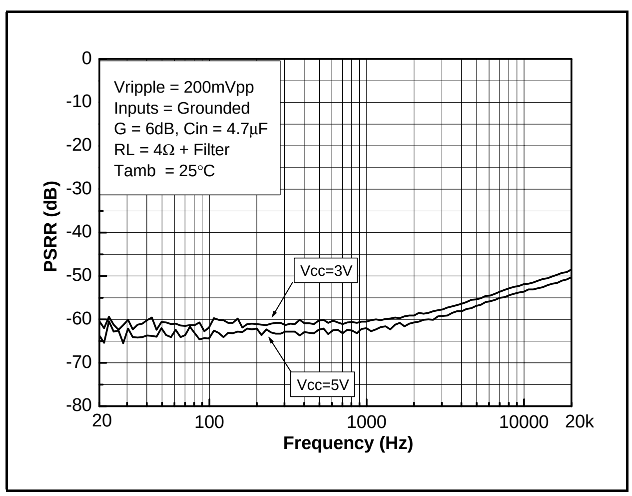


Figure 21: Output power vs power supply voltage

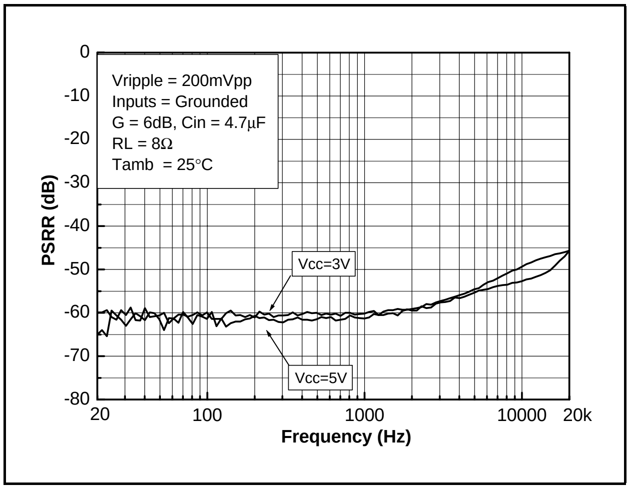


Figure 22: Output power vs power supply voltage

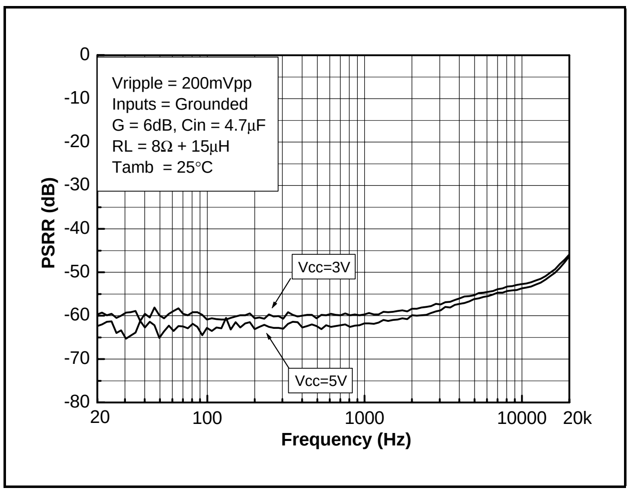


Figure 23: PSRR vs frequency

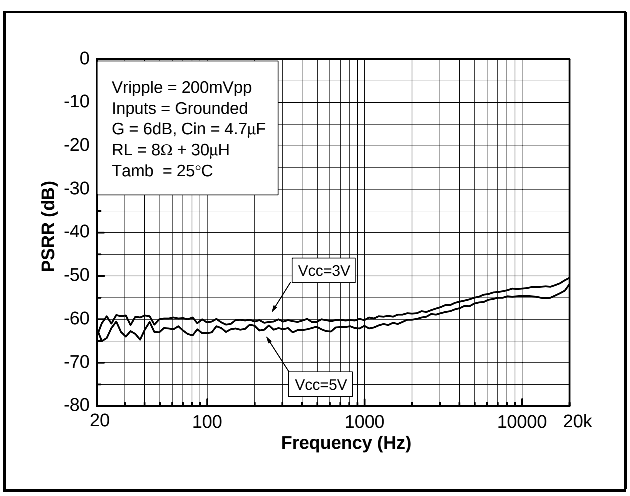


Figure 24: PSRR vs frequency

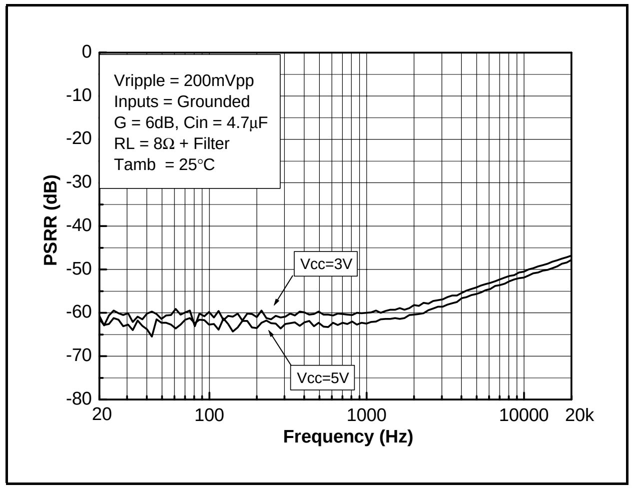


Figure 25: PSRR vs frequency Common Mode Input Voltage

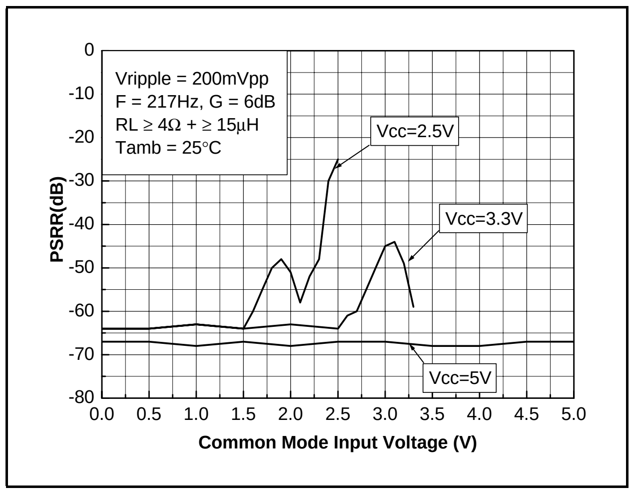


Figure 26: CMRR vs frequency

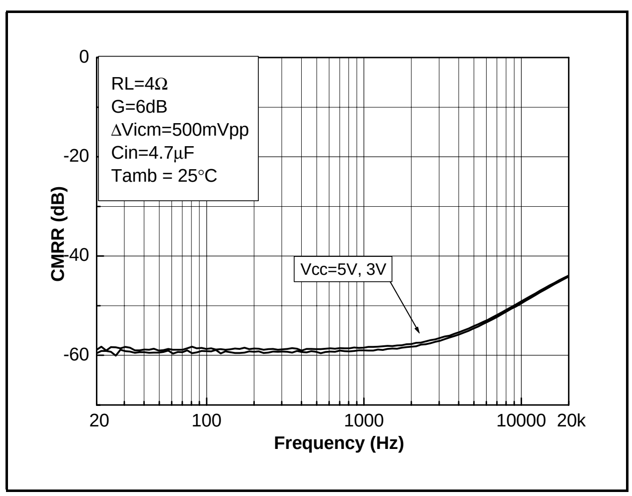


Figure 27: CMRR vs frequency

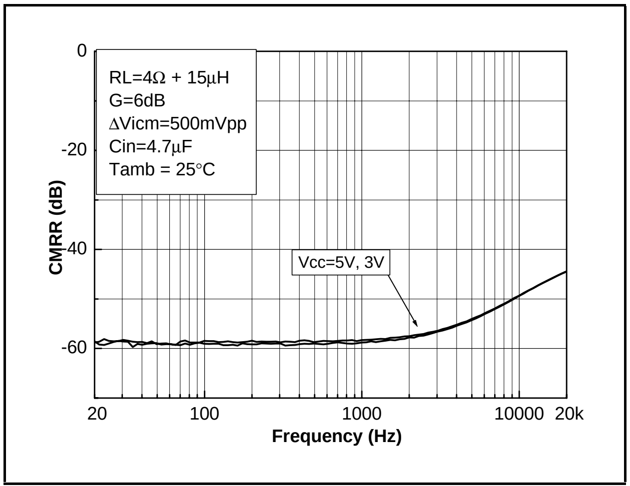


Figure 28: CMRR vs frequency

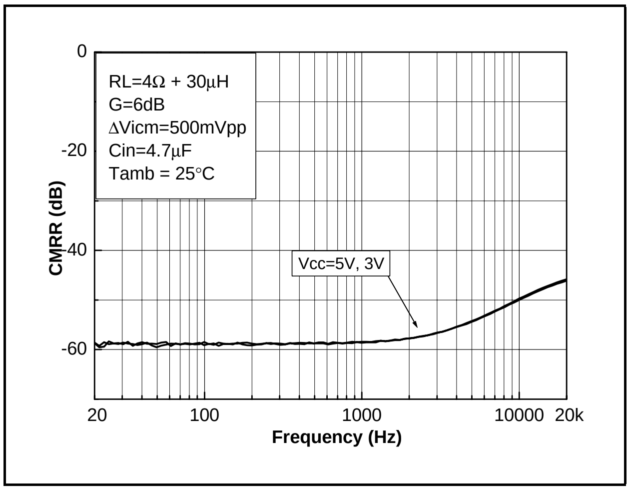


Figure 29: CMRR vs frequency

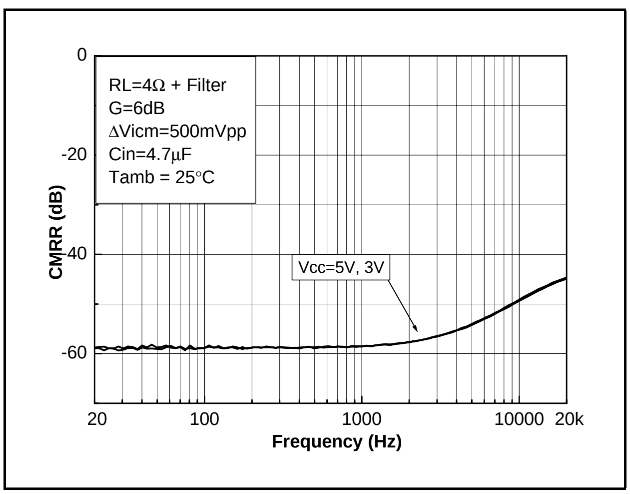


Figure 30: CMRR vs frequency

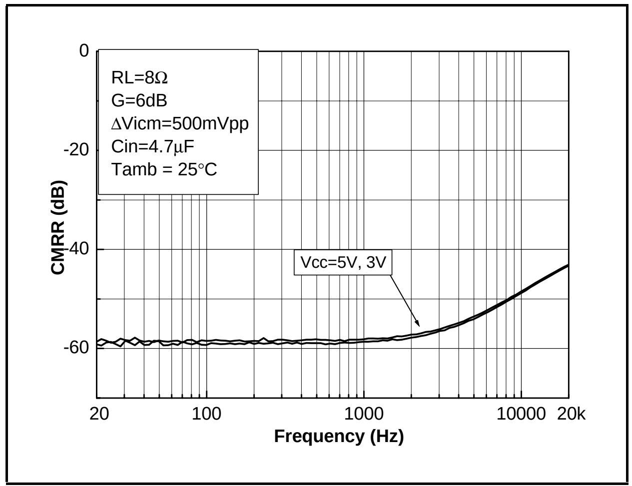


Figure 31: CMRR vs frequency

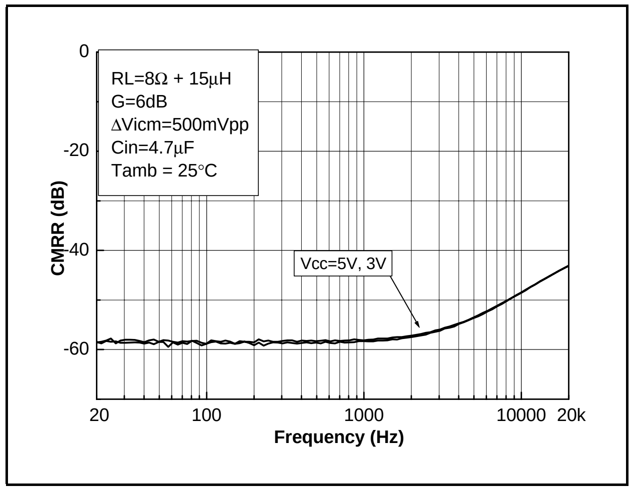


Figure 32: CMRR vs frequency

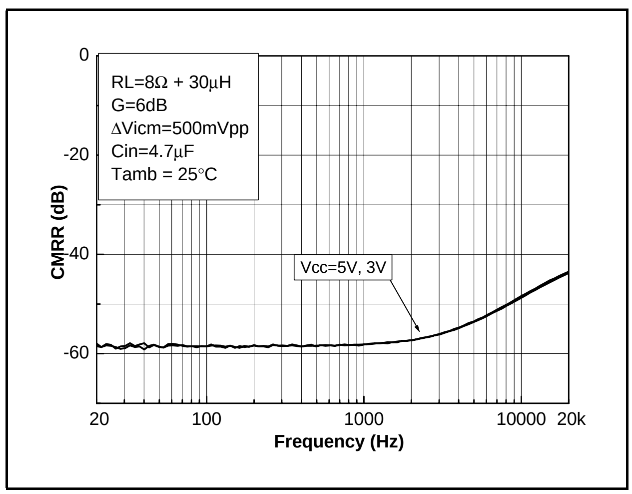


Figure 33: CMRR vs frequency

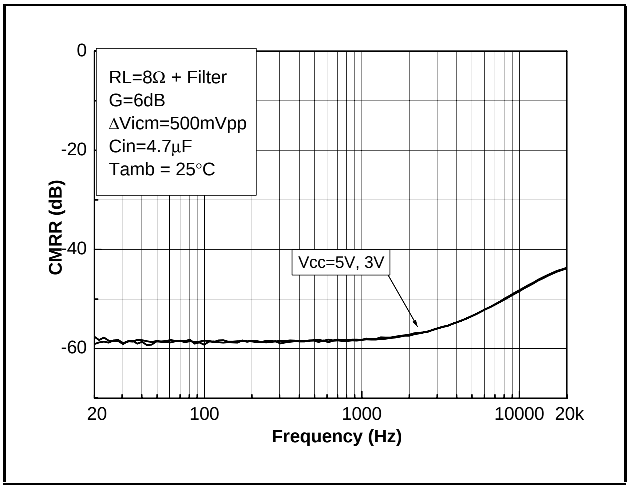


Figure 34: PSRR vs frequency common mode input voltage

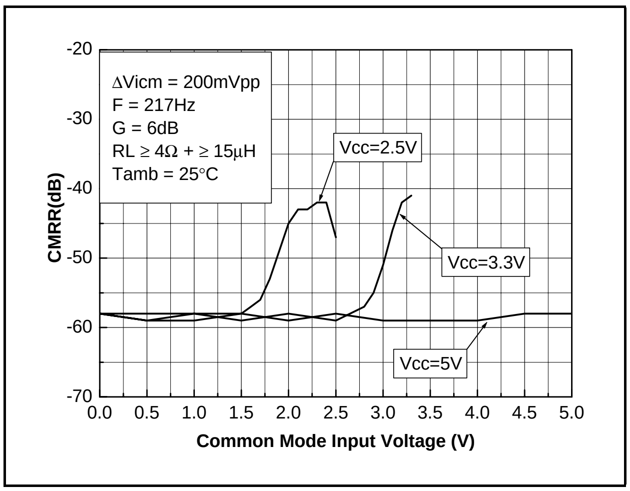


Figure 35: THD+N vs output power

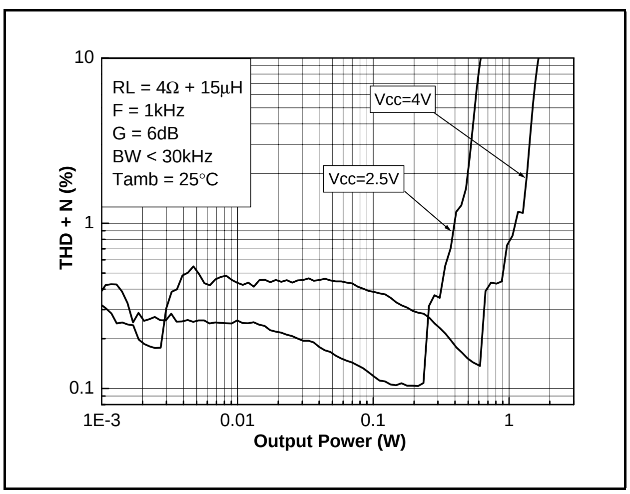


Figure 36: THD+N vs output power

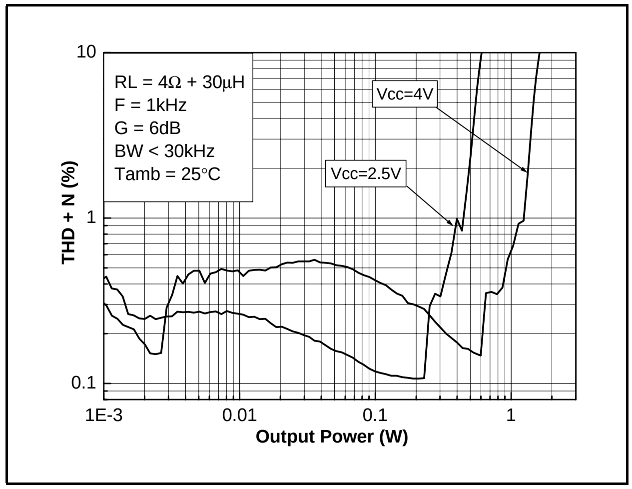


Figure 37: THD+N vs output power

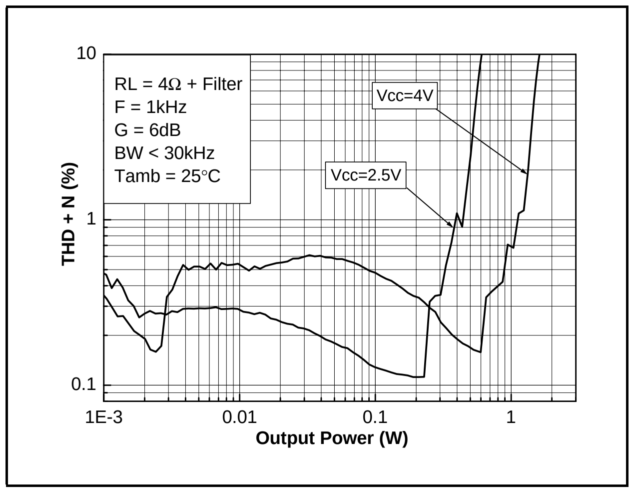


Figure 38: THD+N vs output power

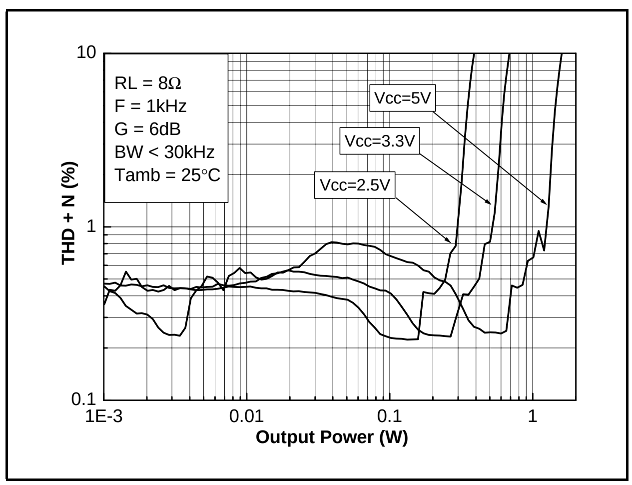


Figure 39: THD+N vs output power

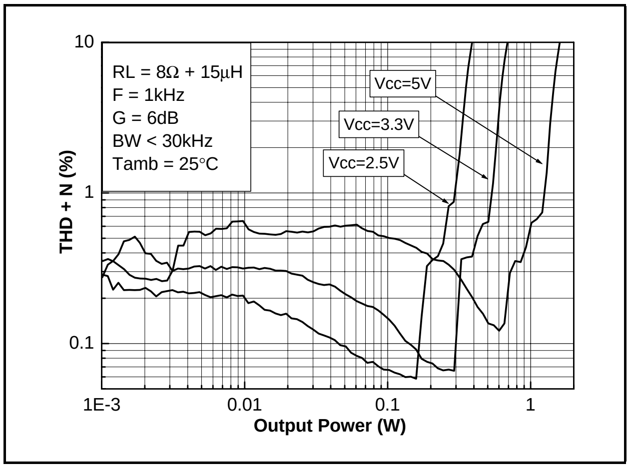


Figure 40: THD+N vs output power

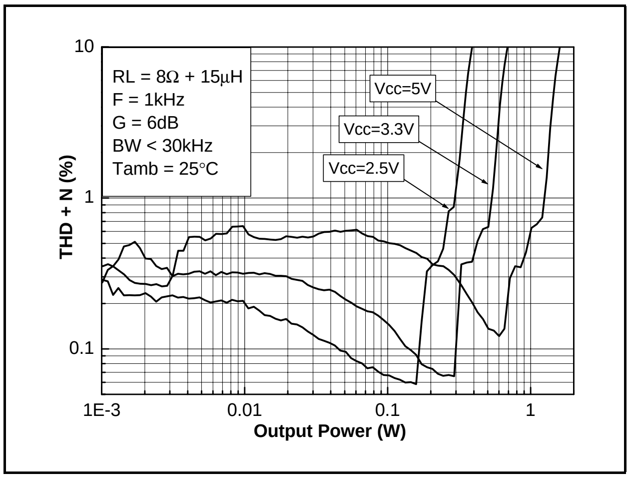


Figure 41: THD+N vs output power

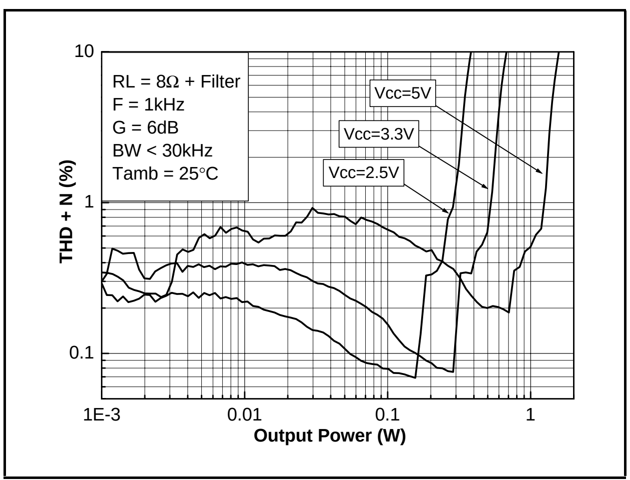


Figure 42: THD+N vs frequency

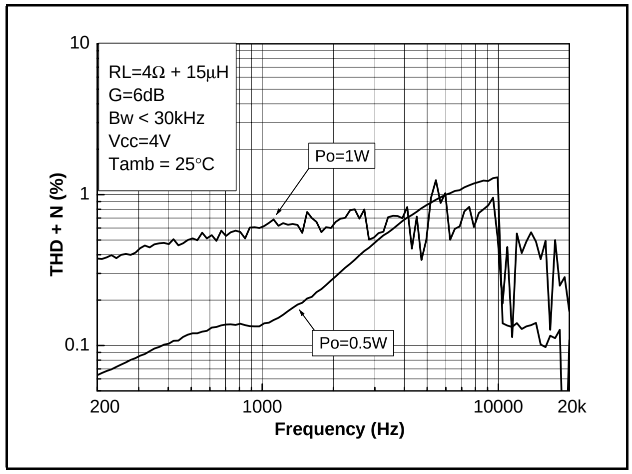


Figure 43: THD+N vs frequency

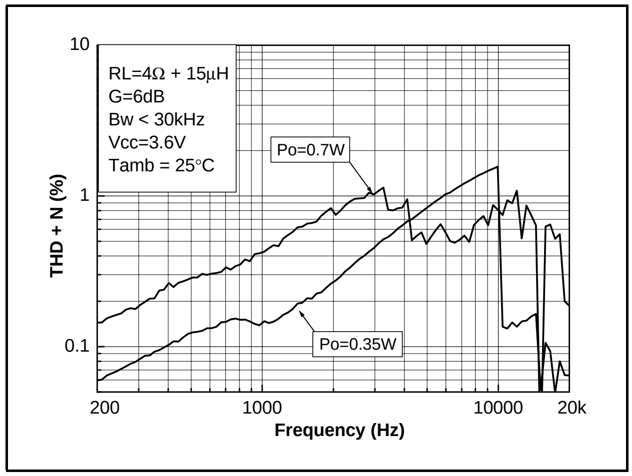


Figure 44: THD+N vs frequency

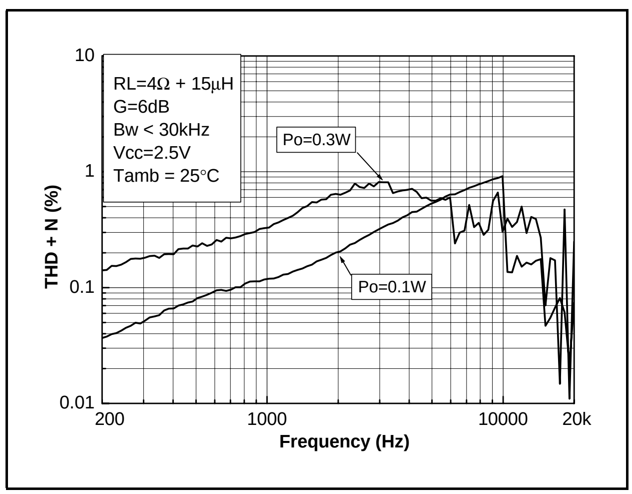


Figure 45: THD+N vs frequency

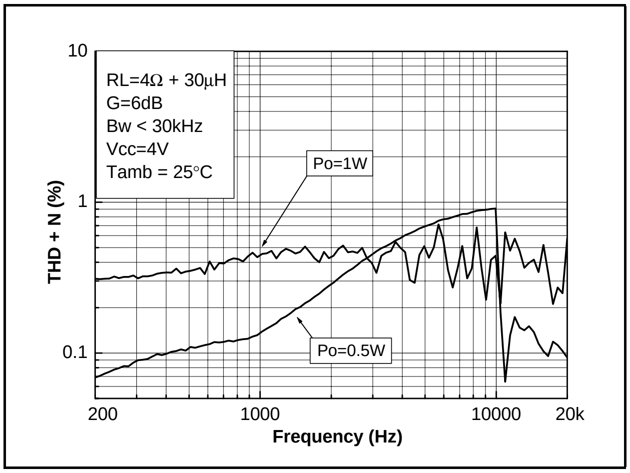


Figure 46: THD+N vs frequency

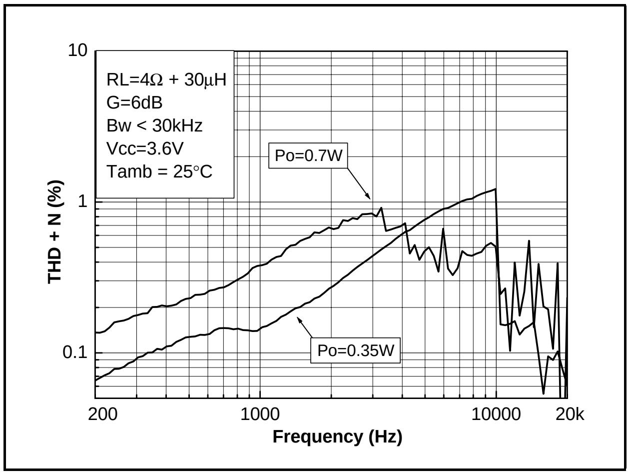


Figure 47: THD+N vs frequency

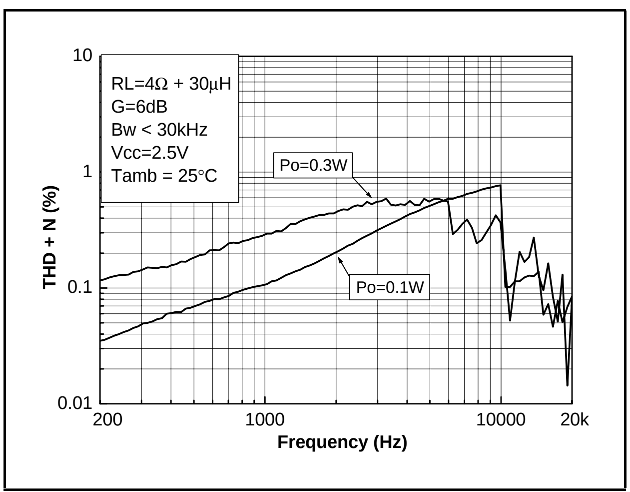


Figure 48: THD+N vs frequency

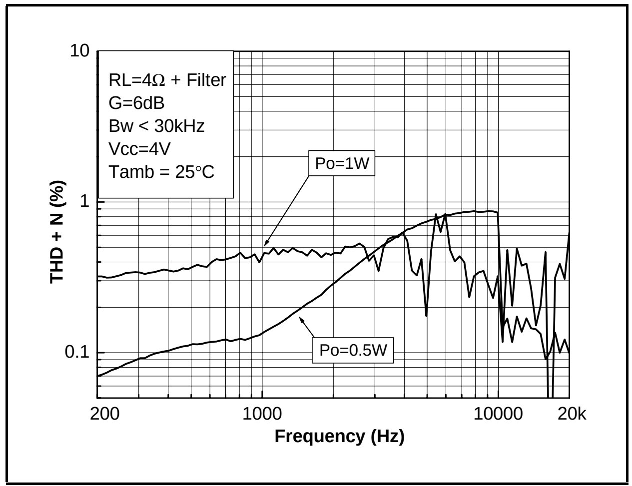


Figure 49: THD+N vs frequency

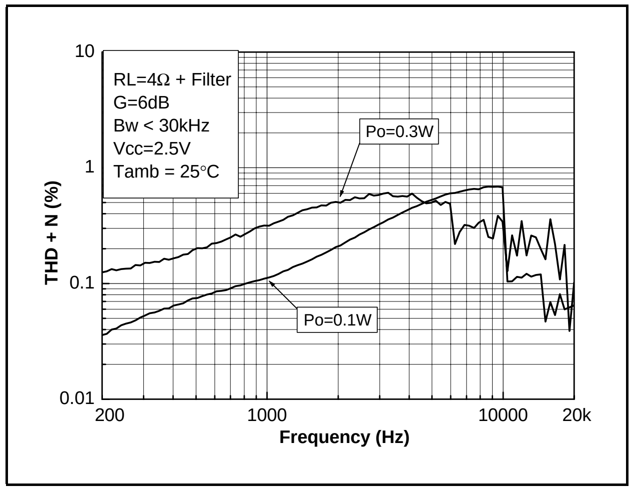


Figure 50: THD+N vs frequency

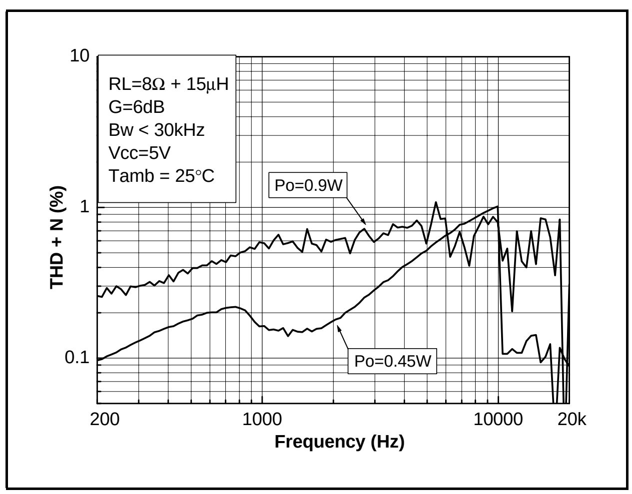


Figure 51: THD+N vs frequency

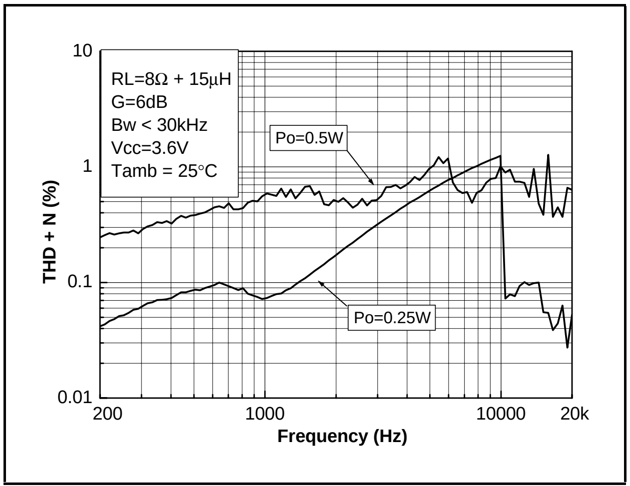


Figure 52: THD+N vs frequency

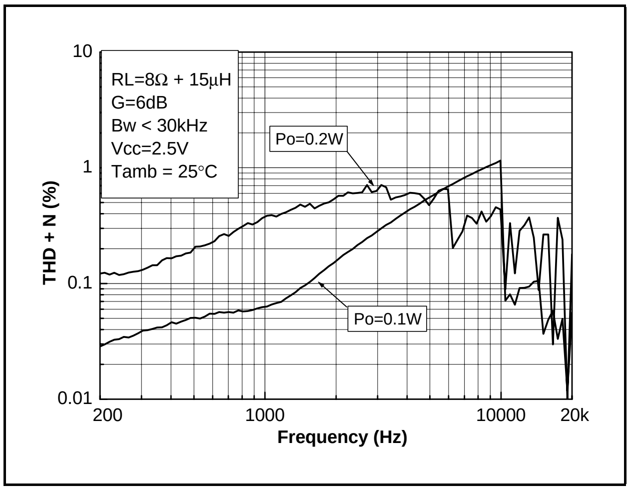


Figure 53: THD+N vs frequency

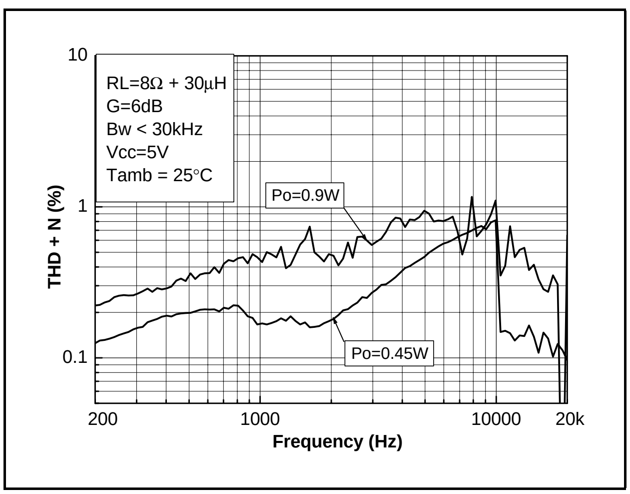


Figure 54: THD+N vs frequency

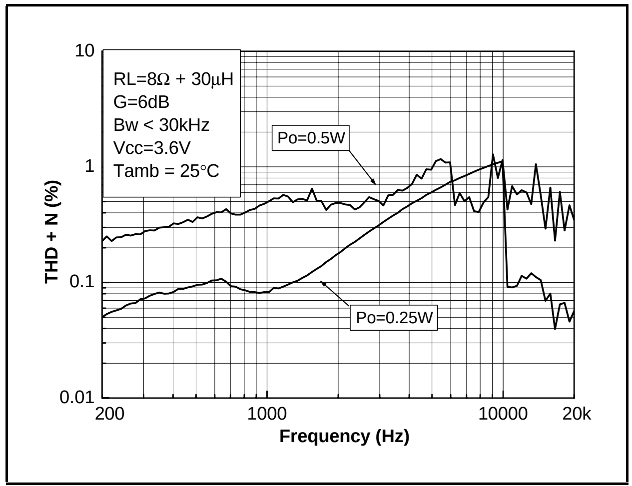


Figure 55: THD+N vs frequency

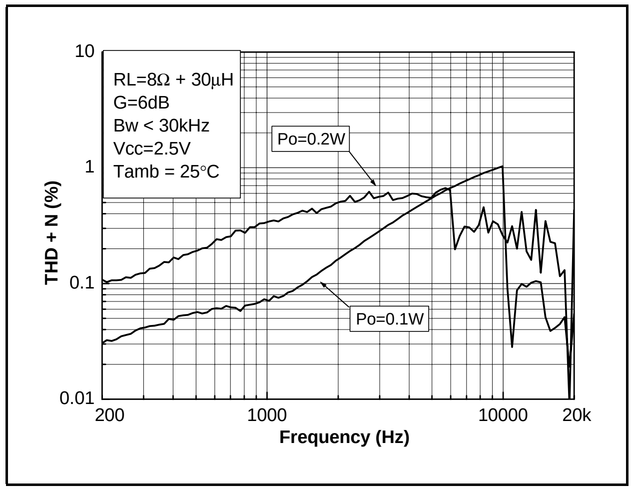


Figure 56: THD+N vs frequency

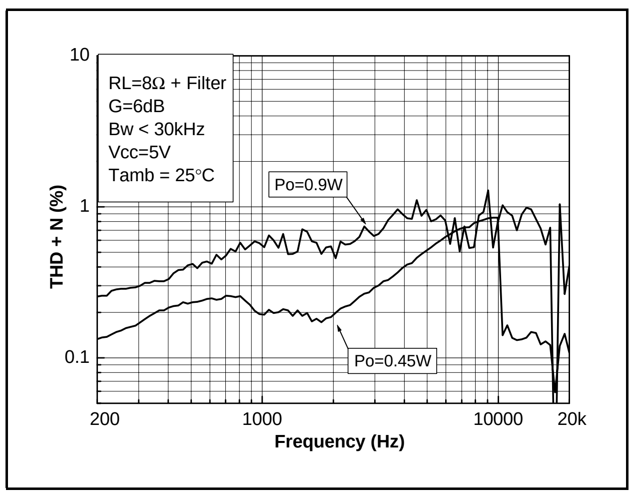


Figure 57: THD+N vs frequency

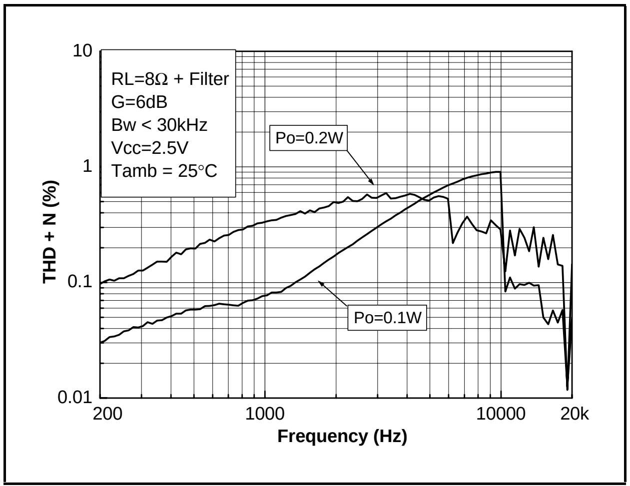


Figure 58: Gain vs frequency

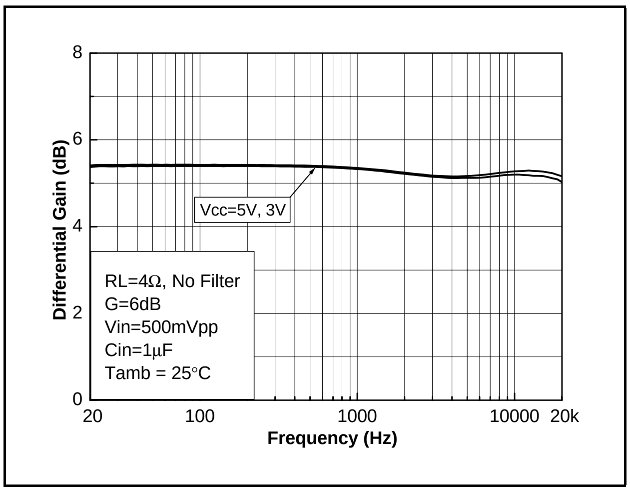


Figure 59: Gain vs frequency

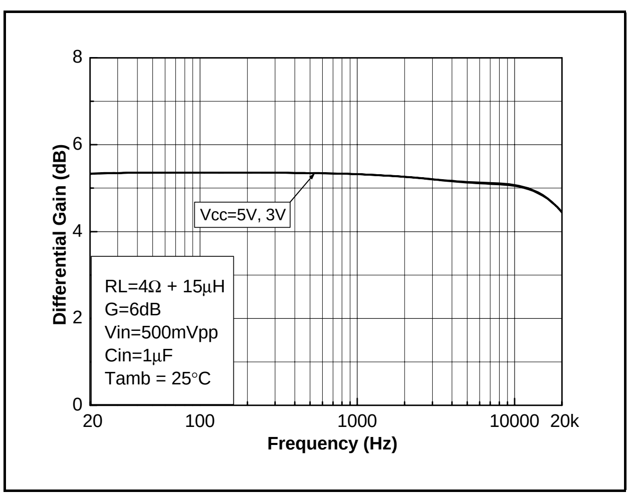


Figure 60: Gain vs frequency

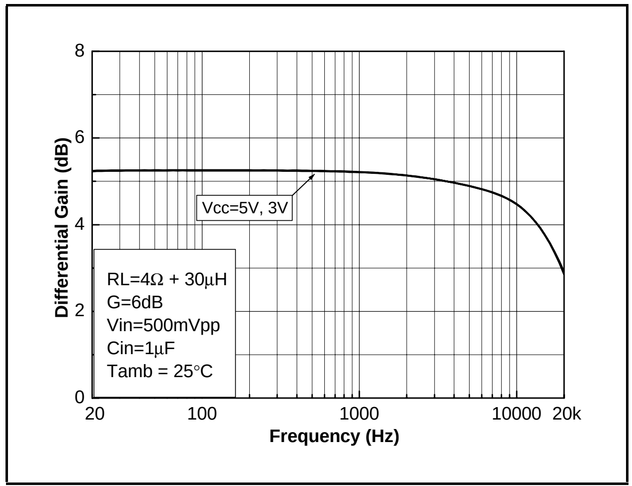


Figure 61: Gain vs frequency

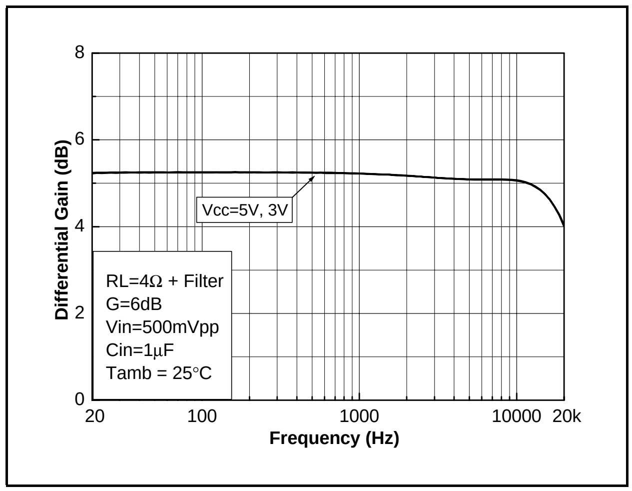


Figure 62: Gain vs frequency

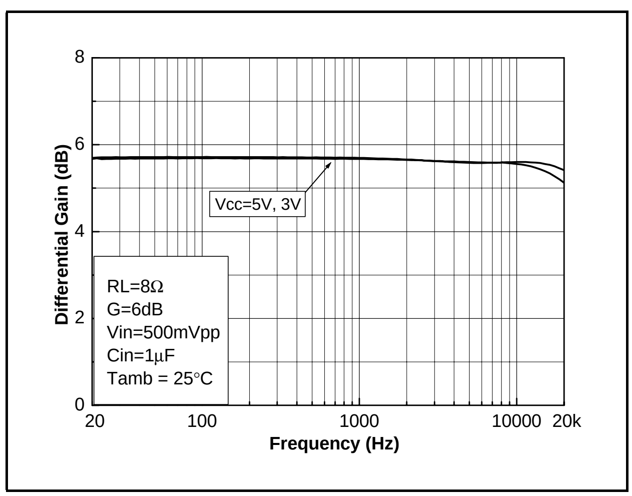


Figure 63: Gain vs frequency

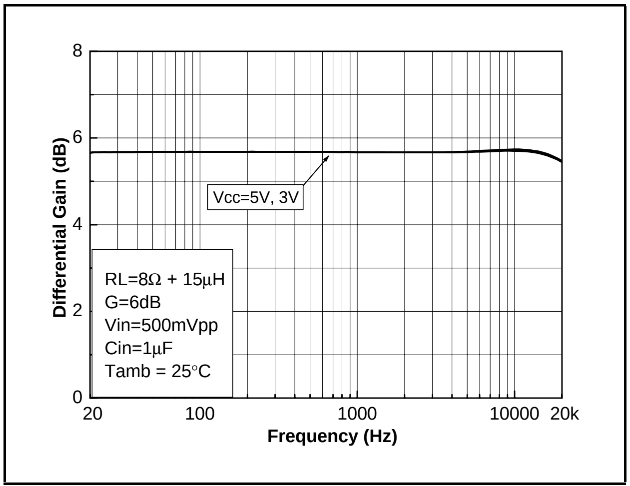


Figure 64: Gain vs frequency

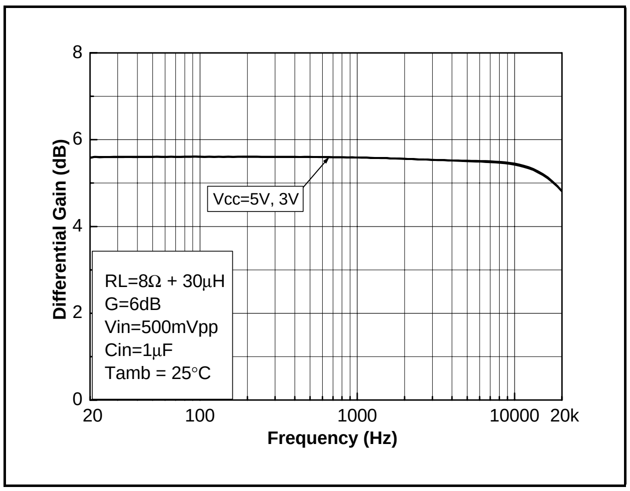


Figure 65: Gain vs frequency

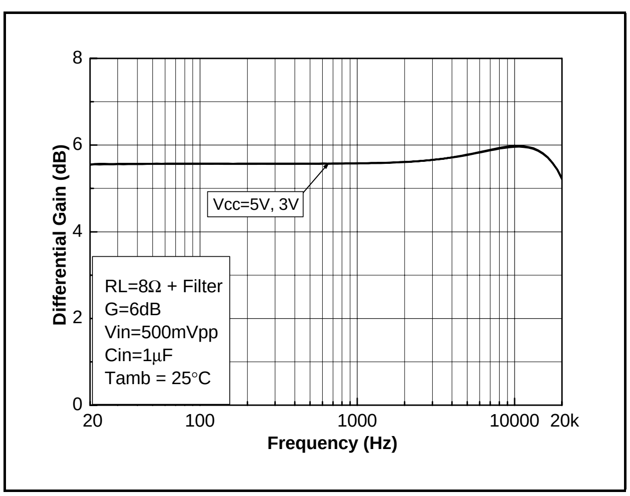


Figure 66: Gain vs frequency

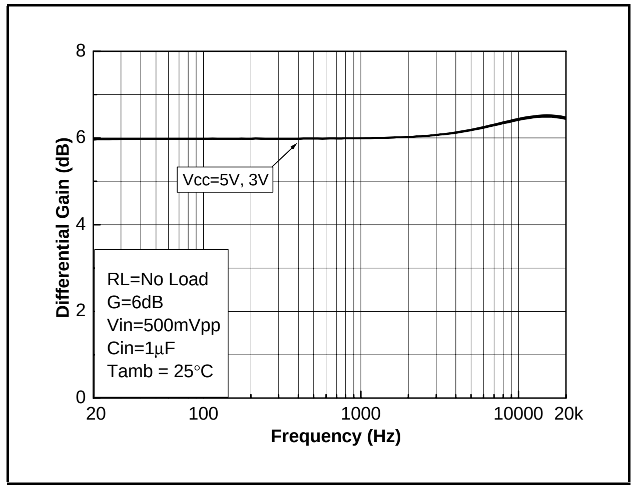


Figure 67: Startup & shutdown time Vcc=5V, G=6dB, C_{IN}=1µF (5ms/div)

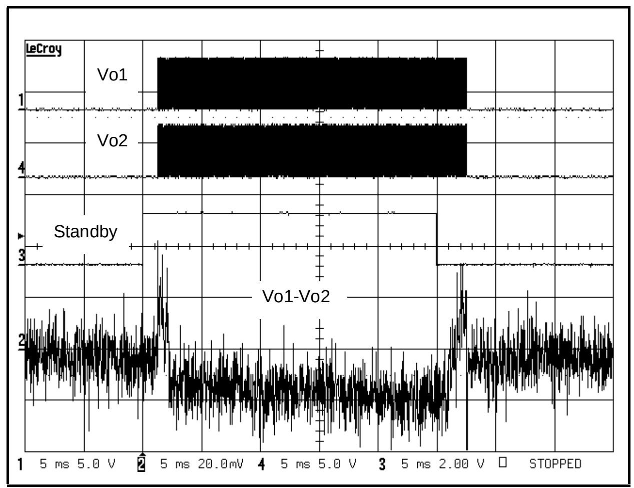


Figure 68: Startup & shutdown time Vcc=3V, G=6dB, C_{IN}=1µF (5ms/div)

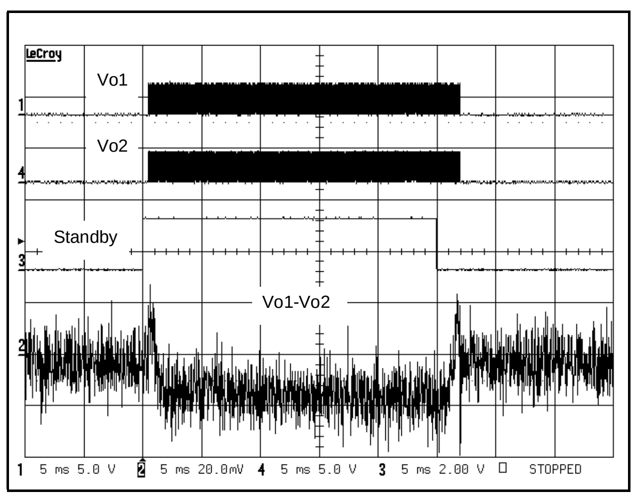


Figure 69: Startup & shutdown time
Vcc=5V, G=6dB, C_{IN}=100nF (5ms/div)

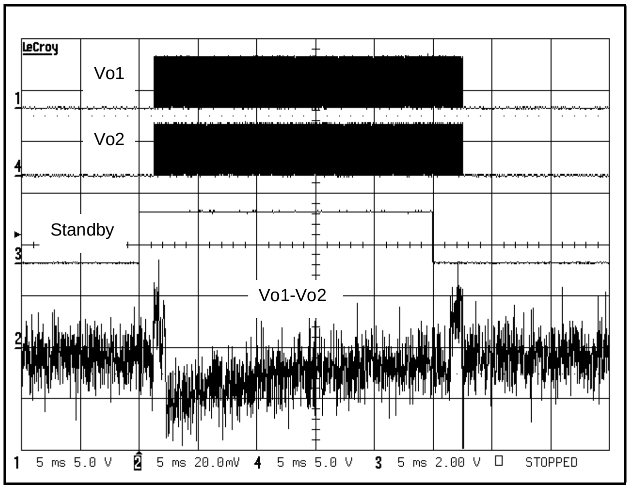


Figure 70: Startup & shutdown time
Vcc=3V, G=6dB, C_{IN}=100nF (5ms/div)

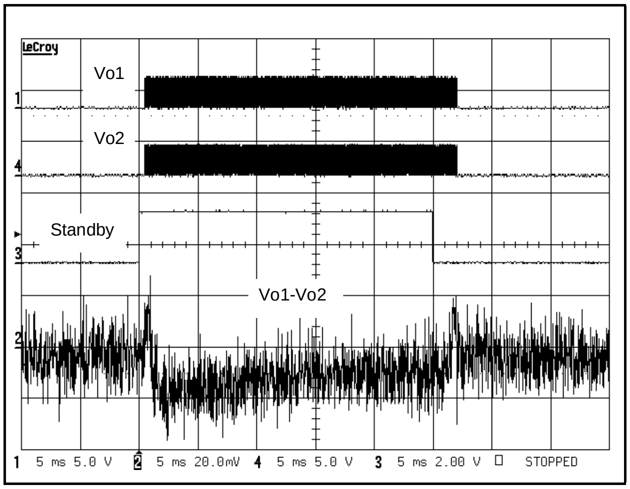


Figure 71: Startup & shutdown time
Vcc=5V, G=6dB, NoC_{IN} (5ms/div)

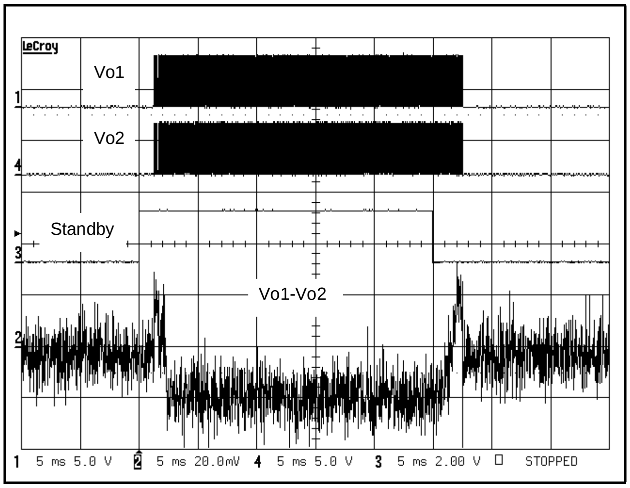
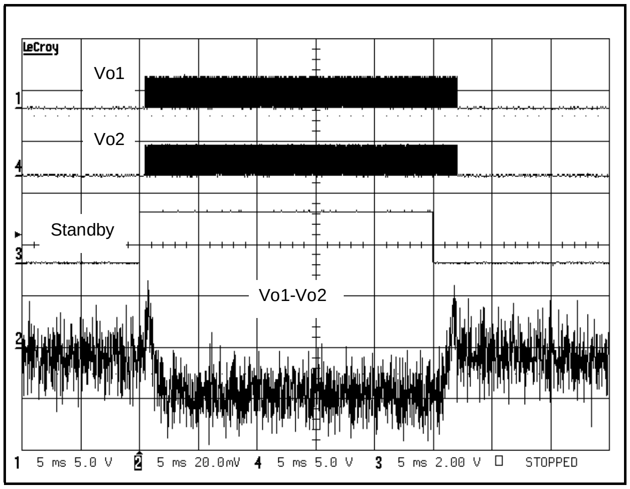


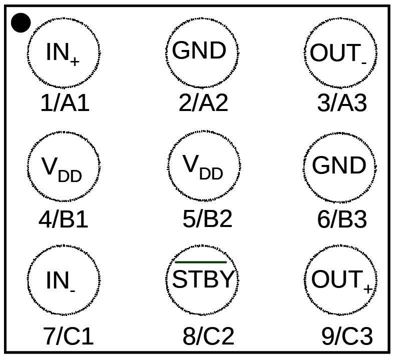
Figure 72: Startup & shutdown time
Vcc=3V, G=6dB, NoC_{IN} (5ms/div)



4 Package Mechanical Data

4.1 9 CONNECTIONS - Flip-Chip 300µm bump diam.

Figure 73: Pin out (top view)



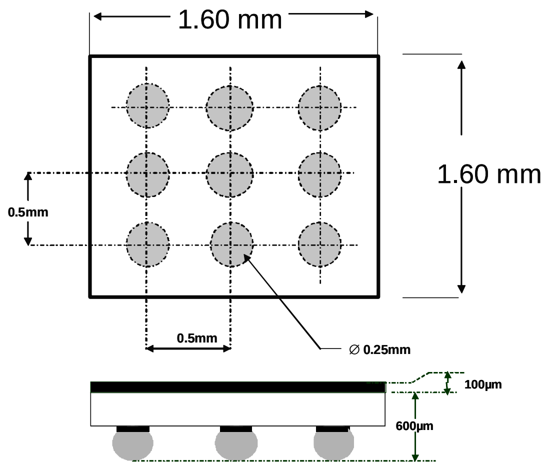
- Balls are underneath

Figure 74: Marking (top view)

Marking: A62

- ST Logo
- Part Number: A62
- Three digits Datecode: YWW
- E symbol for lead-free only
- The dot is for marking pin A1

4.2 FLIP CHIP - 9 BUMPS



- Die size : **1.6mm x 1.6mm** ±30µ**m**
- Die height (including bumps) : **600**µ**m**
- Bump diameter : **315**µ**m** ±**50**µ**m**
- Bump diameter before Reflow : **300**µ**m** ±**10**µ**m**
- Bump height: **250**µ**m** ±4**0**µ**m**
- Die Height: **350**µ**m** ±2**0**µ**m**
- Pitch: **500**µ**m** ±**50**µ**m**
- ***Back Coating layer Height : **100**µ**m** ±**10**µ**m**
- Coplanarity: **60**µ**m max**

*** Optional**

5 Revision History

Date	Revision	Description of Changes
01 Nov 2004	1	First Release

STMicroelectronics group of companies
Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America
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