

## 1W Differential Input/Output Audio Power Amplifier with Selectable Standby

- Differential inputs
- Near zero pop & click
- 100dB PSRR @ 217Hz with grounded inputs
- Operating from  $V_{CC} = 2.5V$  to  $5.5V$
- 1W RAIL to RAIL output power @  $V_{CC}=5V$ , THD=1%, F=1kHz, with  $8\Omega$  load
- 90dB CMRR @ 217Hz
- Ultra-low consumption in standby mode (10nA)
- Selectable standby mode (active low or active high)
- Ultra fast startup time: 15ms typ.
- Available in flip-chip 300um/9 bumps, DFN10 3x3, 0.5mm pitch & miniso-8
- All lead-free packages

### Description

The TS4994 is an audio power amplifier capable of delivering 1W of continuous RMS output power into an  $8\Omega$  load @ 5V. Thanks to its differential inputs, it exhibits outstanding noise immunity.

An external standby mode control reduces the supply current to less than 10nA. A STBY MODE pin allows the standby pin to be active HIGH or LOW (except in the MiniSO8 version). An internal thermal shutdown protection is also provided, making the device capable of sustaining short-circuits.

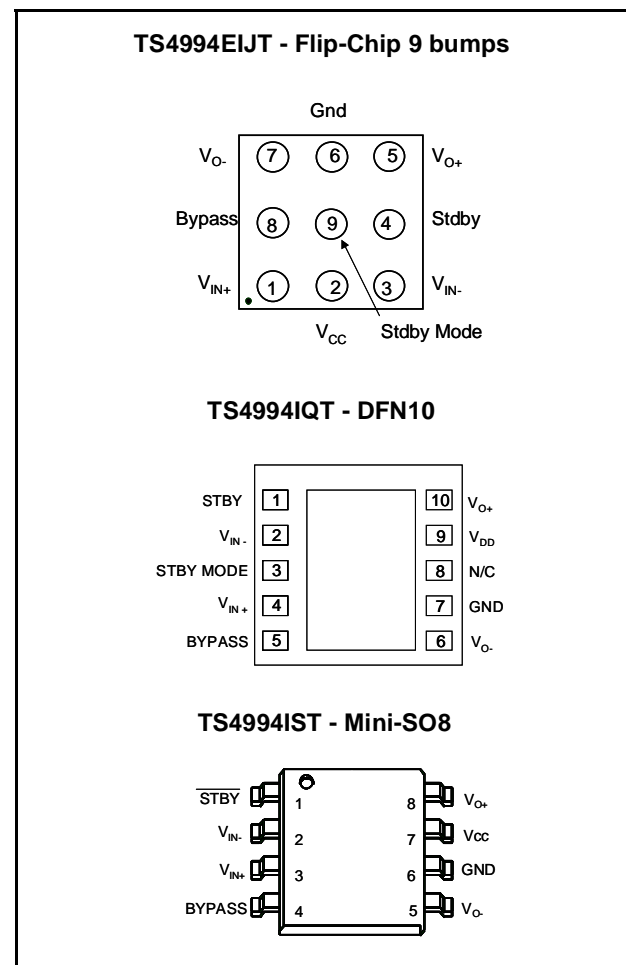
The device is equipped with Common Mode Feedback circuitry allowing outputs to be always biased at  $V_{CC}/2$  regardless of the input common mode voltage.

The TS4994 has been designed for high quality audio applications such as mobile phones and requires few external components.

### Applications

- Mobile phones (cellular / cordless)
- Laptop / notebook computers
- PDAs
- Portable audio devices

### PIN CONNECTIONS (top view)



### ORDER CODES

Part Number	Temperature Range	Package	Packaging	Marking
TS4994EIJT	-40, +85°C	Lead free Flip-Chip9	Tape & Reel	A94
TS4994IQT		DFN10		K994
TS4994IST		miniSO-8		K994

# 1 Application Component Information

Components	Functional Description
$C_S$	Supply Bypass capacitor which provides power supply filtering.
$C_B$	Bypass capacitor which provides half supply filtering.
$R_{FEED}$	Feedback resistor which sets the closed loop gain in conjunction with $R_{IN}$ $A_V = \text{Closed Loop Gain} = R_{FEED}/R_{IN}$ .
$R_{IN}$	Inverting input resistor which sets the closed loop gain in conjunction with $R_{FEED}$ .
$C_{IN}$	Optional input capacitor making a high pass filter together with $R_{IN}$ . ( $f_{cl} = 1 / (2 \times \text{Pi} \times R_{IN} \times C_{IN})$ )

Figure 1: Typical Application Flip-Chip Version

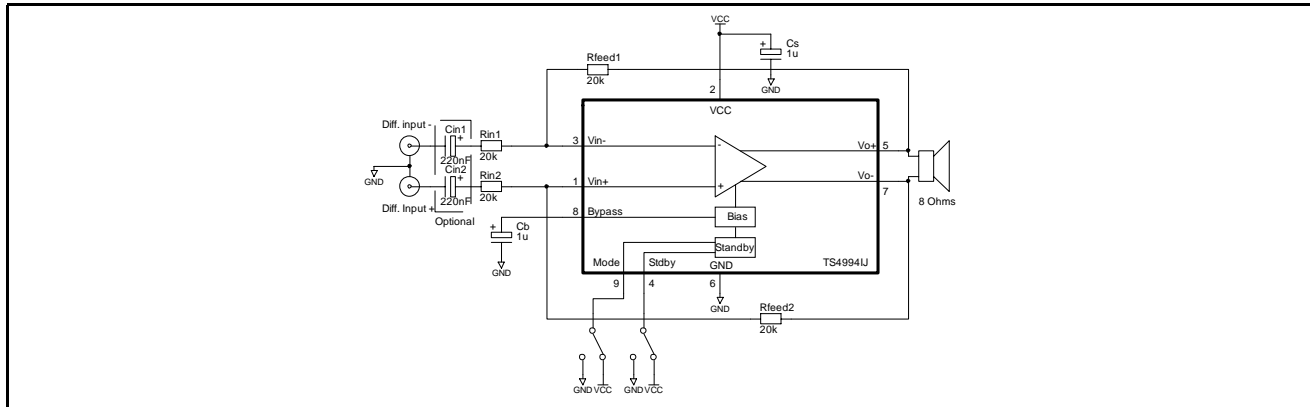


Figure 2: Typical Application DFN10 Version

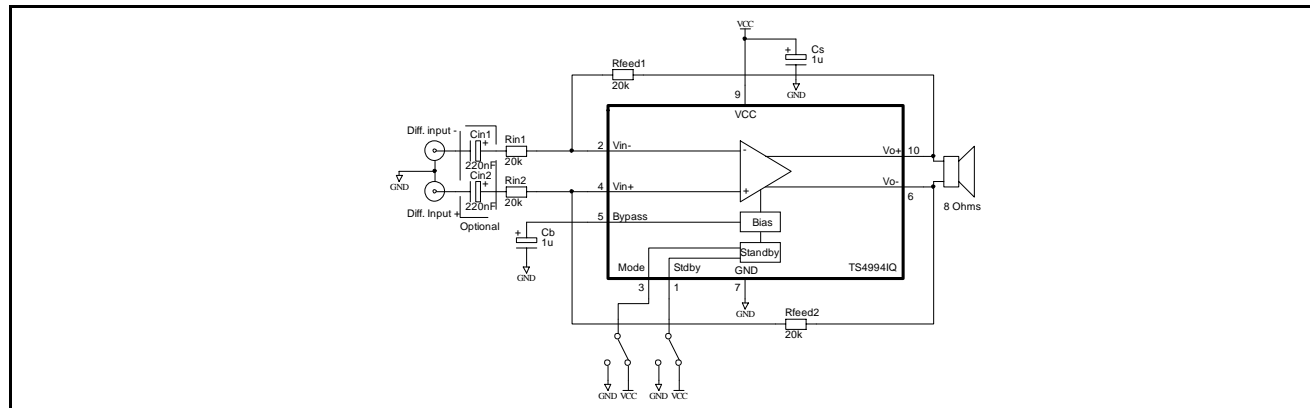
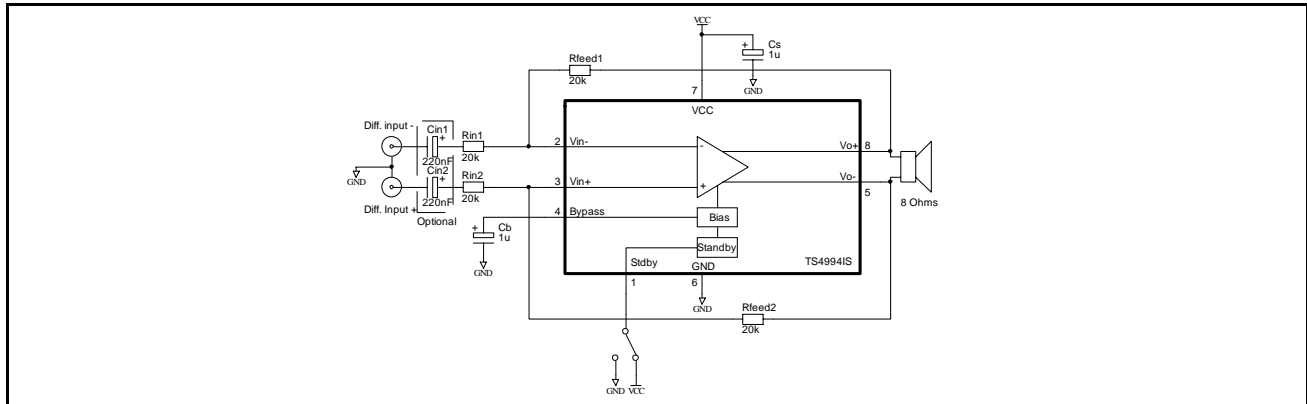


Figure 3: Typical Application Mini-SO8 Version



## 2 Absolute Maximum Ratings

Table 1: Key parameters and their absolute maximum ratings

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply voltage <sup>1</sup>	6	V
V <sub>i</sub>	Input Voltage <sup>2</sup>	G <sub>ND</sub> to V <sub>CC</sub>	V
T <sub>oper</sub>	Operating Free Air Temperature Range	-40 to + 85	°C
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>j</sub>	Maximum Junction Temperature	150	°C
R <sub>thja</sub>	Thermal Resistance Junction to Ambient <sup>3</sup> DFN10 Flip-Chip Mini-SO8	120 250 215	°C/W
P <sub>d</sub>	Power Dissipation	internally limited	W
ESD	Human Body Model	2	kV
ESD	Machine Model	200	V
	Latch-up Immunity	200	mA
	Lead Temperature (soldering, 10sec)	260	°C

1) All voltages values are measured with respect to the ground pin.

2) The magnitude of input signal must never exceed V<sub>CC</sub> + 0.3V / G<sub>ND</sub> - 0.3V

3) The device is protected by a thermal shutdown active at 150°C

Table 2: Operating conditions

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage	2.5 to 5.5	V
V <sub>SM</sub>	Standby Mode Voltage Input: Standby Active LOW Standby Active HIGH	V <sub>SM</sub> =GND V <sub>SM</sub> =V <sub>CC</sub>	V
V <sub>STB</sub>	Standby Voltage Input: Device ON (V <sub>SM</sub> =GND) or Device OFF (V <sub>SM</sub> =V <sub>CC</sub> ) Device OFF (V <sub>SM</sub> =GND) or Device ON (V <sub>SM</sub> =V <sub>CC</sub> )	1.5 ≤ V <sub>STB</sub> ≤ V <sub>CC</sub> G <sub>ND</sub> ≤ V <sub>STB</sub> ≤ 0.4 <sup>1</sup>	V
T <sub>SD</sub>	Thermal Shutdown Temperature	150	°C
R <sub>L</sub>	Load Resistor	≥ 8	Ω
R <sub>THJA</sub>	Thermal Resistance Junction to Ambient DFN10 <sup>2</sup> Flip-Chip Mini-SO8	80 100 190	°C/W

1) The minimum current consumption (I<sub>STANDBY</sub>) is guaranteed when V<sub>STB</sub>=GND or V<sub>CC</sub> (i.e. supply rails) for the whole temperature

2) When mounted on a 4-layer PCB.

### 3 Electrical Characteristics

**Table 3: Electrical characteristics -  $V_{CC} = +5V$ ,  $GND = 0V$ ,  $T_{amb} = 25^{\circ}C$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{CC}$	Supply Current No input signal, no load		4	7	mA
$I_{STANDBY}$	Standby Current No input signal, $V_{stdby} = V_{SM} = G_{ND}$ , $R_L = 8\Omega$ No input signal, $V_{stdby} = V_{SM} = V_{CC}$ , $R_L = 8\Omega$		10	1000	nA
$V_{OO}$	Differential Output Offset Voltage No input signal, $R_L = 8\Omega$		0.1	10	mV
$V_{ICM}$	Input Common Mode Voltage $CMRR \leq -60dB$	0.6		$V_{CC} - 0.9$	V
$P_o$	Output Power $THD = 1\% \text{ Max}$ , $F = 1kHz$ , $R_L = 8\Omega$	0.8	1		W
THD + N	Total Harmonic Distortion + Noise $P_o = 850mW \text{ rms}$ , $A_v = 1$ , $20Hz \leq F \leq 20kHz$ , $R_L = 8\Omega$		0.5		%
$PSRR_{IG}$	Power Supply Rejection Ratio with Inputs Grounded <sup>1</sup> $F = 217Hz$ , $R = 8\Omega$ , $A_v = 1$ , $C_{in} = 4.7\mu F$ , $C_b = 1\mu F$ $V_{ripple} = 200mV_{PP}$		100		dB
CMRR	Common Mode Rejection Ratio $F = 217Hz$ , $R_L = 8\Omega$ , $A_v = 1$ , $C_{in} = 4.7\mu F$ , $C_b = 1\mu F$ $V_{ic} = 200mV_{PP}$		90		dB
SNR	Signal-to-Noise Ratio (A Weighted Filter, $A_v = 2.5$ ) ( $R_L = 8\Omega$ , $THD + N < 0.7\%$ , $20Hz \leq F \leq 20kHz$ )		100		dB
GBP	Gain Bandwidth Product $R_L = 8\Omega$		2		MHz
$V_N$	Output Voltage Noise, $20Hz \leq F \leq 20kHz$ , $R_L = 8\Omega$ Unweighted, $A_v = 1$ A weighted, $A_v = 1$ Unweighted, $A_v = 2.5$ A weighted, $A_v = 2.5$ Unweighted, $A_v = 7.5$ A weighted, $A_v = 7.5$ Unweighted, Standby A weighted, Standby		6 5.5 12 10.5 33 28 1.5 1		$\mu V_{RMS}$
$T_{WU}$	Wake-Up Time <sup>2</sup> $C_b = 1\mu F$		15		ms

1) Dynamic measurements -  $20 \cdot \log(\text{rms}(V_{out})/\text{rms}(V_{ripple}))$ . Vripple is the super-imposed sinus signal relative to  $V_{cc}$ .

2) Time from standby transition to have fully operational amplifier.

**Table 4: Electrical Characteristics:  $V_{CC} = +3.3V$  (all electrical values are guaranteed with correlation measurements at 2.6V and 5V)  $GND = 0V$ ,  $T_{amb} = 25^{\circ}C$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{CC}$	Supply Current No input signal, no load		3	7	mA
$I_{STANDBY}$	Standby Current No input signal, $V_{stdby} = V_{SM} = G_{ND}$ , $R_L = 8\Omega$ No input signal, $V_{stdby} = V_{SM} = V_{CC}$ , $R_L = 8\Omega$		10	1000	nA
$V_{OO}$	Differential Output Offset Voltage No input signal, $R_L = 8\Omega$		0.1	10	mV
$V_{ICM}$	Input Common Mode Voltage $CMRR \leq -60dB$	0.6		$V_{CC} - 0.9$	V
$P_o$	Output Power $THD = 1\% \text{ Max}$ , $F = 1kHz$ , $R_L = 8\Omega$	300	380		mW
THD + N	Total Harmonic Distortion + Noise $P_o = 300mW \text{ rms}$ , $A_v = 1$ , $20Hz \leq F \leq 20kHz$ , $R_L = 8\Omega$		0.5		%
$PSRR_{IG}$	Power Supply Rejection Ratio with Inputs Grounded <sup>1</sup> $F = 217Hz$ , $R = 8\Omega$ , $A_v = 1$ , $C_{in} = 4.7\mu F$ , $C_b = 1\mu F$ Vripple = 200mV <sub>PP</sub>		100		dB
CMRR	Common Mode Rejection Ratio $F = 217Hz$ , $R_L = 8\Omega$ , $A_v = 1$ , $C_{in} = 4.7\mu F$ , $C_b = 1\mu F$ $V_{ic} = 200mV_{PP}$		90		dB
SNR	Signal-to-Noise Ratio (A Weighted Filter, $A_v = 2.5$ ) ( $R_L = 8\Omega$ , $THD + N < 0.7\%$ , $20Hz \leq F \leq 20kHz$ )		100		dB
GBP	Gain Bandwidth Product $R_L = 8\Omega$		2		MHz
$V_N$	Output Voltage Noise, $20Hz \leq F \leq 20kHz$ , $R_L = 8\Omega$ Unweighted, $A_v = 1$ A weighted, $A_v = 1$ Unweighted, $A_v = 2.5$ A weighted, $A_v = 2.5$ Unweighted, $A_v = 7.5$ A weighted, $A_v = 7.5$ Unweighted, Standby A weighted, Standby		6 5.5 12 10.5 33 28 1.5 1		$\mu V_{RMS}$
$T_{WU}$	Wake-Up Time <sup>2</sup> $C_b = 1\mu F$		15		ms

1) Dynamic measurements -  $20 \cdot \log(\text{rms}(V_{out})/\text{rms}(V_{ripple}))$ . Vripple is the super-imposed sinus signal relative to  $V_{cc}$ .

2) Time from standby transition to have fully operational amplifier.

Table 5: Electrical Characteristics -  $V_{CC} = +2.6V$ ,  $GND = 0V$ ,  $T_{amb} = 25^{\circ}C$  (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{CC}$	Supply Current No input signal, no load		3	7	mA
$I_{STANDBY}$	Standby Current No input signal, $V_{stdby} = V_{SM} = G_{ND}$ , $R_L = 8\Omega$ No input signal, $V_{stdby} = V_{SM} = V_{CC}$ , $R_L = 8\Omega$		10	1000	nA
$V_{OO}$	Differential Output Offset Voltage No input signal, $R_L = 8\Omega$		0.1	10	mV
$V_{ICM}$	Input Common Mode Voltage $CMRR \leq -60dB$	0.6		$V_{CC} - 0.9$	V
$P_O$	Output Power $THD = 1\% \text{ Max}$ , $F = 1kHz$ , $R_L = 8\Omega$	200	250		mW
THD + N	Total Harmonic Distortion + Noise $P_O = 225mW \text{ rms}$ , $A_v = 1$ , $20Hz \leq F \leq 20kHz$ , $R_L = 8\Omega$		0.5		%
$PSRR_{IG}$	Power Supply Rejection Ratio with Inputs Grounded <sup>1</sup> $F = 217Hz$ , $R = 8\Omega$ , $A_v = 1$ , $C_{in} = 4.7\mu F$ , $C_b = 1\mu F$ $V_{ripple} = 200mV_{PP}$		100		dB
CMRR	Common Mode Rejection Ratio $F = 217Hz$ , $R_L = 8\Omega$ , $A_v = 1$ , $C_{in} = 4.7\mu F$ , $C_b = 1\mu F$ $V_{ic} = 200mV_{PP}$		90		dB
SNR	Signal-to-Noise Ratio (A Weighted Filter, $A_v = 2.5$ ) ( $R_L = 8\Omega$ , $THD + N < 0.7\%$ , $20Hz \leq F \leq 20kHz$ )		100		dB
GBP	Gain Bandwidth Product $R_L = 8\Omega$		2		MHz
$V_N$	Output Voltage Noise, $20Hz \leq F \leq 20kHz$ , $R_L = 8\Omega$ Unweighted, $A_v = 1$ A weighted, $A_v = 1$ Unweighted, $A_v = 2.5$ A weighted, $A_v = 2.5$ Unweighted, $A_v = 7.5$ A weighted, $A_v = 7.5$ Unweighted, Standby A weighted, Standby		6 5.5 12 10.5 33 28 1.5 1		$\mu V_{RMS}$
$T_{WU}$	Wake-Up Time <sup>2</sup> $C_b = 1\mu F$		15		ms

1) Dynamic measurements -  $20 \cdot \log(\text{rms}(V_{out})/\text{rms}(V_{ripple}))$ . Vripple is the super-imposed sinus signal relative to  $V_{CC}$ .

2) Time from standby transition to have fully operational amplifier.

Figure 4: Current consumption vs. power supply voltage

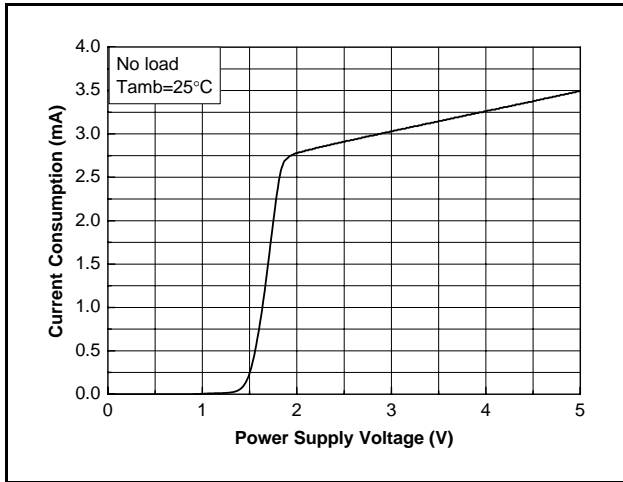


Figure 7: Current consumption vs. standby voltage

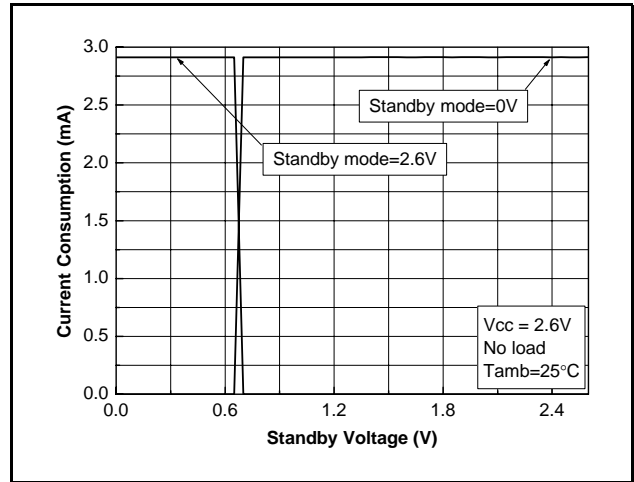


Figure 5: Current consumption vs. standby voltage

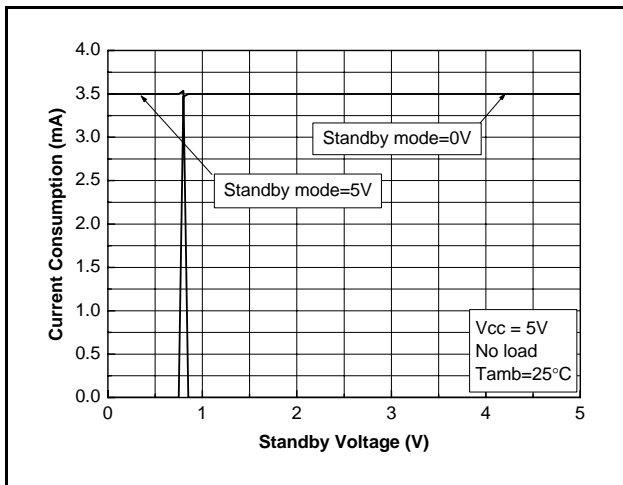


Figure 8: Differential DC output voltage vs. common mode input voltage

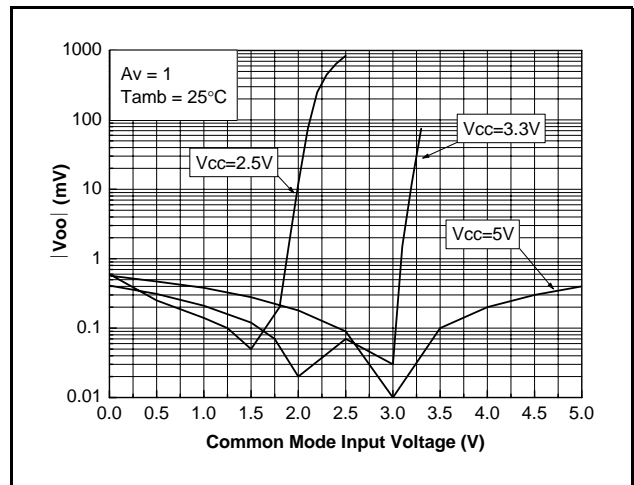


Figure 6: Current consumption vs. standby voltage

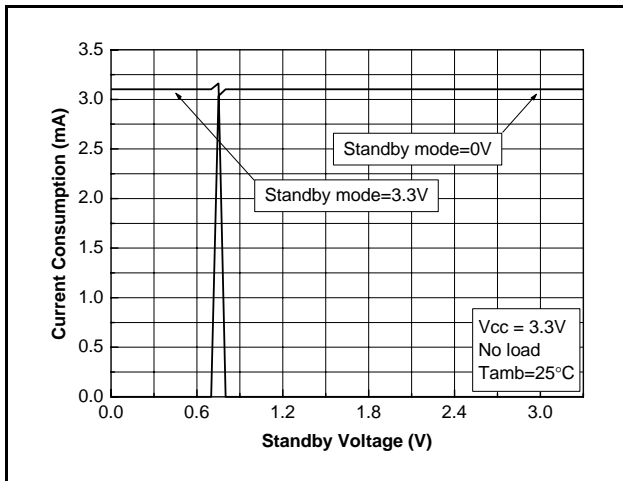


Figure 9: Power dissipation vs. output power

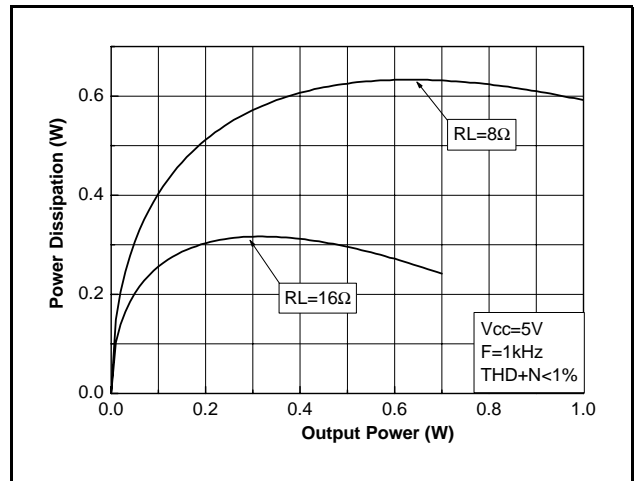




Figure 10: Power dissipation vs. output power

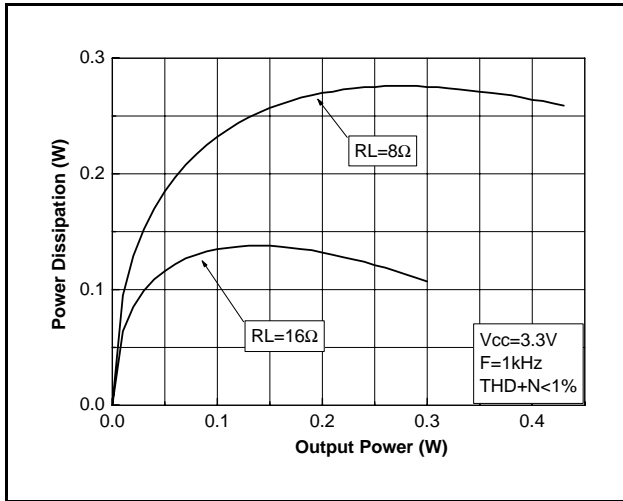


Figure 13: Output power vs. power supply voltage

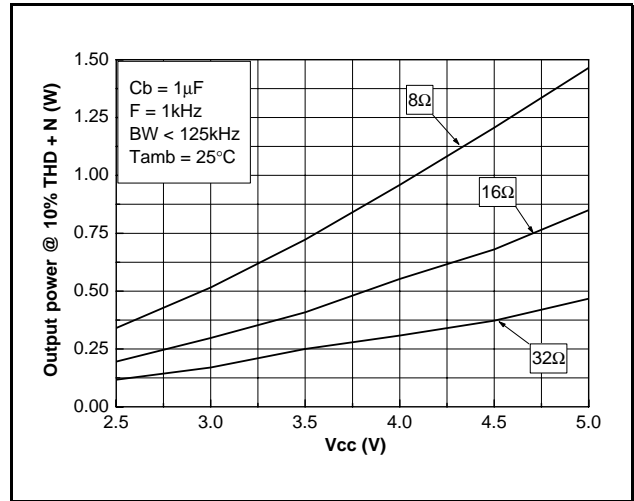


Figure 11: Power dissipation vs. output power

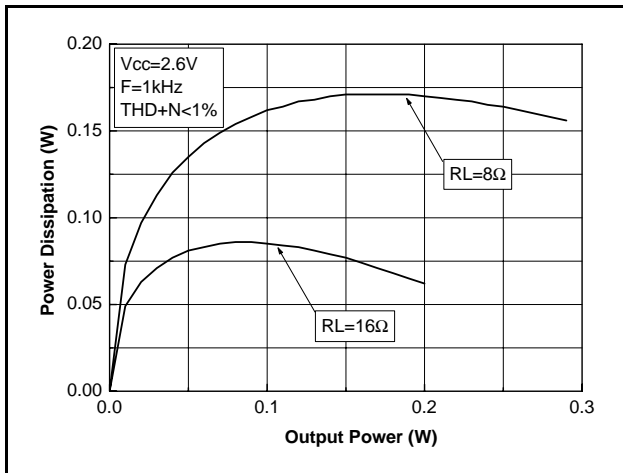


Figure 14: Output power vs. load resistance

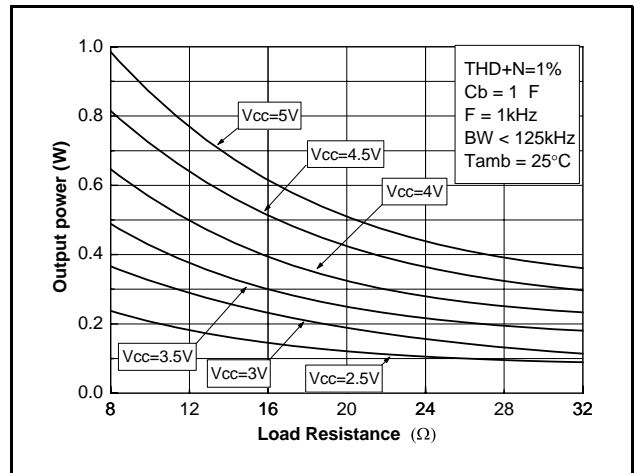


Figure 12: Output power vs. power supply voltage

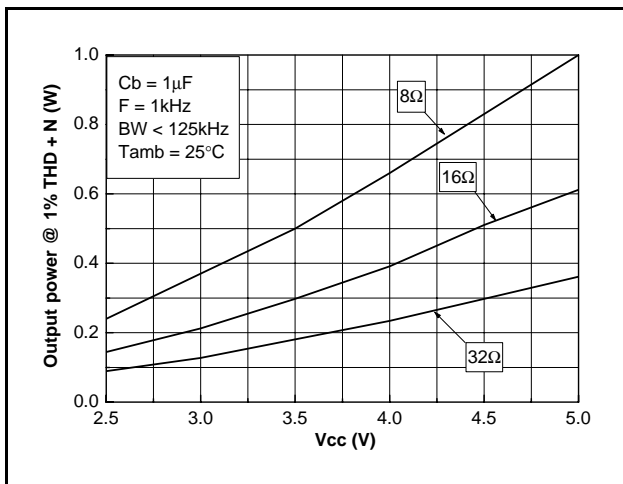


Figure 15: Power derating curves

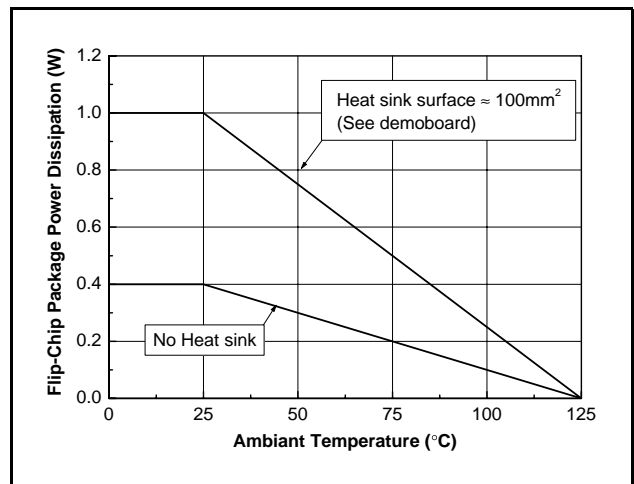


Figure 16: Power derating curves

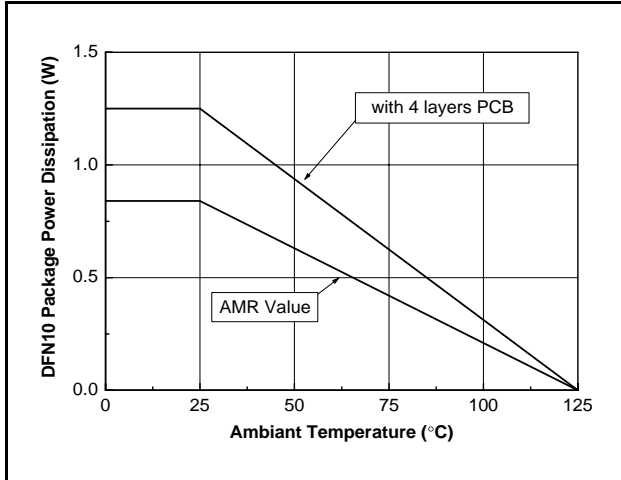


Figure 19: Open loop gain vs. frequency

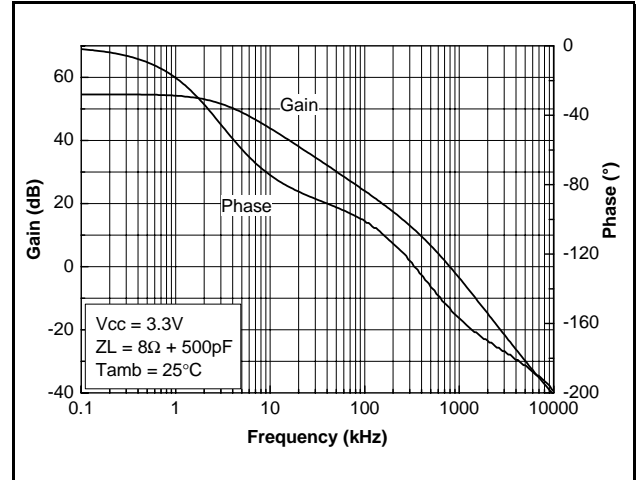


Figure 17: Power derating curves

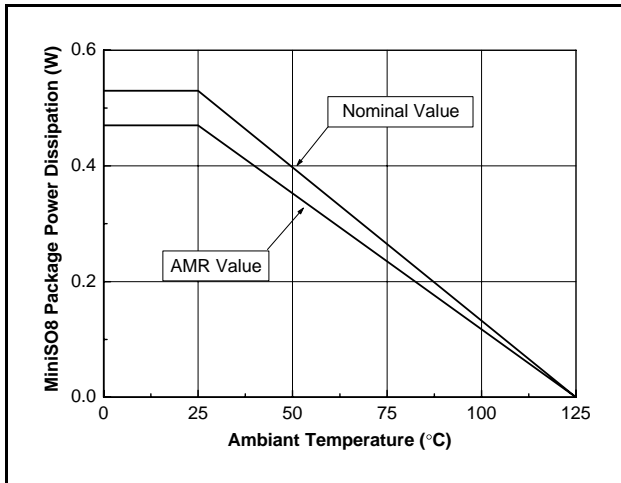


Figure 20: Open Loop gain vs. frequency

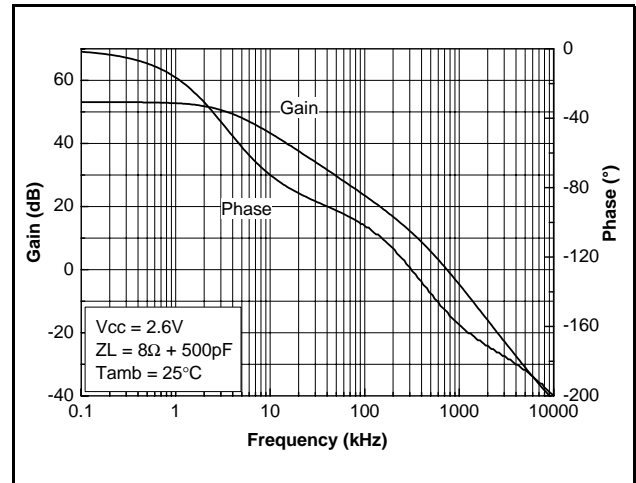


Figure 18: Open loop gain vs. frequency

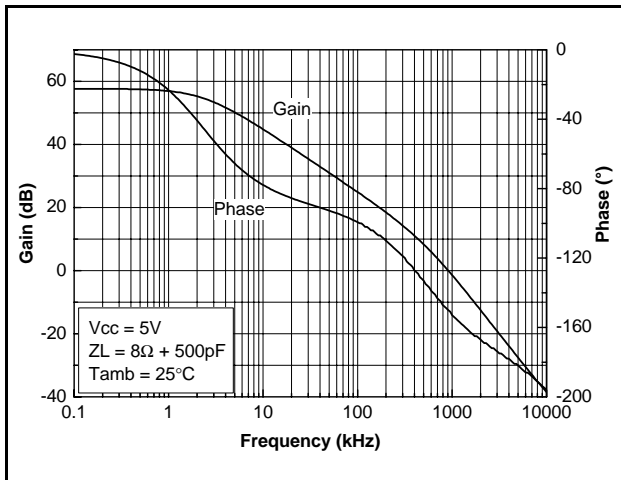


Figure 21: Close loop gain vs. frequency

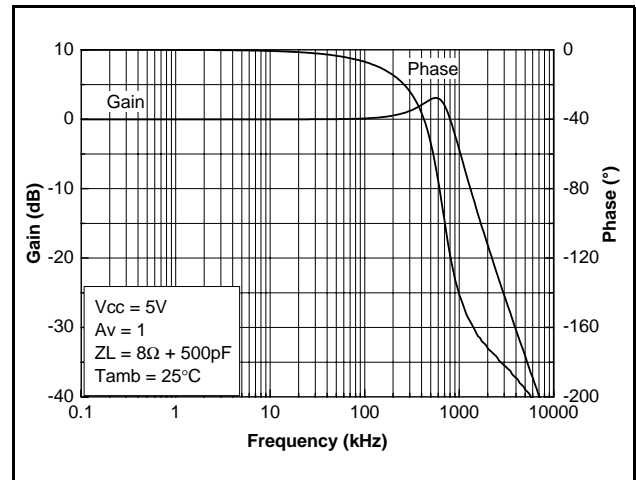


Figure 22: Close loop gain vs. frequency

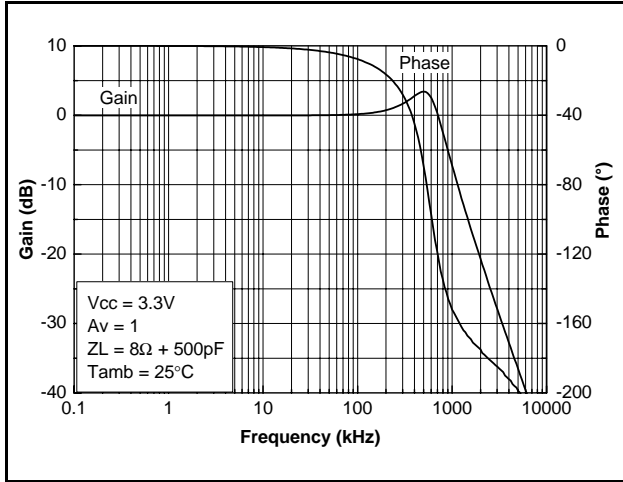


Figure 25: PSRR vs. frequency

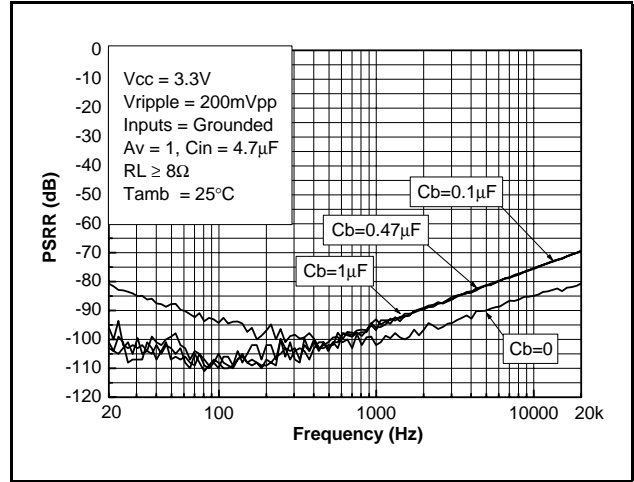


Figure 23: Close loop gain vs. frequency

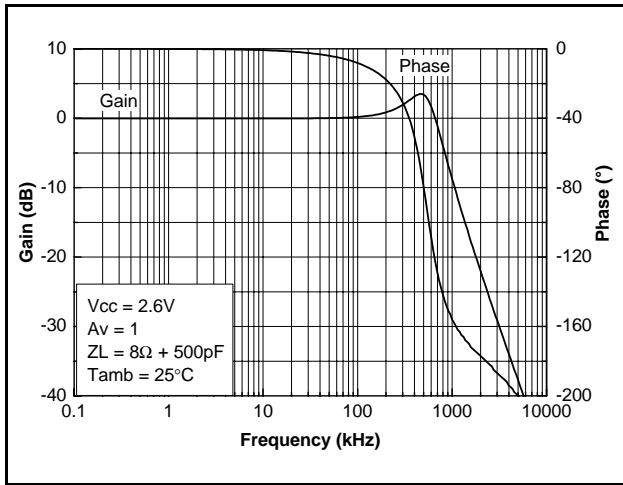


Figure 26: PSRR vs. frequency

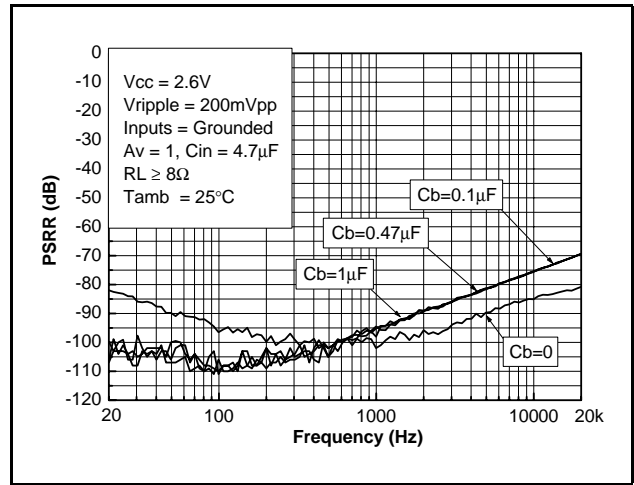


Figure 24: PSRR vs. frequency

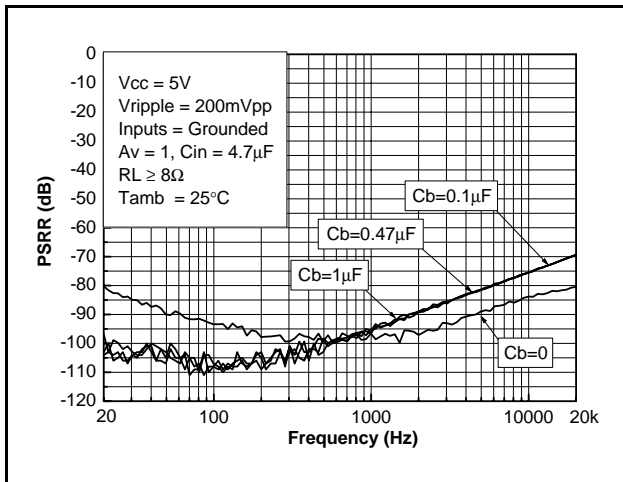


Figure 27: PSRR vs. frequency

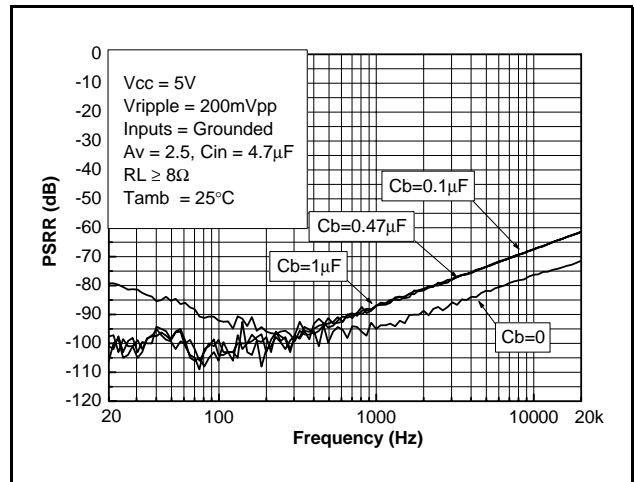


Figure 28: PSRR vs. frequency

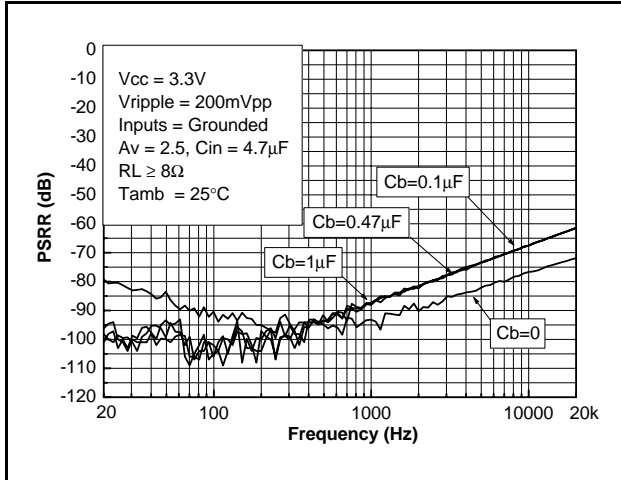


Figure 31: PSRR vs. frequency

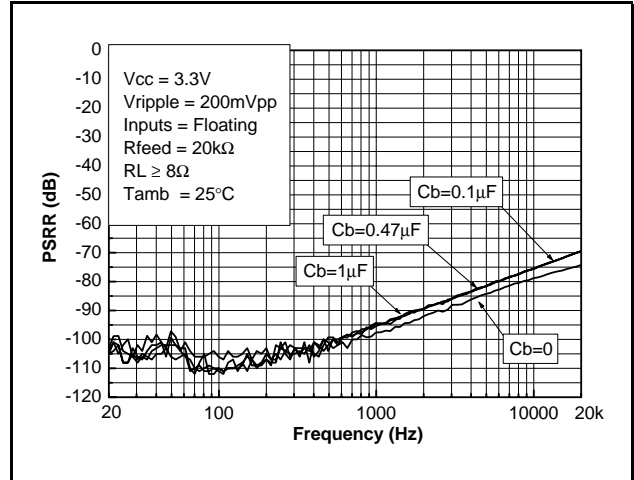


Figure 29: PSRR vs. frequency

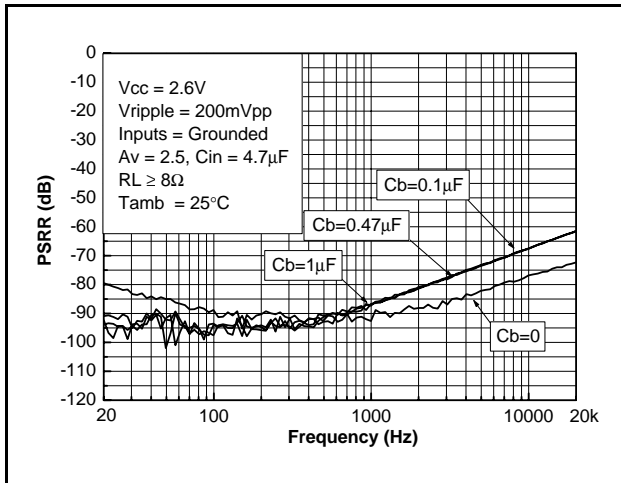


Figure 32: PSRR vs. frequency

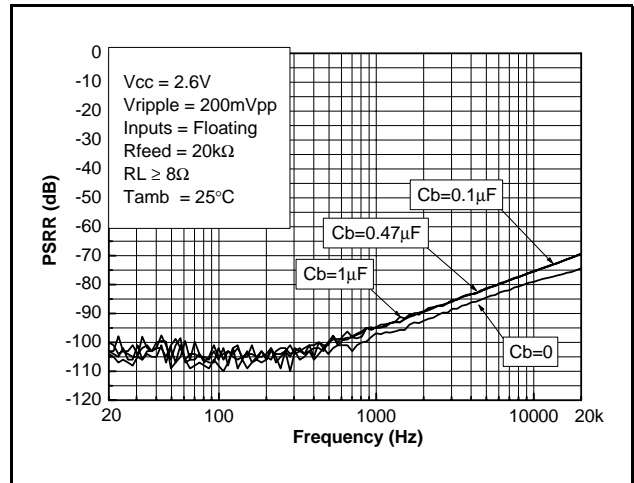


Figure 30: PSRR vs. frequency

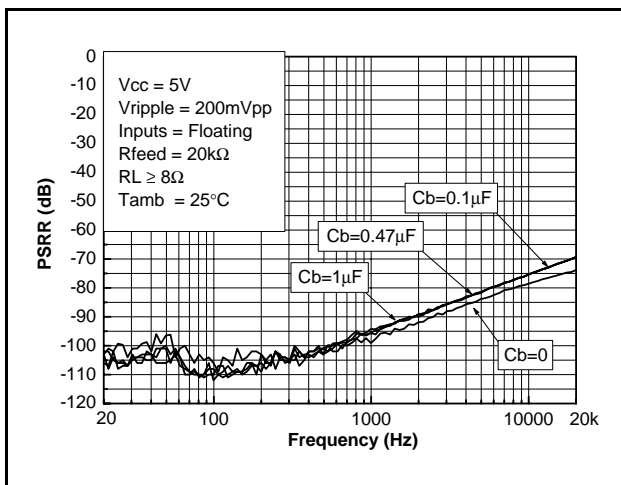


Figure 33: PSRR vs. common mode input voltage

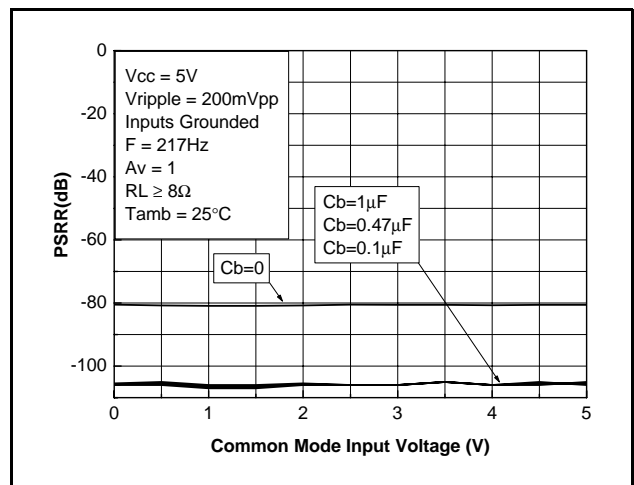


Figure 34: PSRR vs. common mode input voltage

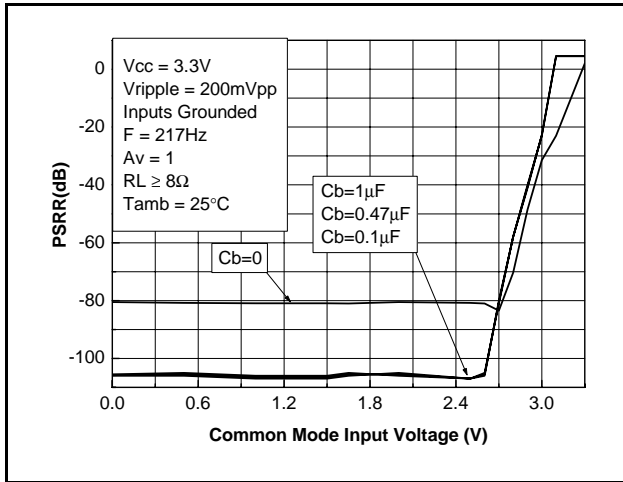


Figure 37: PSRR vs. frequency

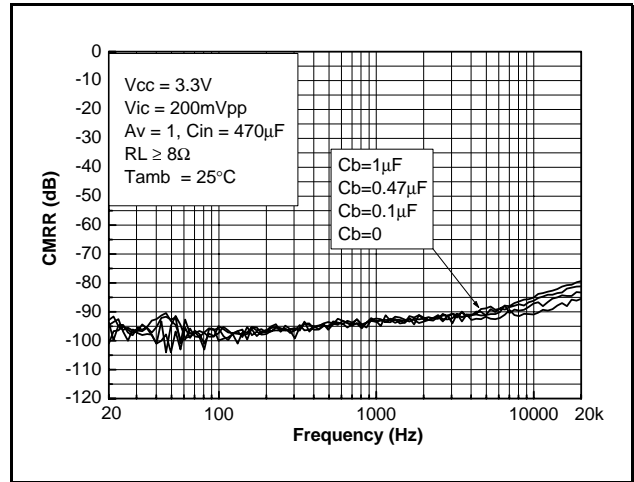


Figure 35: PSRR vs. common mode input voltage

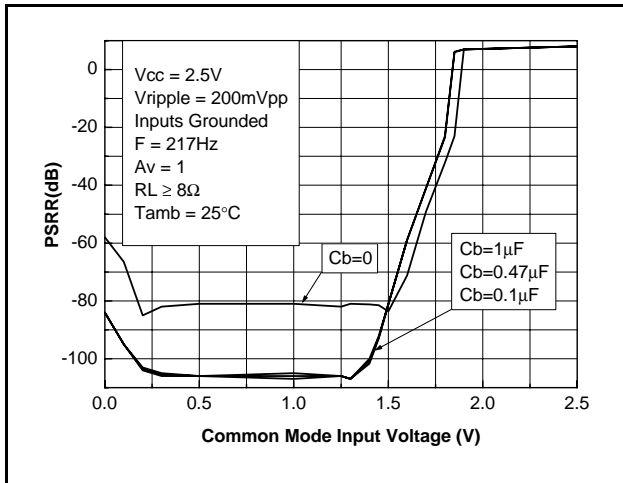


Figure 38: CMRR vs. frequency

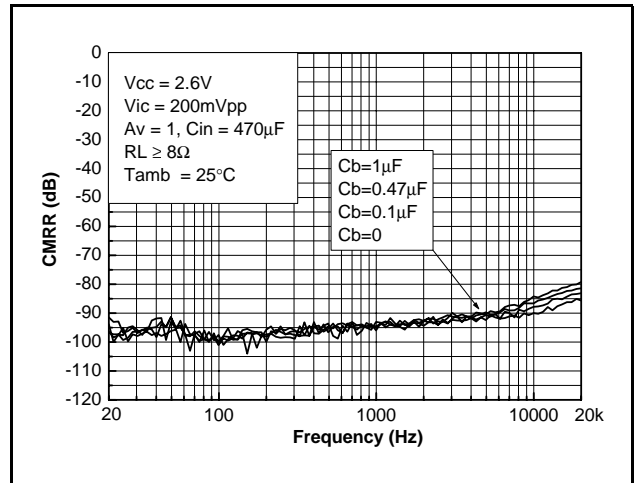


Figure 36: CMRR vs. frequency

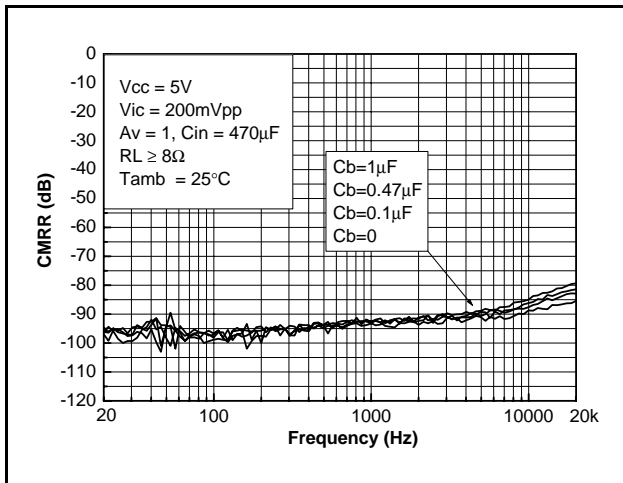


Figure 39: CMRR vs. frequency

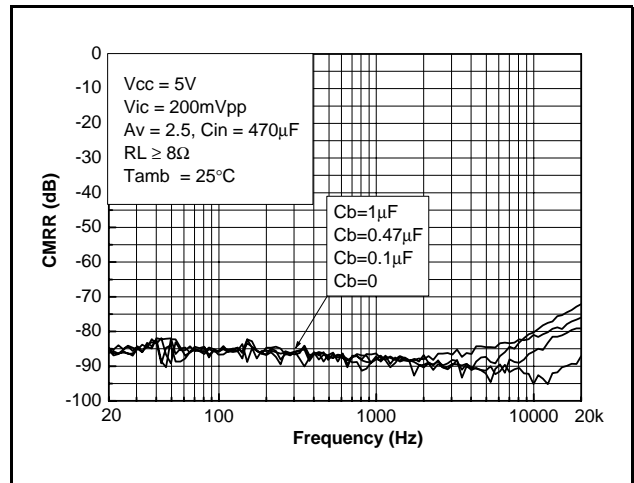


Figure 40: CMRR vs. frequency

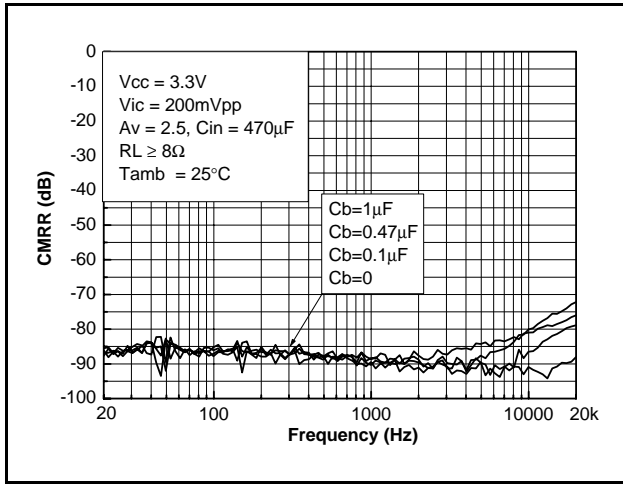


Figure 41: CMRR vs. frequency

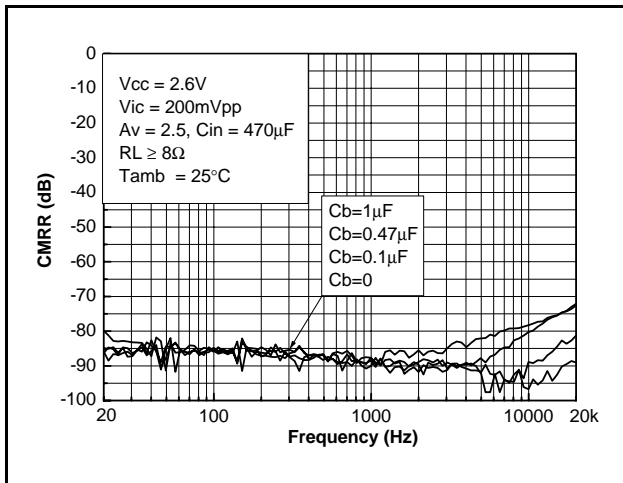


Figure 42: CMRR vs. common mode input voltage

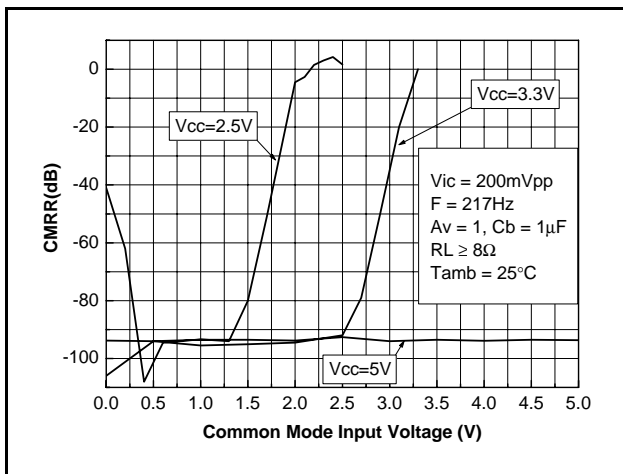


Figure 43: CMRR vs. common mode input voltage

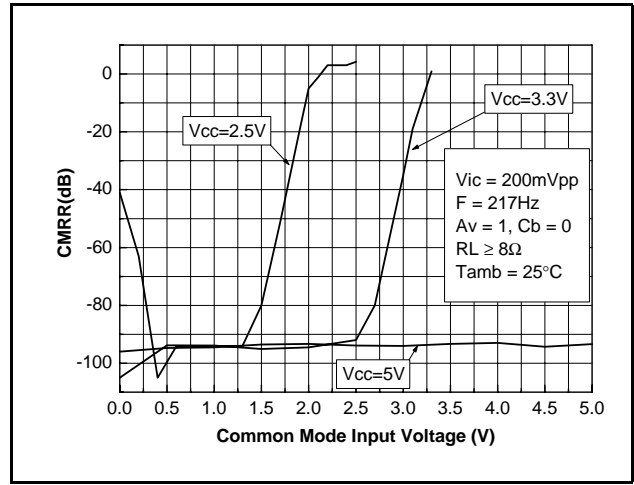


Figure 44: THD+N vs. output power

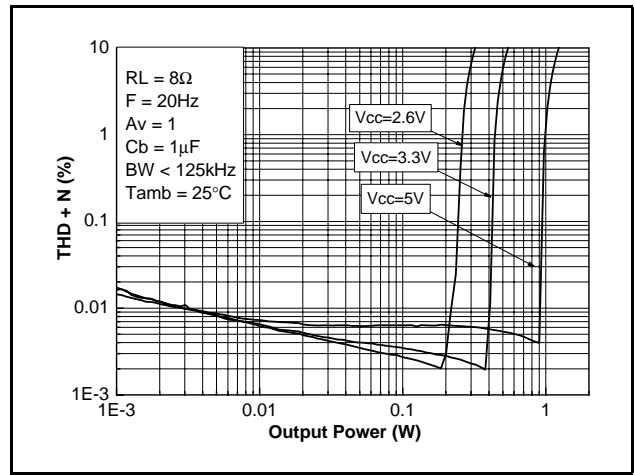


Figure 45: THD+N vs. output power

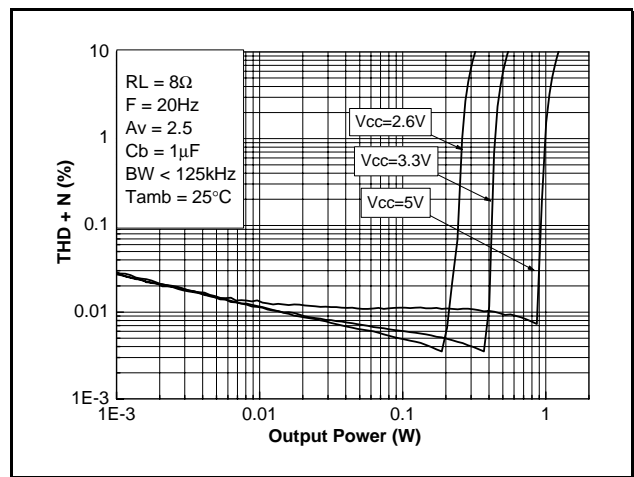


Figure 46: THD+N vs. output power

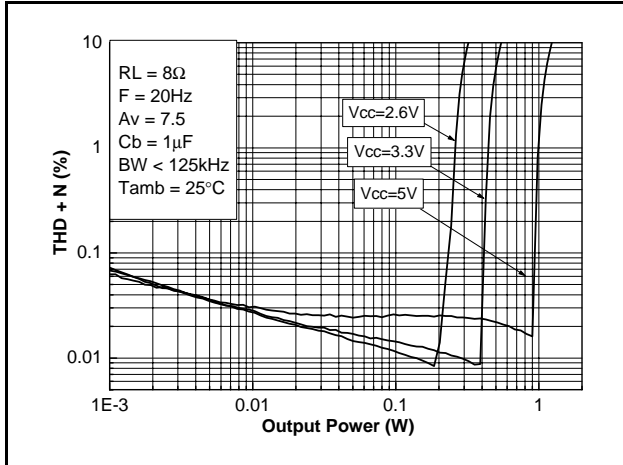


Figure 49: THD+N vs. output power

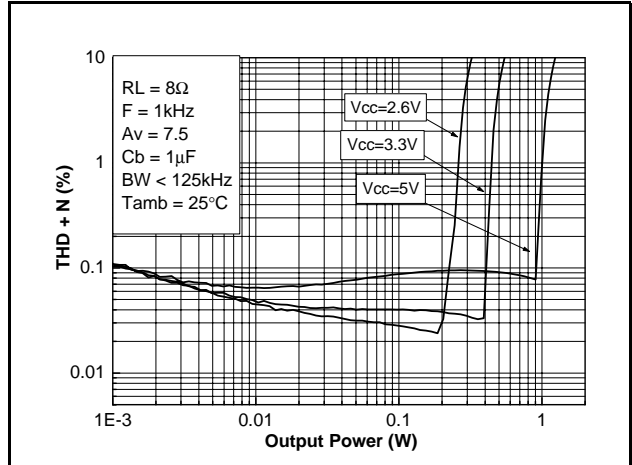


Figure 47: THD+N vs. output power

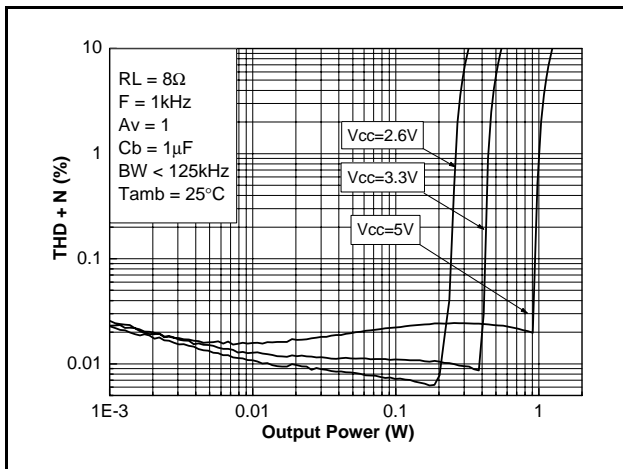


Figure 50: THD+N vs. output power

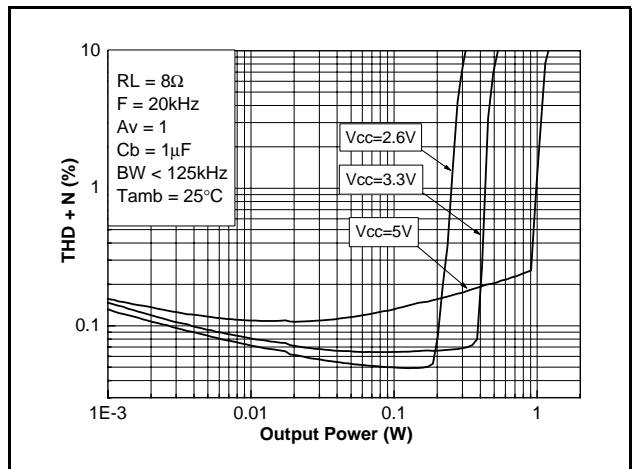


Figure 48: THD+N vs. output power

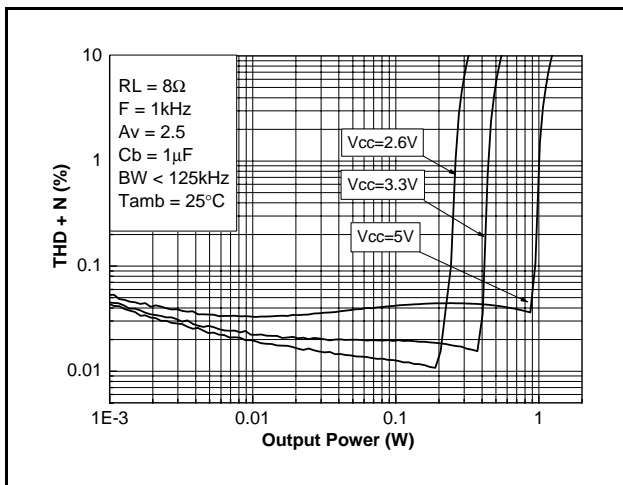


Figure 51: THD+N vs. output power

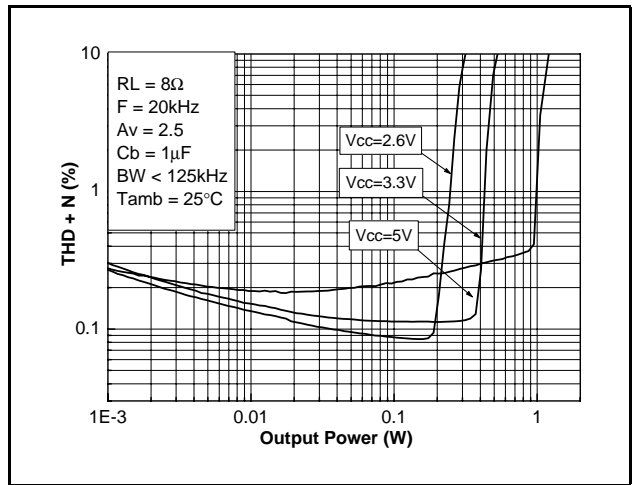


Figure 52: THD+N vs. output power

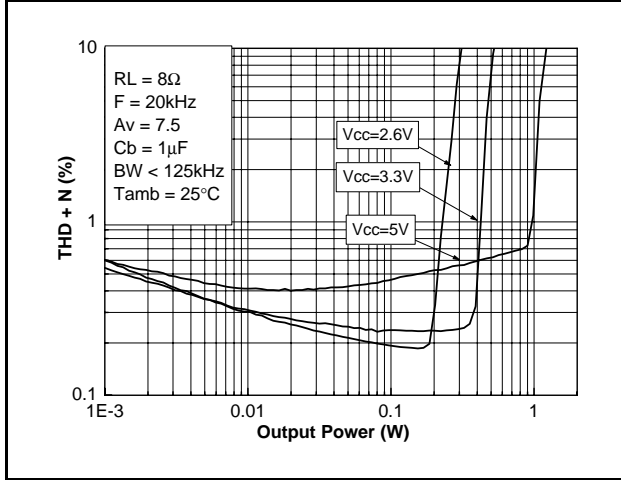


Figure 55: THD+N vs. output power

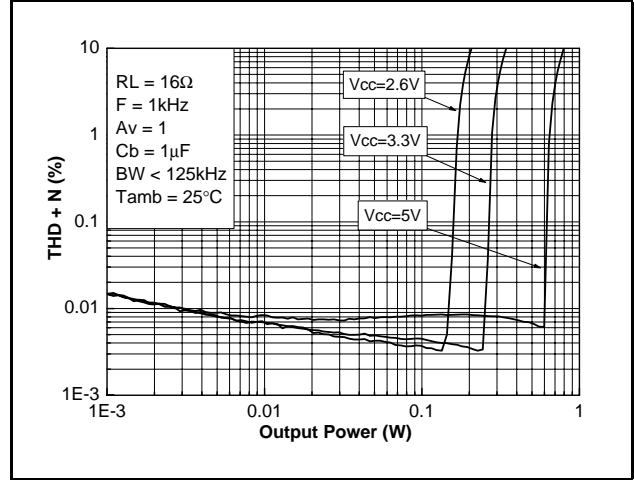


Figure 53: THD+N vs. output power

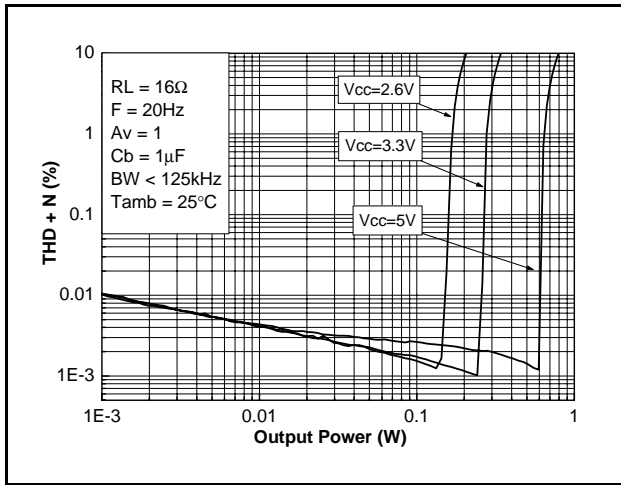


Figure 56: THD+N vs. output power

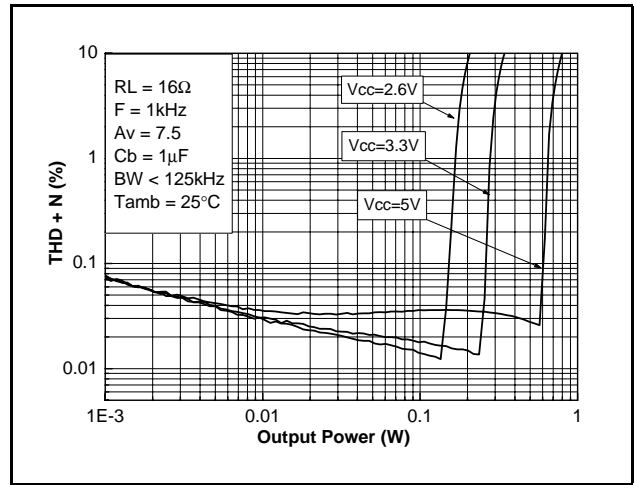


Figure 54: THD+N vs. output power

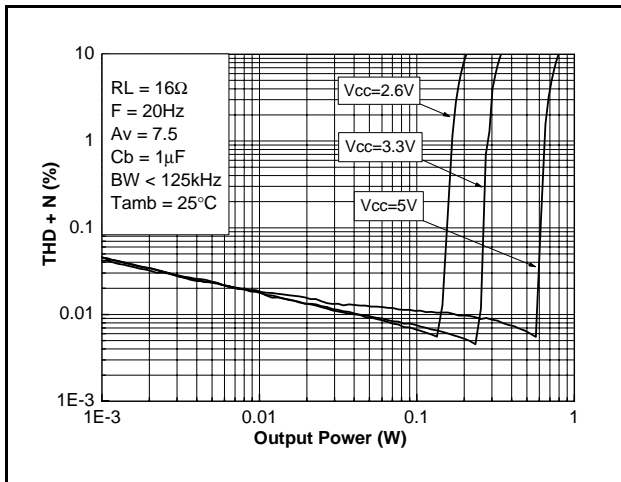


Figure 57: THD+N vs. output power

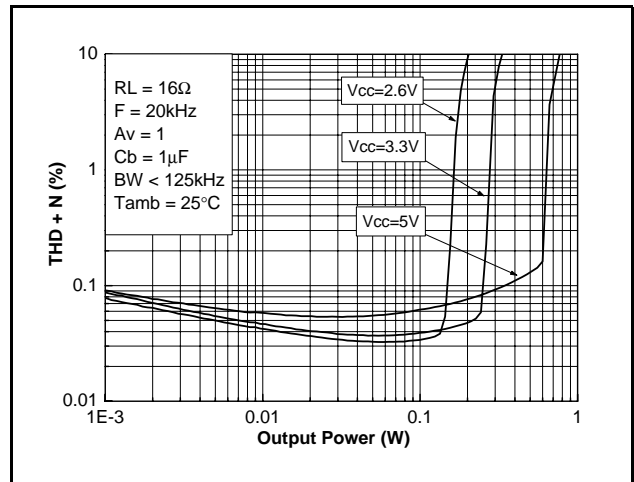




Figure 58: THD+N vs. output power

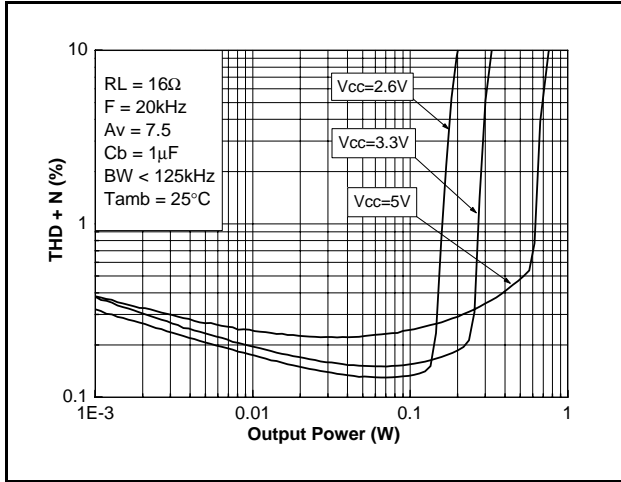


Figure 61: THD+N vs. output power

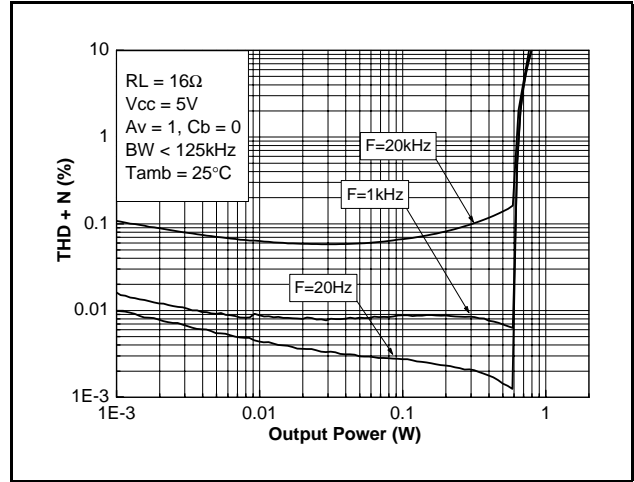


Figure 59: THD+N vs. output power

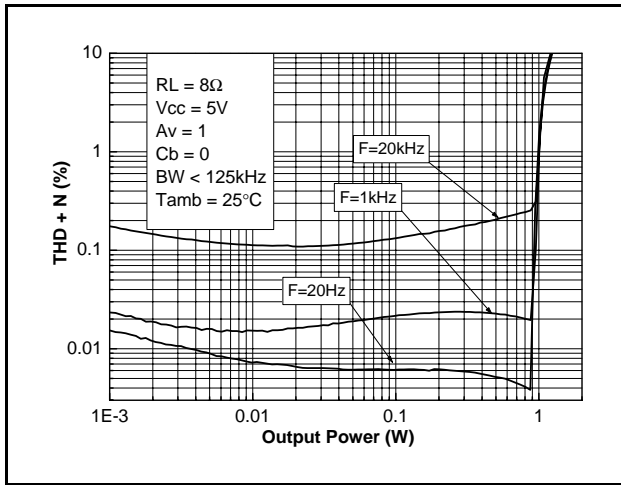


Figure 62: THD+N vs. output power

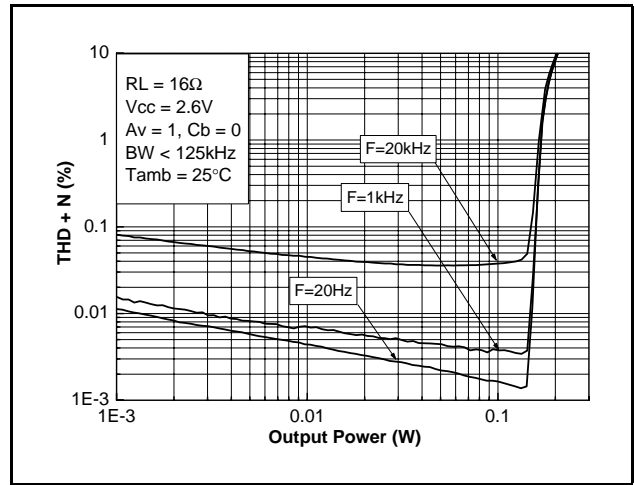


Figure 60: THD+N vs. output power

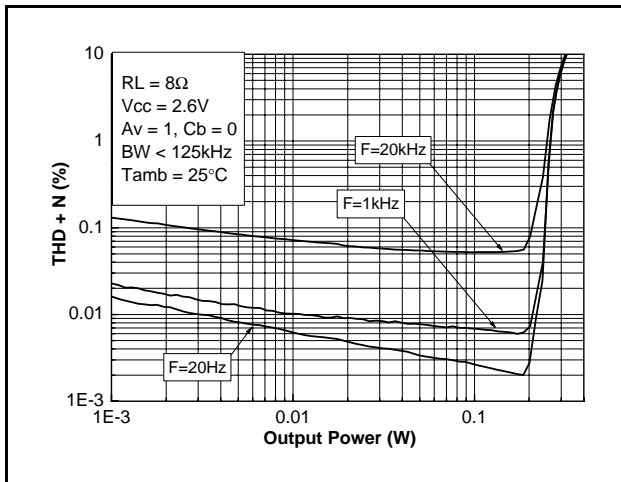


Figure 63: THD+N vs. frequency

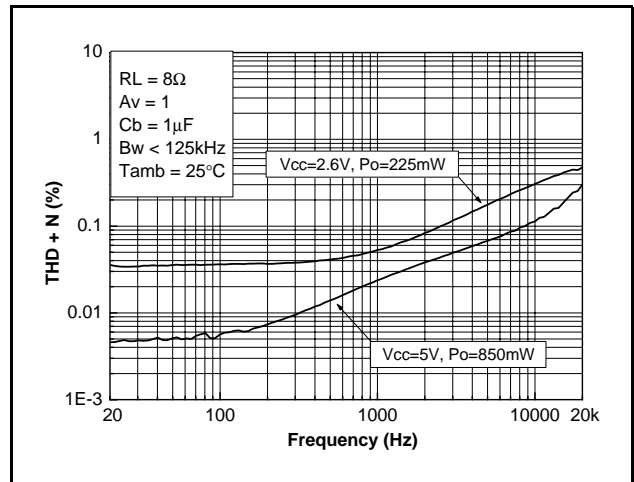


Figure 64: THD+N vs. frequency

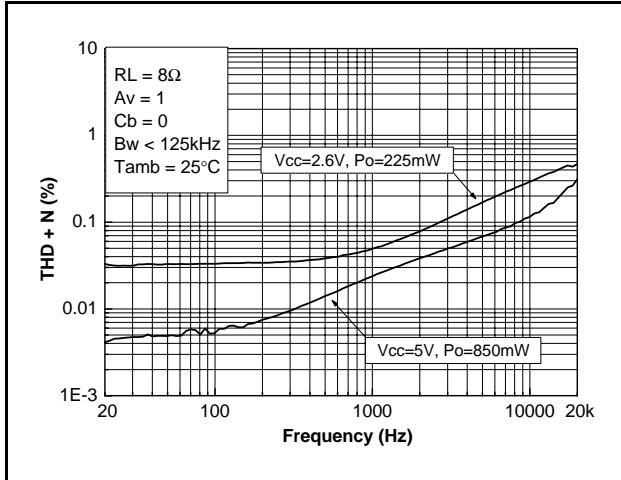


Figure 67: THD+N vs. frequency

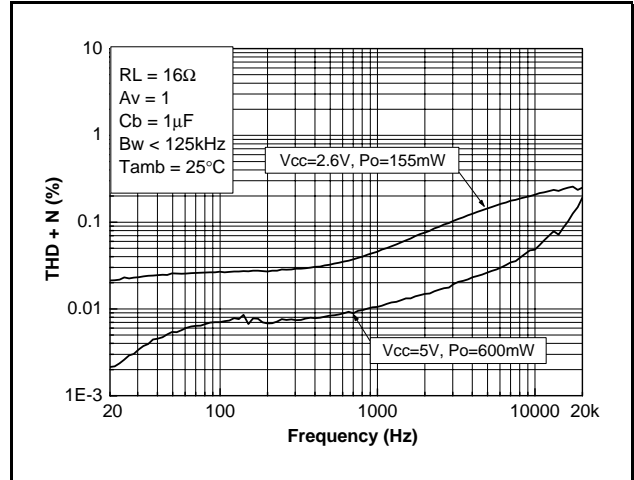


Figure 65: THD+N vs. frequency

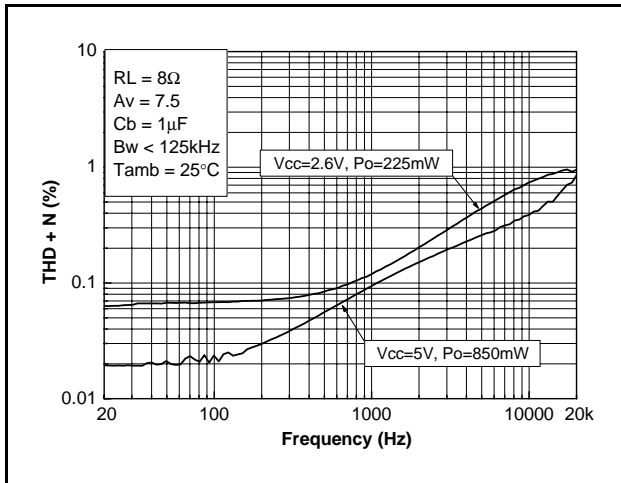


Figure 68: THD+N vs. frequency

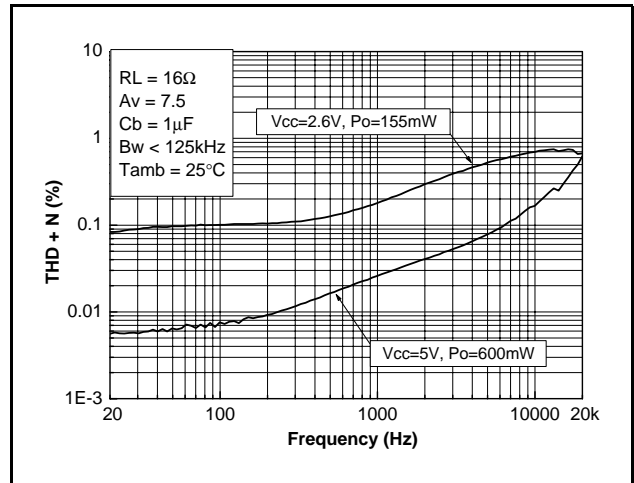


Figure 66: THD+N vs. frequency

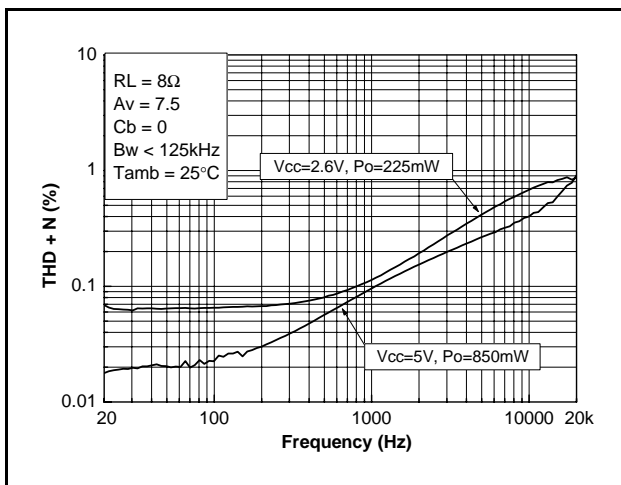


Figure 69: SNR vs. power supply voltage with unweighted filter

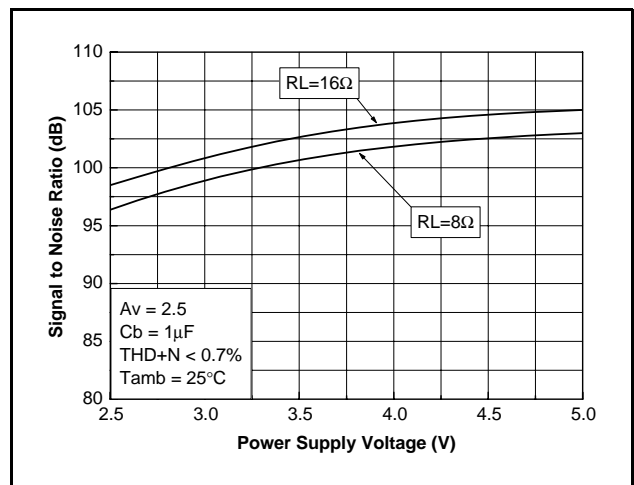


Figure 70: SNR vs. power supply voltage with a weighted filter

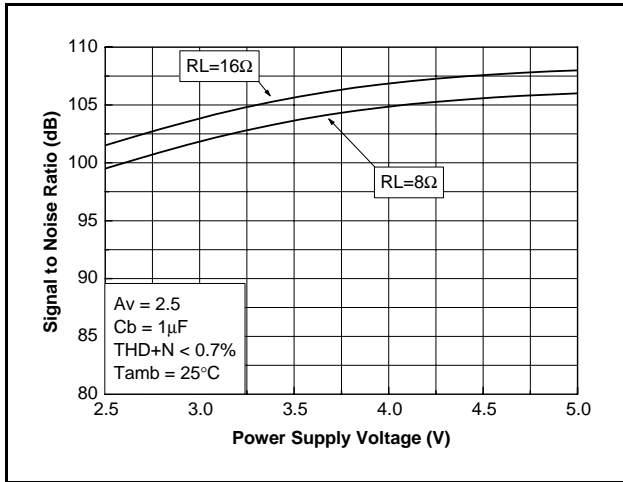
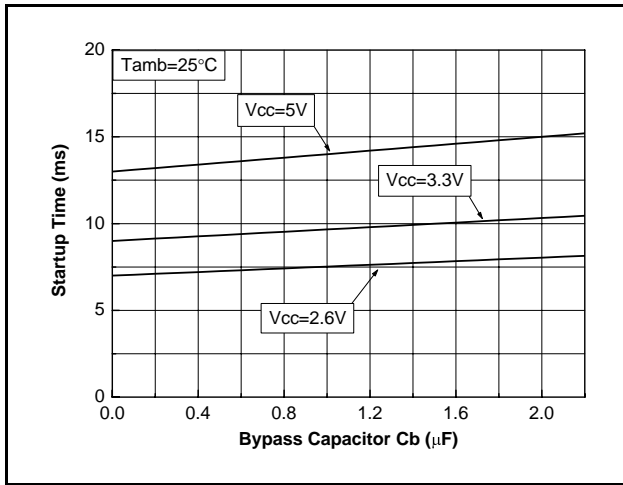


Figure 71: Startup time vs. bypass capacitor



## 4 Application Information

### 4.1 Differential Configuration Principle

The TS4994 is a monolithic full-differential input/output power amplifier. The TS4994 also includes a common mode feedback loop that controls the output bias value to average it at  $V_{CC}/2$  for any DC common mode input voltage. This allows the device to always have a maximum output voltage swing, and by consequence, maximize the output power. Moreover, as the load is connected differentially compared to a single-ended topology, the output is four times higher for the same power supply voltage.

The **advantages** of a full-differential amplifier are:

- Very high PSRR (Power Supply Rejection Ratio).
- High common mode noise rejection.
- Virtually zero pop without additional circuitry, giving an faster start-up time compared to

conventional single-ended input amplifiers.

- Easier interfacing with differential output audio DAC.
- No input coupling capacitors required thanks to common mode feedback loop.
- In theory, the filtering of the internal bias by an external bypass capacitor is not necessary. But, to reach maximal performances in all tolerance situations, it's better to keep this option.

The main **disadvantage** is:

- As the differential function is directly linked to external resistors mismatching, in order to reach maximal performances of the amplifier paying particular attention to this mismatching is mandatory.

### 4.2 Gain in typical application schematic

Typical differential applications are shown on the figures on [page 2](#).

In the flat region of the frequency-response curve (no  $C_{in}$  effect), the differential gain is expressed by the relation:

$$A_{V_{diff}} = \frac{V_{O+} - V_{O-}}{\text{Diff.}_{Input+} - \text{Diff.}_{Input-}} = \frac{R_{feed}}{R_{in}}$$

( $A_{V_{diff}}$  will be called  $A_v$  to simplify)

With  $R_{in} = R_{in1} = R_{in2}$  and  $R_{feed} = R_{feed1} = R_{feed2}$

### 4.3 Common mode feedback loop limitations.

As explained previously, the common mode feedback loop allows the output DC bias voltage to be averaged at  $V_{CC}/2$  for any DC common mode bias input voltage.

However, due to VICM limitation of the input stage (see [Electrical Characteristics](#) on page 5), the common mode feedback loop can ensure its role only within a defined range. This range depends upon the values of  $V_{CC}$ ,  $R_{in}$  and  $R_{feed}$  ( $A_v$ ). To have a good estimation of the VICM value, we can apply this formula:

$$V_{ICM} = \frac{V_{CC} \times R_{in} + 2 \times V_{IC} \times R_{feed}}{2 \times (R_{in} + R_{feed})} \quad (V)$$

with

$$V_{IC} = \frac{\text{Diff.}_{Input+} + \text{Diff.}_{Input-}}{2} \quad (V)$$

and the result of the calculation must be in the range:

$$0.6V \leq V_{ICM} \leq V_{CC} - 0.9V$$

If the result of VICM calculation is not in the previous range, an input coupling capacitor must be used.

**Example:** With  $V_{CC}=2.5V$ ,  $R_{in}=R_{feed}=20k$  and  $V_{IC}=2V$ , we found  $V_{ICM}=1.63V$ . This is higher than  $2.5V-0.9V=1.6V$ , so input coupling capacitors are required or you will have to change the  $V_{IC}$  value.

#### 4.4 Low and high frequency response

In the low frequency region,  $C_{in}$  starts to have an effect.  $C_{in}$  forms, with  $R_{in}$ , a high-pass filter with a -3dB cut-off frequency.  $F_{CL}$  is in Hz.

$$F_{CL} = \frac{1}{2 \times \pi \times R_{in} \times C_{in}} \quad (\text{Hz})$$

In the high-frequency region, you can limit the bandwidth by adding a capacitor ( $C_{feed}$ ) in parallel with  $R_{feed}$ . It forms a low-pass filter with a -3dB cut-off frequency.  $F_{CH}$  is in Hz.

$$F_{CH} = \frac{1}{2 \times \pi \times R_{feed} \times C_{feed}} \quad (\text{Hz})$$

While these bandwidth limitations are in theory attractive, in practice, because of low performance in terms of capacitor precision (and by consequence in terms of mismatching), they deteriorate the values of PSRR and CMRR.

We will discuss the influence of mismatching on PSRR and CMRR performance in more detail in the following paragraphs.

**Example:** A typical application with input coupling and feedback capacitor with  $F_{CL}=50\text{Hz}$  and  $F_{CH}=8\text{kHz}$ . We assume that the mismatching

#### 4.5 Calculating the influence of mismatching

##### On PSRR performance:

For this calculation, we consider that  $C_{in}$  and  $C_{feed}$  have no influence.

We use the same kind of resistor (same tolerance) and  $\Delta R$  is the tolerance value in %.

The following equation is valid for frequencies ranging from DC to about 1kHz. Above this frequency, parasitic effects start to be significant and a literal equation is not possible to write.

The PSRR equation is ( $\Delta R$  in %):

$$PSRR \leq 20 \times \text{Log} \left[ \frac{\Delta R \times 100}{(10000 - \Delta R^2)} \right] \quad (\text{dB})$$

This equation doesn't include the additional performance provided by bypass capacitor filtering. If a bypass capacitor is added, it acts, together with the internal high output impedance bias, as a low-pass filter, and the result is a quite

between  $R_{in1,2}$  and  $C_{feed1,2}$  can be neglected. If we sweep the frequency from DC to 20kHz we observe the following with respect to the PSRR value:

- From DC to 200Hz,  $C_{in}$  impedance decreases from infinite to a finite value and the  $C_{feed}$  impedance is high enough to be neglected. Due to the tolerance of  $C_{in1,2}$ , we must introduce a mismatch ( $R_{in1} \times C_{in1} \neq R_{in2} \times C_{in2}$ ) that will decrease the PSRR performance.
- From 200Hz to 5kHz,  $C_{in}$  impedance is low enough to be neglected compare to  $R_{in}$  and  $C_{feed}$  impedance is high enough to be also neglected. In this range, we can reach the PSRR performance of the TS4994 itself.
- From 5kHz to 20kHz,  $C_{in}$  impedance is low to be neglected compare to  $R_{in}$  and  $C_{feed}$  impedance decreases to a finite value. Due to tolerance of  $C_{feed1,2}$ , we introduce a mismatching ( $R_{feed1} \times C_{feed1} \neq R_{feed2} \times C_{feed2}$ ) that will decrease the PSRR performance.

important PSRR improvement with a relatively small bypass capacitor.

The complete PSRR equation ( $\Delta R$  in %,  $C_b$  in microFarad and  $F$  in Hz) is:

$$PSRR \leq 20 \times \text{Log} \left[ \frac{\Delta R \times 100}{(10000 - \Delta R^2) \times \sqrt{1 + F^2 \times C_b^2 \times 22.2}} \right] \quad (\text{dB})$$

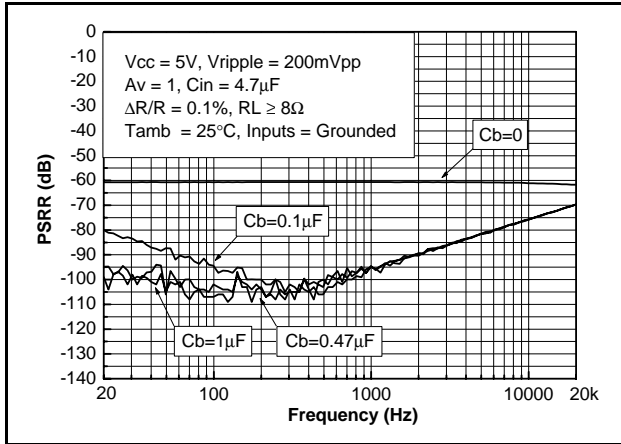
**Example:** With  $\Delta R=0.1\%$  and  $C_b=0$ , the minimum PSRR would be -60dB. With a 100nF bypass capacitor, at 100Hz the new PSRR would be -93dB.

This example is a worst case scenario, where each resistor has extreme tolerance and illustrates the fact that with only a small bypass capacitor, the TS4994 produce high PSRR performance.

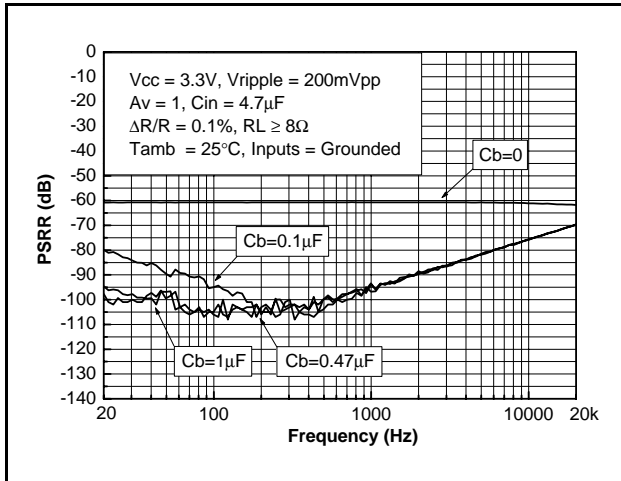
In addition, it's important to note that this is a theoretical formula. As the TS4994 has self-generated noise, you should consider that the highest practical PSRR reachable is about -110dB. It is therefore unreasonable to target a -120dB PSRR.

The three following graphs show PSRR versus frequency and versus bypass capacitor  $C_b$  in worst-case condition ( $\Delta R=0.1\%$ ).

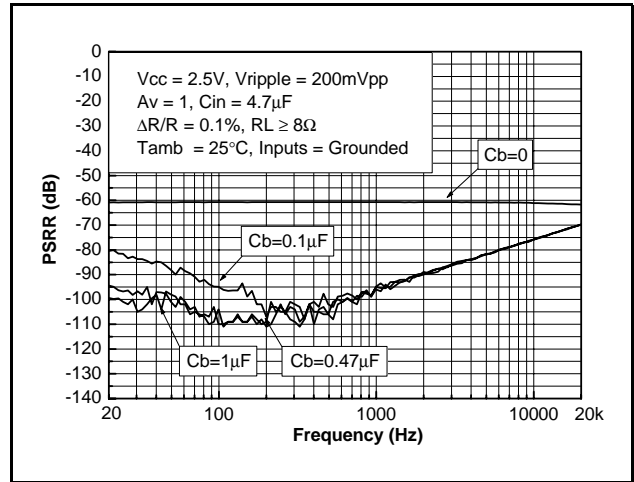
**Figure 72: PSRR vs. frequency worst case condition**



**Figure 73: PSRR vs. frequency worst case condition**

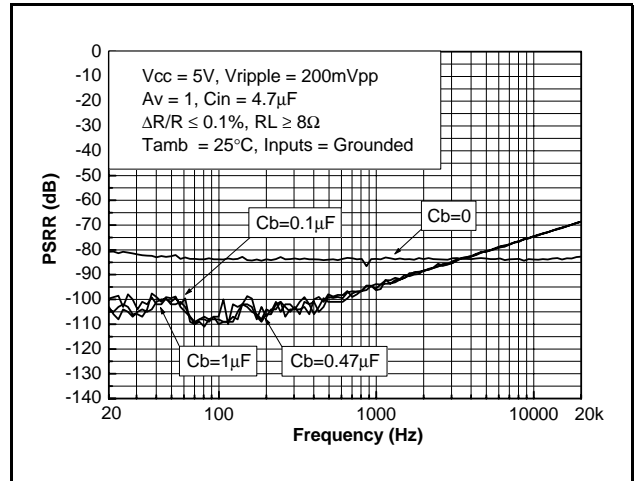


**Figure 74: PSRR vs. frequency worst case condition**

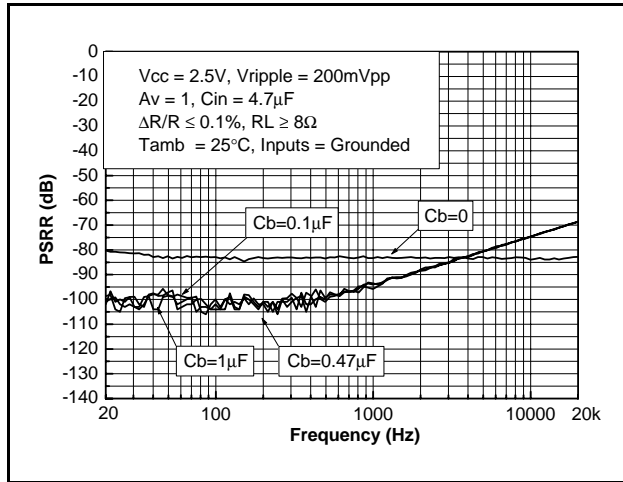


The two following graphs show typical application of TS4994 with four 0.1% tolerances and a random choice for them.

**Figure 75: PSRR vs. frequency with random choice condition**



**Figure 76: PSRR vs. frequency with random choice condition**



**CMRR performance**

For this calculation, we consider there to be no influence of  $C_{in}$  and  $C_{feed}$ .  $C_b$  has no influence in the calculation of the CMRR.

We use the same kind of resistor (same tolerance) and  $\Delta R$  is the tolerance value in %.

The following equation is valid for frequencies ranging from DC to about 1kHz. Above this frequency, parasitic effects start to be significant and a literal equation is not possible to write.

The CMRR equation is ( $\Delta R$  in %):

$$CMRR \leq 20 \times \text{Log} \left[ \frac{\Delta R \times 200}{(10000 - \Delta R^2)} \right] \text{ (dB)}$$

**Example:** With  $\Delta R=1\%$ , the minimum CMRR would be -34dB.

With a DC  $V_{ic}=2.5V$ , the DC differential output ( $V_{oo}$ ) which results is 50mV maximum. As this  $V_{oo}$  is across the load, for an  $8\Omega$  load the extra consumption would be  $50mV/8=6.2mA$ .

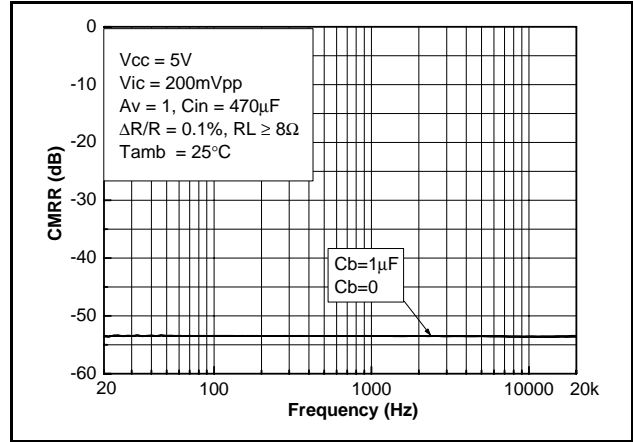
With  $\Delta R=1\%$ , the minimum CMRR would be -53dB that give  $V_{oo}=5.6mV$  and an maximum extra consumption less than  $700\mu A$ .

This example is of a worst case scenario where each resistor has extreme tolerance and illustrates the fact that for CMRR, good matching is essential.

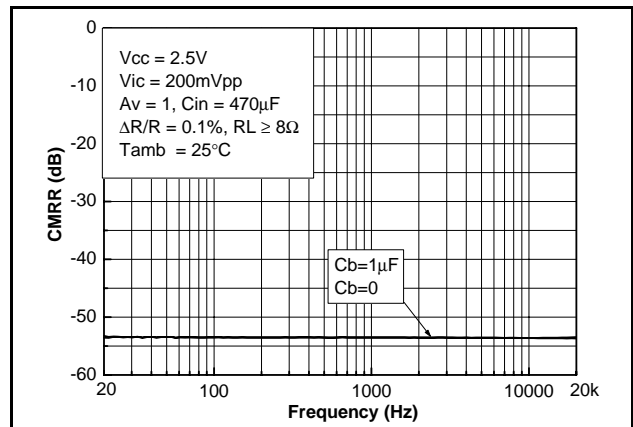
As with the PSRR, due to self-generated noise, the TS4994 CMRR limitation would be about -110dB.

Figures 77 and 78 show CMRR versus frequency and versus bypass capacitor  $C_b$  in worst-case condition ( $\Delta R=0.1\%$ ).

**Figure 77: CMRR vs. frequency worst case condition**

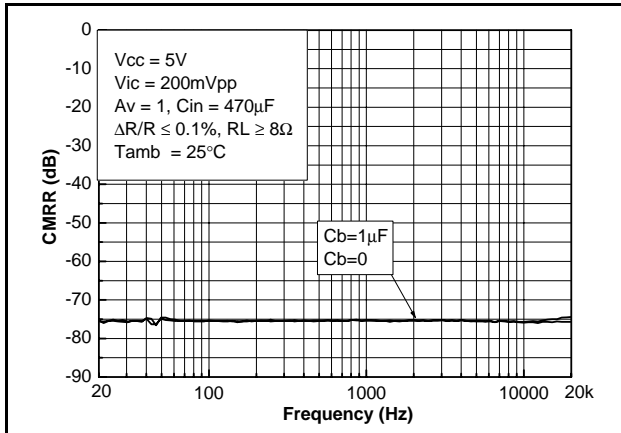


**Figure 78: CMRR vs. frequency worst case condition**

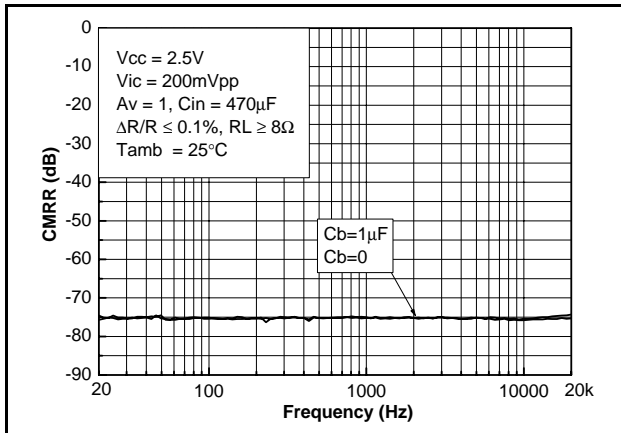


Figures 79 and 80 show CMRR versus frequency for a typical application with four 0.1% tolerances and a random choice for them.

**Figure 79: CMRR vs. frequency with random choice condition**



**Figure 80: CMRR vs. frequency with random choice condition**





## 4.6 Power dissipation and efficiency

### Assumptions:

- Load voltage and current are sinusoidal ( $V_{out}$  and  $I_{out}$ )
- Supply voltage is a pure DC source ( $V_{CC}$ )

Regarding the load we have:

$$V_{out} = V_{PEAK} \sin \omega t \text{ (V)}$$

and

$$I_{out} = \frac{V_{out}}{R_L} \text{ (A)}$$

and

$$P_{out} = \frac{V_{PEAK}^2}{2R_L} \text{ (W)}$$

Therefore, the average current delivered by the supply voltage is:

$$I_{CC\text{AVG}} = 2 \frac{V_{PEAK}}{\pi R_L} \text{ (A)}$$

The power delivered by the supply voltage is:

$$P_{supply} = V_{CC} I_{CC\text{AVG}} \text{ (W)}$$

Then, the **power dissipated by each amplifier** is  $P_{diss} = P_{supply} - P_{out}$  (W)

$$P_{diss} = \frac{2\sqrt{2}V_{CC}}{\pi\sqrt{R_L}} \sqrt{P_{out}} - P_{out}$$

and the maximum value is obtained when:

$$\frac{\partial P_{diss}}{\partial P_{out}} = 0$$

## 4.7 Decoupling of the circuit

Two capacitors are needed to correctly bypass the TS4994. A power supply bypass capacitor  $C_S$  and a bias voltage bypass capacitor  $C_B$ .

$C_S$  has particular influence on the THD+N in the high frequency region (above 7kHz) and an indirect influence on power supply disturbances. With a value for  $C_S$  of 1 $\mu$ F, you can expect similar

and its value is:

$$P_{diss\max} = \frac{2V_{CC}^2}{\pi^2 R_L} \text{ (W)}$$

*Note: This maximum value is only dependent on power supply voltage and load values.*

The **efficiency** is the ratio between the output power and the power supply

$$\eta = \frac{P_{out}}{P_{supply}} = \frac{\pi V_{PEAK}}{4V_{CC}}$$

The maximum theoretical value is reached when  $V_{peak} = V_{CC}$ , so

$$\frac{\pi}{4} = 78.5\%$$

The maximum die temperature allowable for the TS4994 is 125°C. However, in case of overheating, a thermal shutdown set to 150°C, puts the TS4994 in standby until the temperature of the die is reduced by about 5°C.

To calculate the maximum ambient temperature  $T_{AMB}$  allowable, we need to know:

- Power supply Voltage value,  $V_{CC}$
- Load resistor value,  $R_L$
- The package type,  $R_{THJA}$

**Example:**  $V_{CC}=5V$ ,  $R_L=8\Omega$ ,  $R_{THJA}\text{Flip-Chip}=100^\circ\text{C/W}$  (100mm<sup>2</sup> copper heatsink).

We calculate  $P_{diss\max} = 633\text{mW}$ .

With

$$T_{AMB} = 125^\circ\text{C} - R_{THJA} \times P_{diss} \text{ (}^\circ\text{C)}$$

$$T_{AMB} = 125 - 100 \times 0.633 = 61.7^\circ\text{C}$$

THD+N performances to those shown in the datasheet.

In the high frequency region, if  $C_S$  is lower than 1 $\mu$ F, it increases THD+N and disturbances on the power supply rail are less filtered.

On the other hand, if  $C_S$  is higher than 1 $\mu$ F, those disturbances on the power supply rail are more filtered.

$C_b$  has an influence on THD+N at lower frequencies, but its function is critical to the final

#### 4.8 Wake-up Time: $T_{WU}$

When the standby is released to put the device ON, the bypass capacitor  $C_b$  will not be charged immediately. As  $C_b$  is directly linked to the bias of the amplifier, the bias will not work properly until the  $C_b$  voltage is correct. The time to reach this voltage is called the wake-up time or  $T_{WU}$  and is specified in the tables found in [Electrical Characteristics](#) on page 5, with  $C_b=1\mu\text{F}$ . During

#### 4.9 Shutdown time

When the standby command is set, the time required to put the two output stages in high impedance and the internal circuitry in shutdown mode is a few microseconds.

#### 4.10 Pop performance

In theory, due to a fully differential structure, the pop performance of the TS4994 should be perfect. However, due to  $R_{in}$ ,  $R_{feed}$ , and  $C_{in}$  mismatching, some noise could remain at startup. In TS4994 we included a pop reduction circuitry reach the pop that is theoretical with mismatched components. With this circuitry, the TS4994 is

#### 4.11 Single ended input configuration

It's possible to use the TS4994 in a single-ended input configuration. However, an input coupling capacitor is needed in this configuration. The schematic in [Figure 81](#) shows this configuration using the miniSO8 version of the TS4994 as example.

result of PSRR (with input grounded and in the lower frequency region).

the wake-up time phase, the TS4994 gain is close to zero. After the wake-up time period, the gain is released and set to its nominal value.

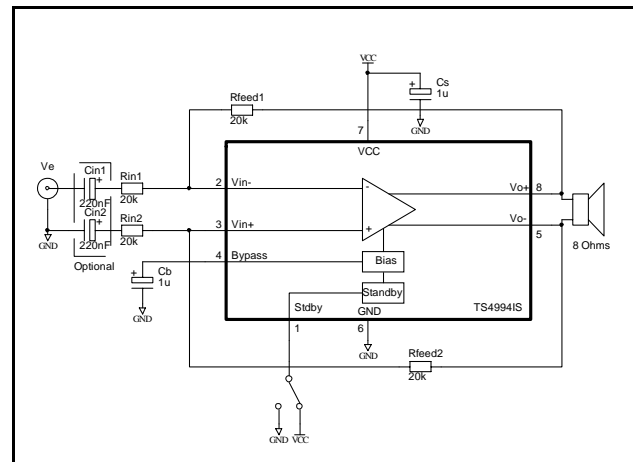
If  $C_b$  has a value other than  $1\mu\text{F}$ , please refer to the graph in [Figure 71](#) to establish the wake-up time value.

*Note: In shutdown mode, Bypass pin and  $V_{in+}$ ,  $V_{in-}$  pins are short-circuited to ground by internal switches. This allows a quick discharge of  $C_b$  and  $C_{in}$  capacitors.*

close to zero pop for all common applications possible.

In addition, when the TS4994 is set in standby, due to the high impedance output stage configuration in this mode, no pop is possible.

**Figure 81: Single ended input typical application**



The components calculations remain the same except for the gain. The new formula is:

$$A_{VSE} = \frac{V_{O+} - V_{O-}}{V_e} = \frac{R_{feed}}{R_{in}}$$

### 4.12 Demoboard

A demoboard for the TS4994 is available, however it is designed only for the TS4994 in the DFN10 package. However, we can guarantee that

all electrical parameters are similar except for the power dissipation.

For more information about this demoboard, please refer to **Application Note AN2013**.

Figure 82: Demoboard schematic

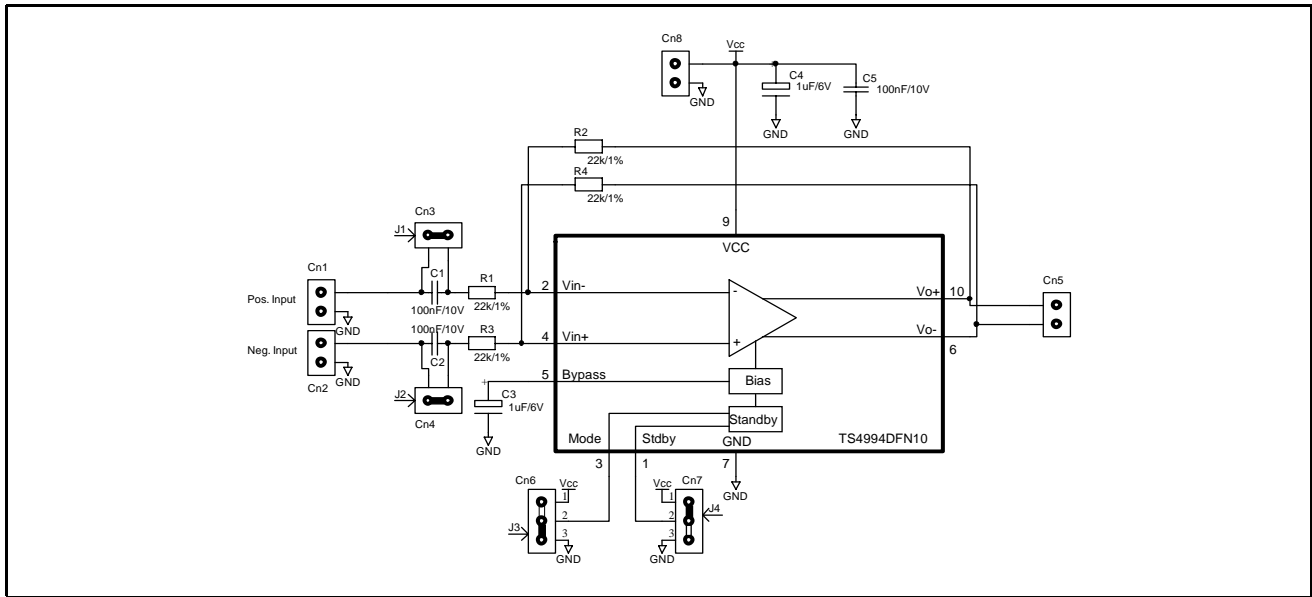


Figure 83: Components location

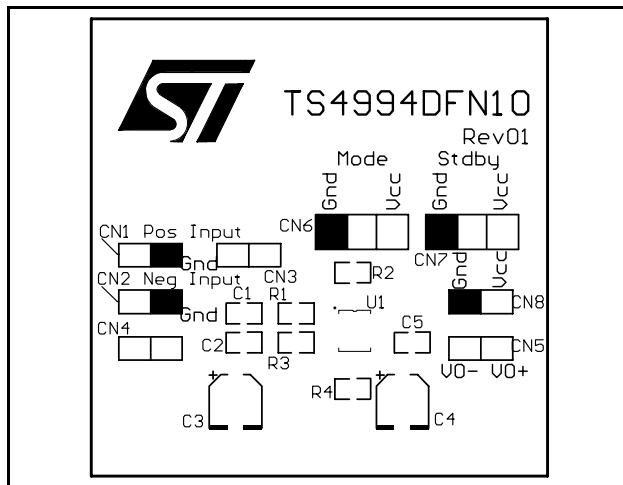


Figure 84: Top layer

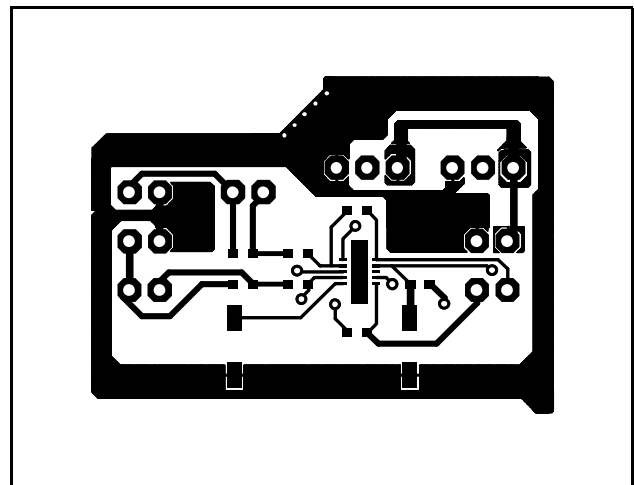
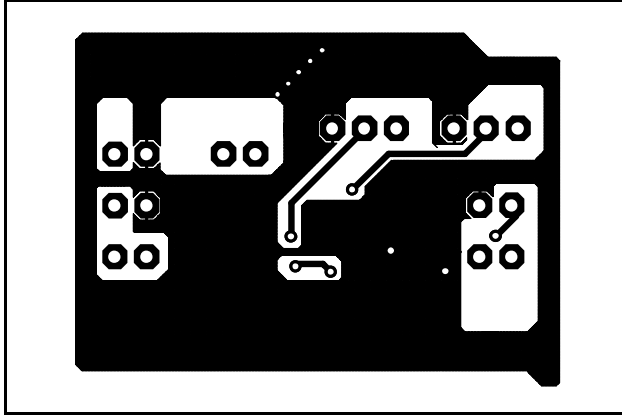


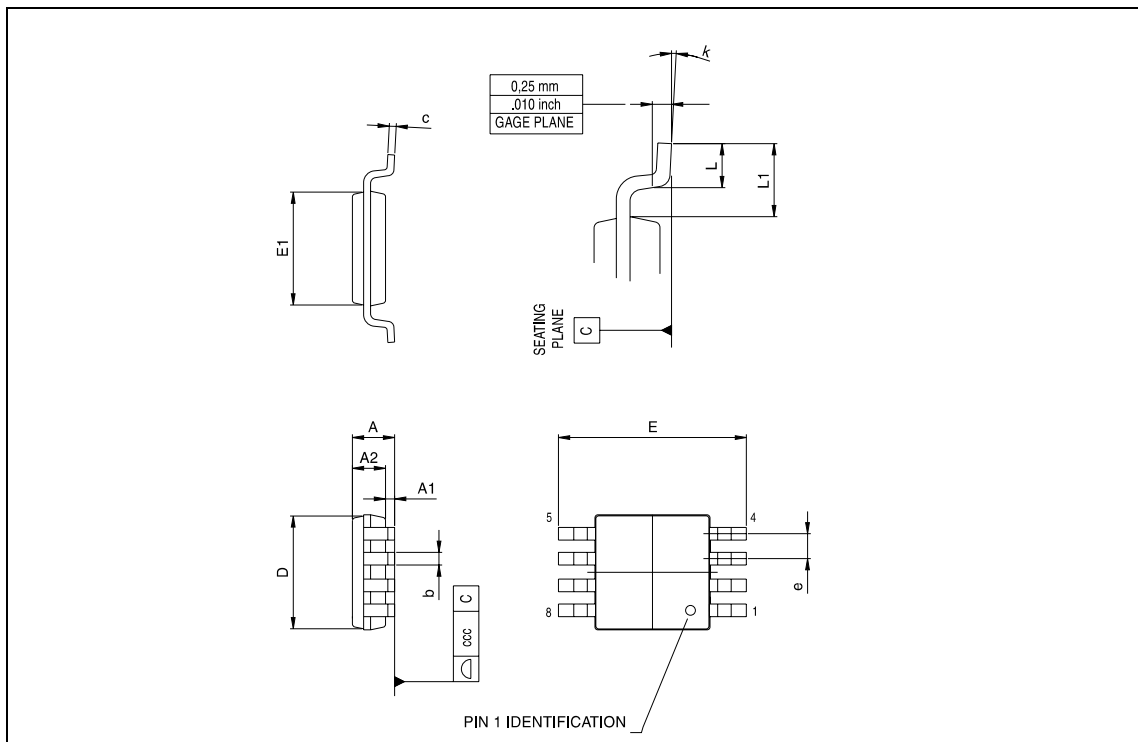
Figure 85: Bottom layer



## 5 Package Mechanical Data

### 5.1 MiniSO8 package

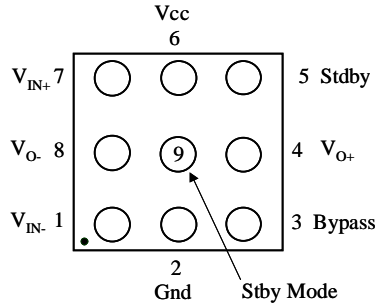
miniSO-8 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.043
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.78	0.86	0.94	0.031	0.031	0.037
b	0.25	0.33	0.40	0.010	0.13	0.013
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.75	4.90	5.05	0.187	0.193	0.199
E1	2.90	3.00	3.10	.0114	0.118	0.122
e		0.65			0.026	
K	0°		6°	0°		6°
L	0.40	0.55	0.70	0.016	0.022	0.028
L1			0.10			0.004



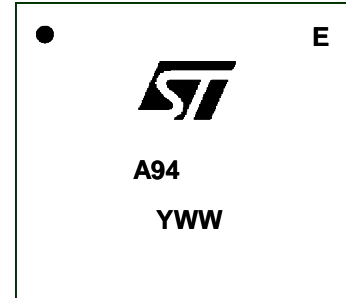
### 5.2 Flip-chip package (9 bumps)

Dimensions in millimeters unless otherwise indicated.

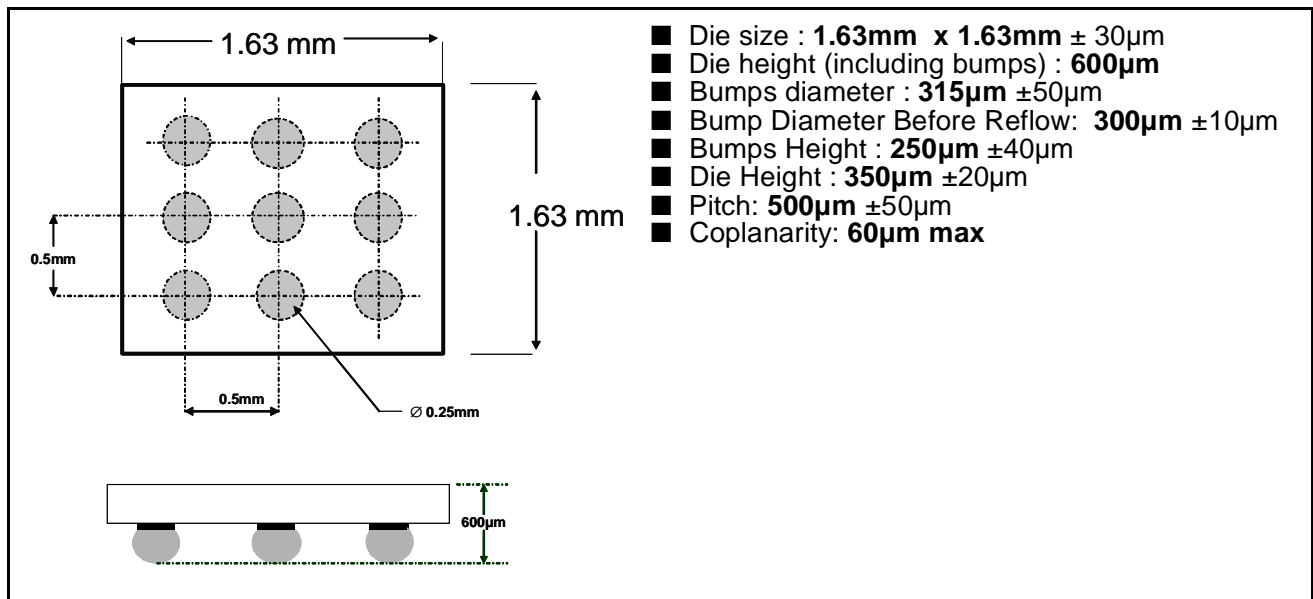
#### PIN OUT (top view)



#### MARKING (top view)

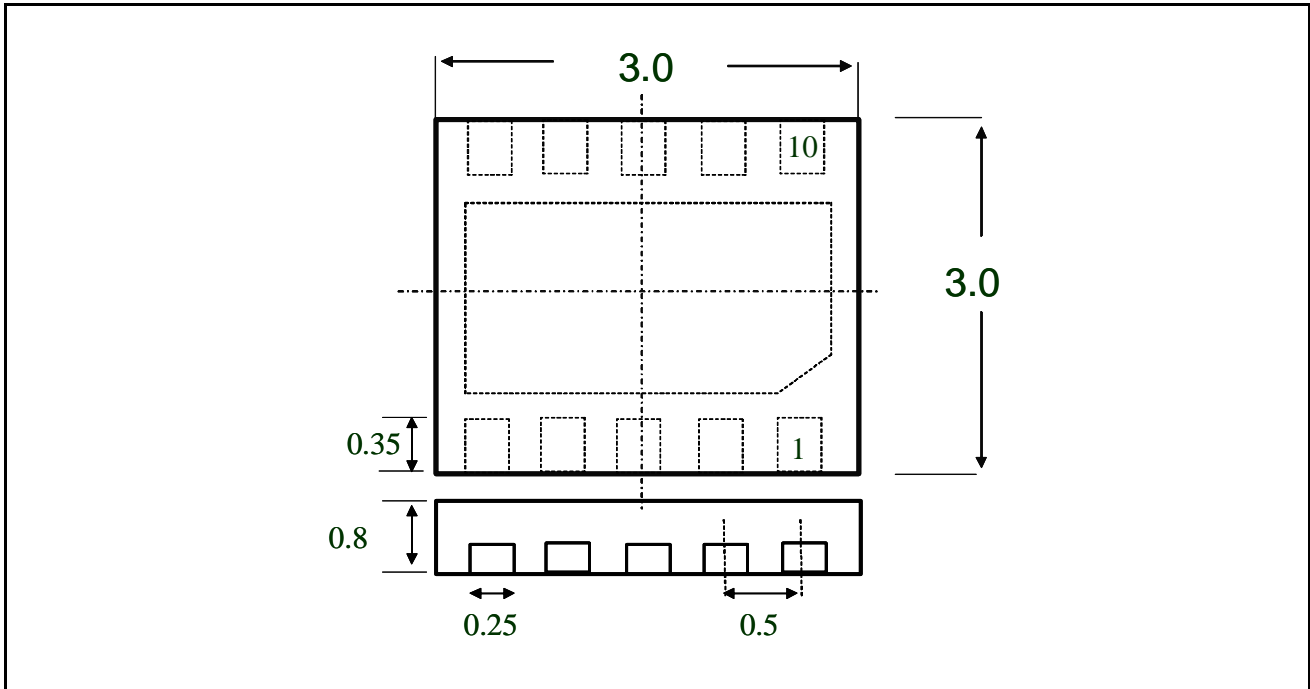


■ Balls are underneath



### 5.3 DFN10 package

Dimensions in millimeters unless otherwise indicated.



## 6 Revision History

Date	Revision	Description of Changes
01 August 2004	1	First Release

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