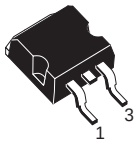
STB10NB20

N-CHANNEL 200V - 0.30Ω - 10A D²PAK
PowerMESH™ MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STB10NB20	200 V	<0.40 Ω	10 A

- TYPICAL RDS(on) = 0.30 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED
- FOR THROUGH-HOLE VERSION CONTACT SALES OFFICE



D²PAK
TO-263
(suffix"T4")

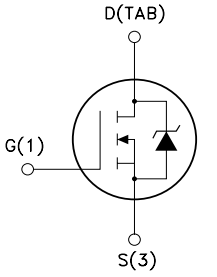
DESCRIPTION

Using the latest high voltage MESH OVERLAY™ process, STMicroelectronis has designed an advanced family of power MOSFETs with outstanding performances. The new patent pending strip layout coupled with the Company's proprietary edge termination structure, gives the lowest RDS(on) per area, exceptional avalanche and dv/dt capabilities and unrivalled gate charge and switching characteristics.

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SWITCH MODE POWER SUPPLIES (SMPS)
- DC-AC CONVERTERS FOR WELDING EQUIPMENT AND UNINTERRUPTIBLE POWER SUPPLIES AND MOTOR DRIVE

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	200	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	200	V
V_{GS}	Gate- source Voltage	±30	V
I_D	Drain Current (continuos) at T_C = 25°C	10	A
I_D	Drain Current (continuos) at T_C = 100°C	6	A
I_{DM}(•)	Drain Current (pulsed)	40	A
P_{tot}	Total Dissipation at T_C = 25°C	85	W
	Derating Factor	0.68	W/°C
dv/dt (2)	Peak Diode Recovery voltage slope	5.5	V/ns
T_{stg}	Storage Temperature	–65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

(•)Pulse width limited by safe operating area.

(2) I_{SD} ≤10A, di/dt ≤300A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_j ≤ $T_{JMAX.}$

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	1.47	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	62.5	°C/W
$R_{thc\text{-}sink}$	Thermal Resistance Case-sink	Typ	0.5	°C/W
T_j	Maximum Lead Temperature For Soldering Purpose		300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	10	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V)	150	mJ

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA V_{GS} = 0	200			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating T_C = 125 °C			1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ±30 V			±100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ I_D = 250 µA	3	4	5	V
$I_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V I_D = 5 A		0.30	0.40	Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ V_{GS} = 10 V	10			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ I_D=5 A	3	4		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitances	V_{DS} = 25V f = 1 MHz V_{GS} = 0		470 135 22	650 190 30	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 100 V I_D = 5 A R_G = 4.7 Ω V_{GS} = 10 V (see test circuit, Figure 3)		10 15	14 20	ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD}=160V I_D=10A V_{GS}=10V		17 7.5 5.5	24	nC nC nC

SWITCHING OFF

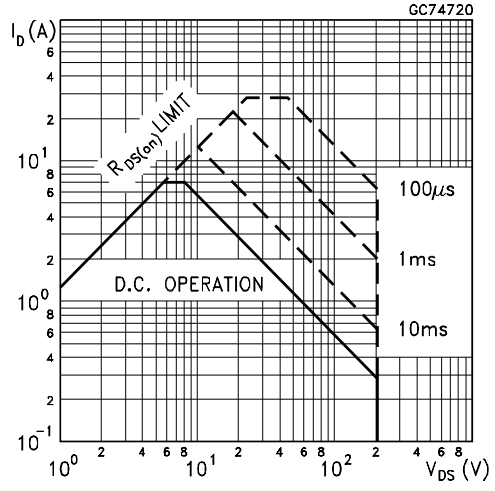
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$ t_r t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{DD} = 160 V I_D = 10 A R_G = 4.7 Ω V_{GS} = 10 V (see test circuit, Figure 5)		8 10 20	11 14 28	ns ns ns

SOURCE DRAIN DIODE

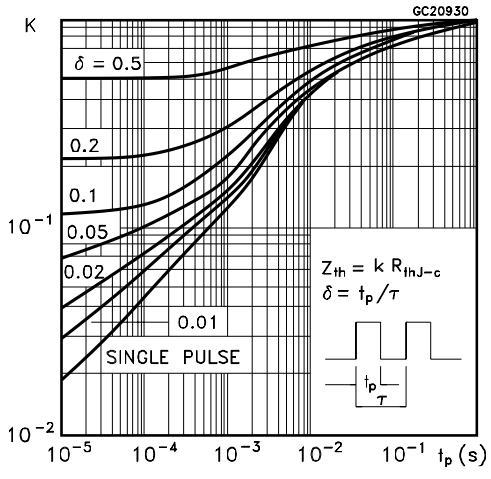
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (•)	Source-drain Current Source-drain Current (pulsed)				10 40	A A
V_{SD} (*)	Forward On Voltage	I_{SD} = 10 A V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 10 A di/dt = 100 A/µs V_{DD} = 50 V T_j = 150 °C (see test circuit, Figure 5)		170 980 11.5		ns nC A

(*)Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
(•)Pulse width limited by safe operating area.

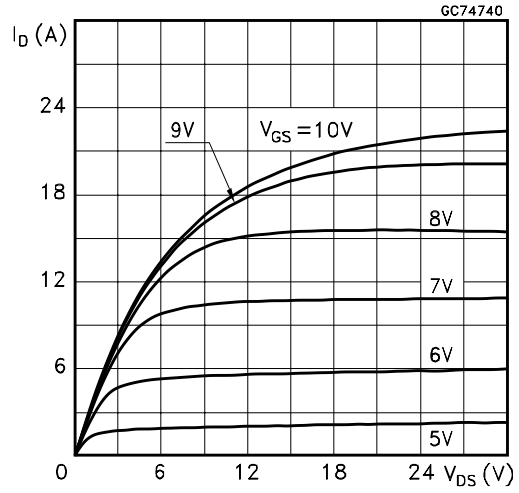
Safe Operating Area



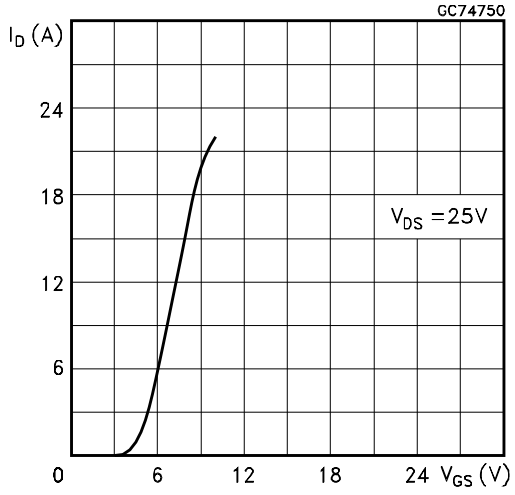
Thermal Impedance



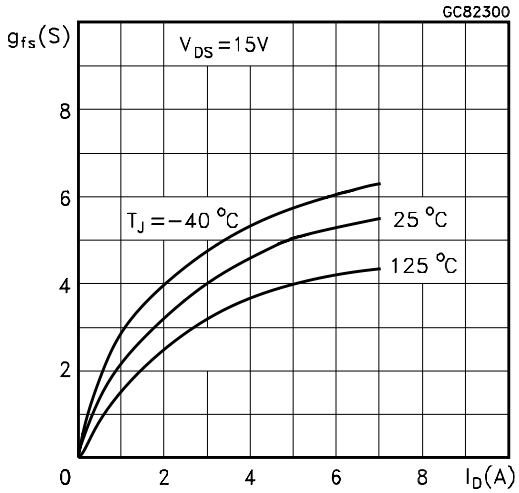
Output Characteristics



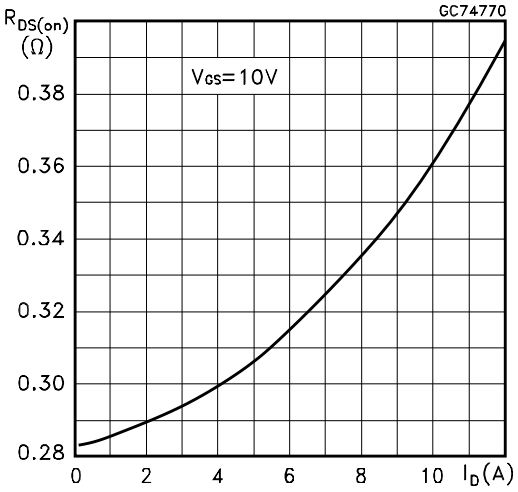
Transfer Characteristics



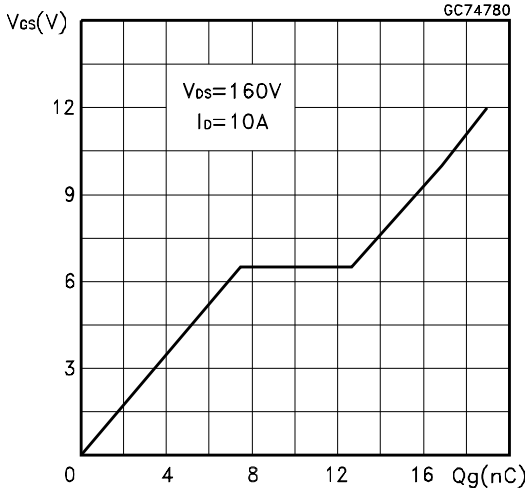
Transconductance



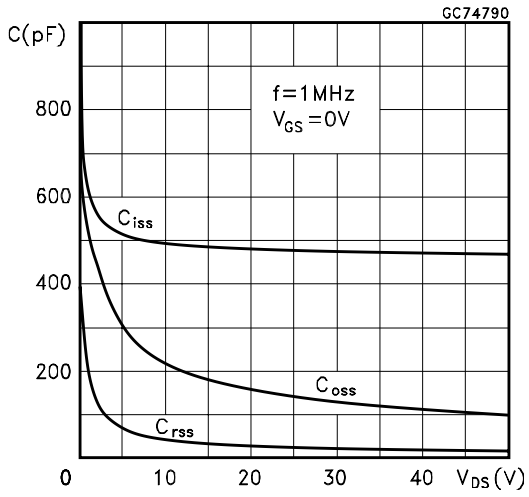
Static Drain-source On Resistance



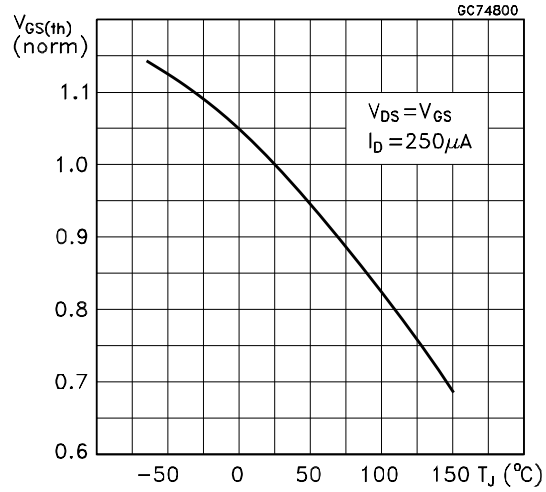
Gate Charge vs Gate-source Voltage



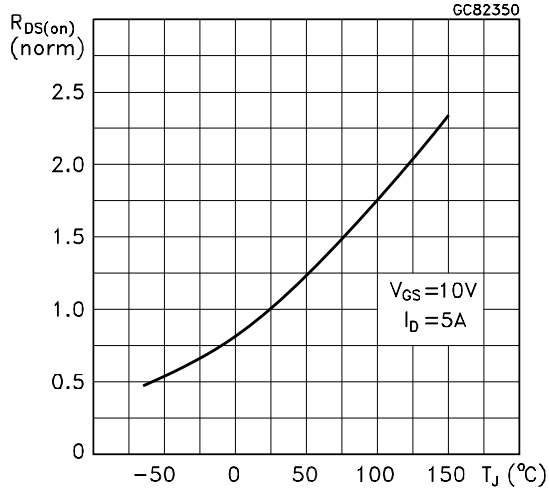
Capacitance Variations



Normalized Gate Threshold Voltage vs Temperature



Normalized Gate Threshold Voltage vs Temperature



Source-drain Diode Forward Characteristics

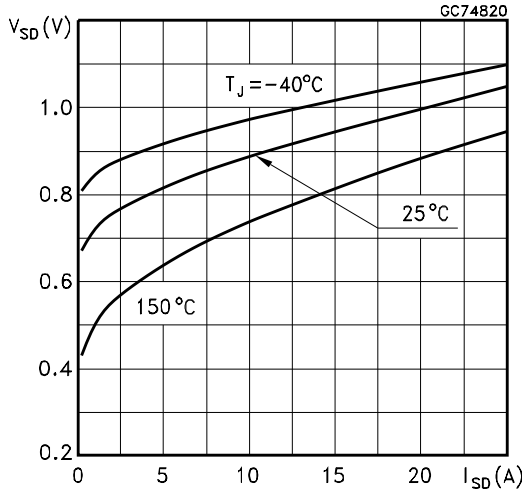


Fig. 1: Unclamped Inductive Load Test Circuit

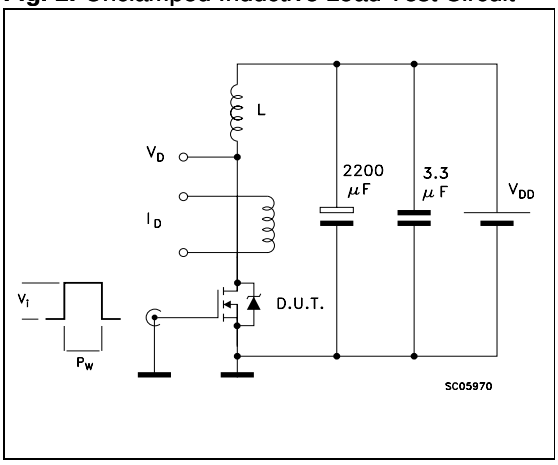


Fig. 2: Unclamped Inductive Waveform

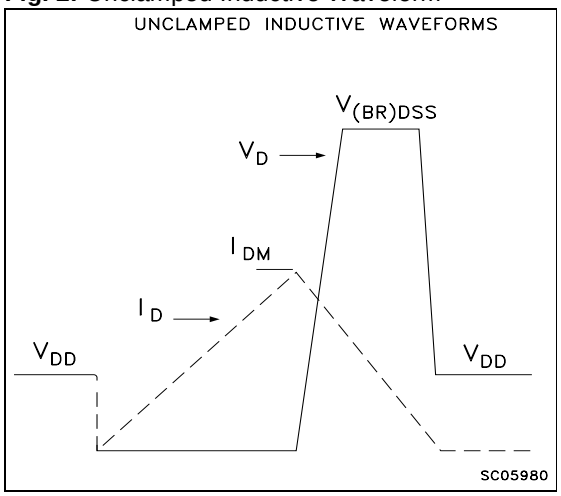


Fig. 3: Switching Times Test Circuits For Resistive Load

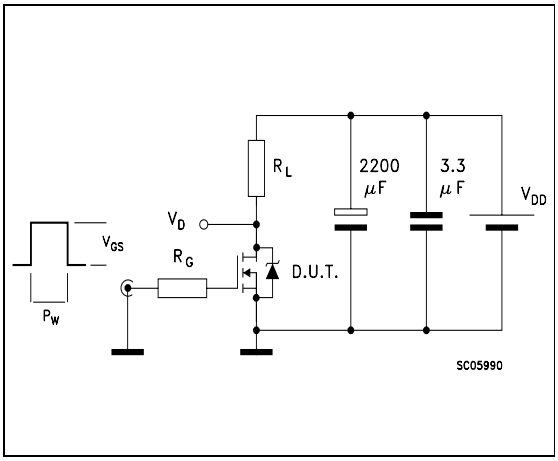


Fig. 4: Gate Charge test Circuit

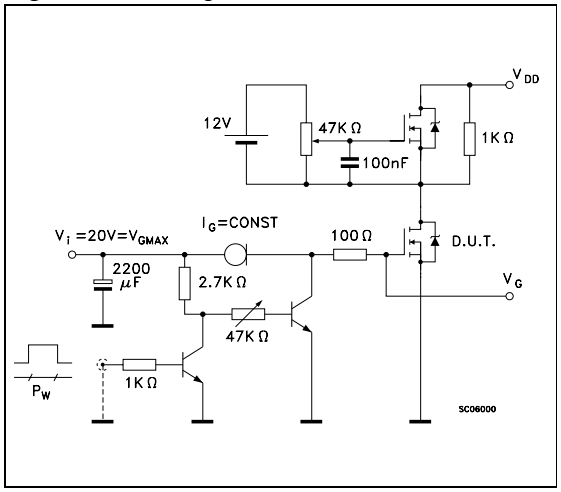
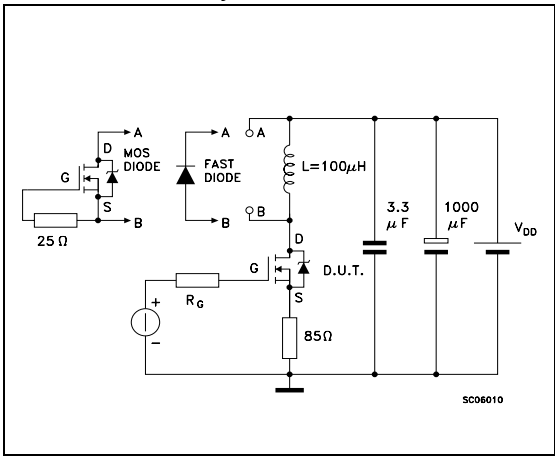


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		8°