DM114、DM115

8-Bit CONSTANT CURRENT LED DRIVERS with

3.3v ~ 5v supply voltage

DM114、DM115

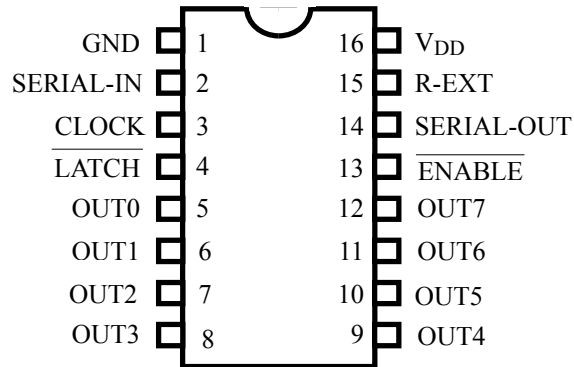# 8-Bit CONSTANT CURRENT LED DRIVERS with

3.3v ~ 5v Supply Voltage

General Description

The DM114、DM115 is the constant current driver specifically designed for LED display applications. The value of constant current can be varied using an external resistor. The devices include an 8-bit shift register, latches, and constant current drivers on a single Silicon CMOS chip.
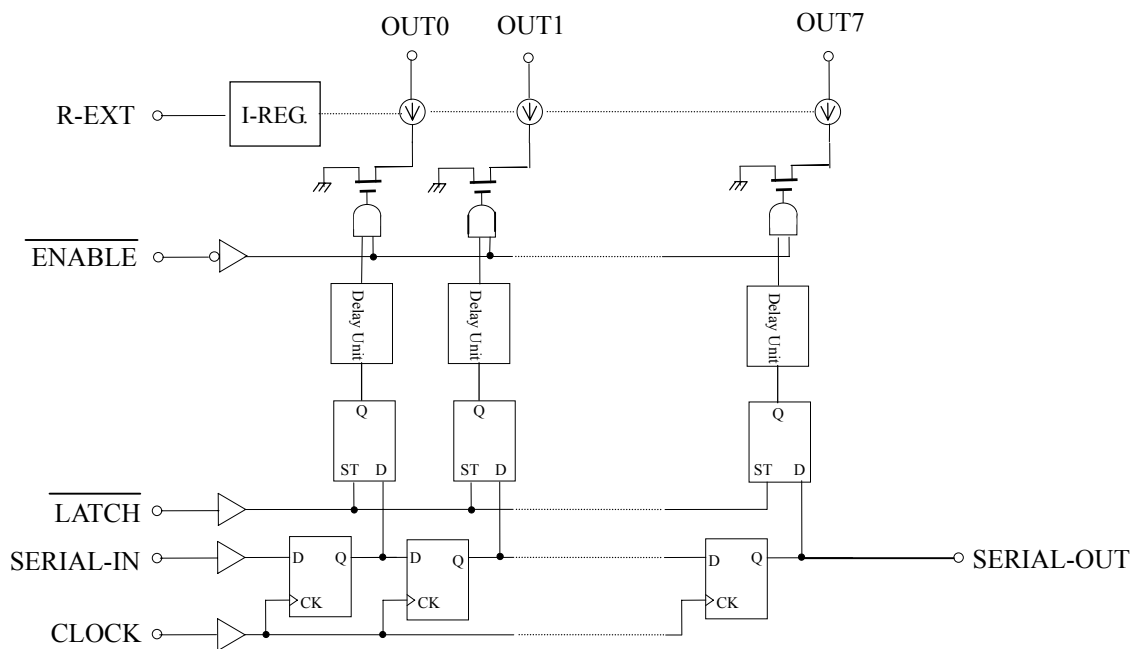
Features

- Maximum Output Voltage: 17V
- Maximum Clock Frequency: 25MHz (Cascade Operation)
- Power Supply Voltage: 3.3V to 5.0V
- CMOS Compatible Input
- Package: PDIP16, SOP16, SSOP16
- Package and Pin Layout: Pin layout and functionality are similar to those of the ST2221A. (Each characteristic value is different.)
- Constant Current Matching: (Ta = 25°C、V_{DD} = 5.0V)

    Chip-to-Chip: ± 10.0%

    DM114: Bit-to-Bit: ± 4.0% @ I_{OUT} = 30 ~ 90mA

    ± 6.0% @ I_{OUT} = 20 ~ 30mA

    DM115: Bit-to-Bit: ± 4.0% @ I_{OUT} = 20 ~ 60mA

    ± 6.0% @ I_{OUT} = 5 ~ 20mA

Preliminary

Pin Connection (Top view)

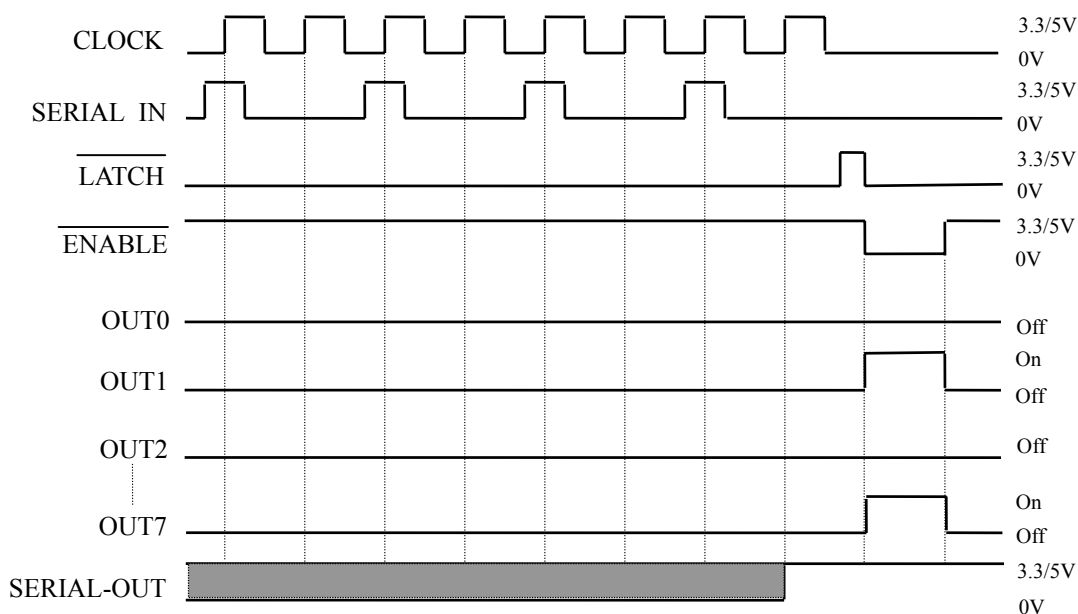|			
GND	1	16	V_{DD}
SERIAL-IN	2	15	R-EXT
CLOCK	3	14	SERIAL-OUT
$\overline{\text{LATCH}}$	4	13	$\overline{\text{ENABLE}}$
OUT0	5	12	OUT7
OUT1	6	11	OUT6
OUT2	7	10	OUT5
OUT3	8	9	OUT4

Block Diagram

Preliminary

Timing Diagram

(Note) Latches are level sensitive (not edge triggered).

$\overline{\text{LATCH}}$-terminal = H level, latches become transparent; $\overline{\text{LATCH}}$-terminal = L level, latches hold data.

$\overline{\text{ENABLE}}$-terminal = H level, all outputs (OUT0~7) are off.

An external resistor is connected between R-EXT and GND for setting up the value of constant current.

SERIAL-OUT changes state on the rising edges of clock.

Pin Description

PIN No.	PIN NAME	FUNCTION
1	GND	GND terminal
2	SERIAL-IN	Input terminal of a data shift register
3	CLOCK	Input terminal of a clock for shift register
4	$\overline{\text{LATCH}}$	Input terminal for data strobe
5~12	OUT0~7	Output terminals
13	$\overline{\text{ENABLE}}$	Input terminal for output enable (active low)
14	SERIAL-OUT	Output terminal of a data shift register
15	R-EXT	Input terminal of an external resistor
16	V_{DD}	3.3/5V Supply voltage terminal

Equivalent Circuit of Inputs and Outputs

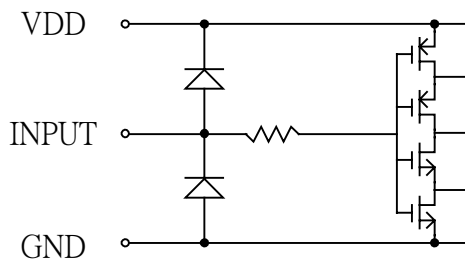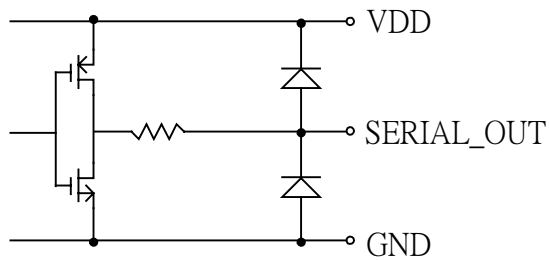**1. $\overline{\text{ENABLE}}$ terminal**
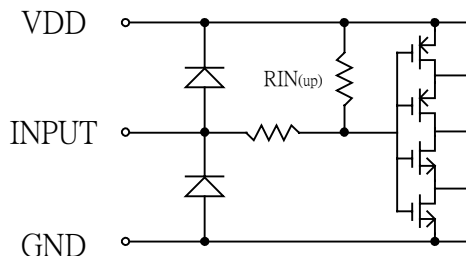
2. $\overline{\text{LATCH}}$ terminal
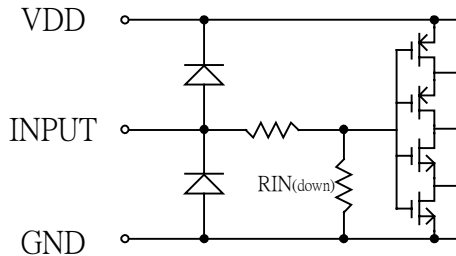
3. CLOCK, SERIAL-IN terminal

4. SERIAL-OUT terminal

Preliminary

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Maximum Ratings (Ta = 25°C, Tj$_{(max)}$ = 150°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V$_{DD}$	0 ~ 7.0	V
Input Voltage	V$_{IN}$	-0.4 ~ VDD+0.4	V
Output Current	I$_{OUT}$	90 (DM114)	mA
		60 (DM115)	
Output Voltage	V$_{OUT}$	-0.3 ~ 17	V
Clock Frequency	f$_{CLK}$	25	MHz
GND Terminal Current	I$_{GND}$	750	mA
		500	
Power Dissipation	P$_D$	1.64 (PDIP-16 : Ta=25°C)	W
		1.08 (SOP-16 : Ta=25°C)	
		0.8 (SSOP-16 : Ta=25°C)	
Thermal Resistance	R$_{th(j-a)}$	76 (PDIP-16)	°C/W
		115 (SOP-16)	
		155 (SSOP-16)	
Storage Temperature	T$_{stg}$	-55 ~ 150	°C

Recommended Operating Condition

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V$_{DD}$	——	3.0	——	5.5	V
Output Voltage	V$_{OUT}$	——	——	——	17	V
Operating temperature	T$_{OPR}$	——	-40	——	85	℃
Output Current	I$_O$	OUTn	——	——	60	mA
	I$_{OH}$	SERIAL-OUT	——	——	1.0	
	I$_{OL}$	SERIAL-OUT	——	——	-1.0	
Input Voltage	V$_{IH}$	——	0.7VDD	——	VDD+0.3	V
	V$_{IL}$	——	-0.3	——	0.3VDD	
LATCH Pulse Width	tw $_{LAT}$	V$_{DD}$ = 3.0 ~ 5.5 V	15	——	——	ns
CLOCK Pulse Width	tw $_{CLK}$		15	——	——	ns
Set-up Time for DATA	tsetup(D)		10	——	——	ns
Hold Time for DATA	thold(D)		10	——	——	ns
Set-up Time for LATCH	tsetup(L)		15	——	——	ns
Clock Frequency	f$_{CLK}$	2 chips cascade operation	——	——	25	MHz
Power Dissipation	P$_D$	Ta = 85°C(PDIP-16)	——	——	0.85	W
		Ta = 85°C(SOP-16)	——	——	0.56	
		Ta = 85°C(SSOP-16)	——	——	0.41	

Electrical Characteristics (VDD = 5.0 V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION		MIN.	TYP.	MAX.	UNIT
Input Voltage "H" Level	V_{IH}	——		0.7VDD	——	VDD	V
Input Voltage "L" Level	V_{IL}	——		GND	——	0.3VDD	
Output Leakage Current	I_{OH}	VOH = 17 V		——	——	1.0	uA
Output Voltage (S - OUT)	V_{OL}	IOL = 1.0 mA, VDD=5V		——	——	0.4	V
	V_{OH}	IOH = -1.0 mA, VDD=5V		4.6	——	——	
	V_{OL}	IOL = 1.0 mA, VDD=3.3V		——	——	0.4	
	V_{OH}	IOH = -1.0 mA, VDD=3.3V		2.7	——	——	
Output Current (Bit-Bit)	ΔI_{out}	DM114 VOUT = 1.2V	REXT = 390Ω	——	±1.5	±4	%
		DM115 (1 channel on)	REXT = 780Ω				
Output Current (Chip-Chip)	I_{out}	DM114 VOUT = 1.2V	REXT = 390Ω	36.0	40.0	44.0	mA
		DM115 (1 channel on)	REXT = 780Ω	18.0	20.0	22.0	
Output Voltage Regulation	% / V_{out}	Vdd = 3.3V ~ 5.0V		——	0.1	0.5	% / V
Pull-Up Resistor	$R_{IN(up)}$	——		200	400	600	KΩ
Pull-Down Resistor	$R_{IN(down)}$	——		100	200	300	KΩ
Supply Current "OFF"	$I_{dd (off)}$ VDD=5V	DM114 REXT = OPEN, all outputs off		——	1.3	——	mA
		DM114 REXT = 200Ω, OUT0~7 = off			11.0		
		DM115 REXT = OPEN, all outputs off		——	5.0	——	
		DM115 REXT = 300Ω, OUT0~7 = off		——	11.0	——	
Supply Current "ON"	$I_{dd (on)}$ VDD=5V	DM114 REXT = 200Ω, OUT0~7 = on		——	11.0	——	
		DM115 REXT = 300Ω, OUT0~7 = on		——	11.0	——	
Supply Current "OFF"	$I_{dd (off)}$ VDD=3.3V	DM114 REXT = OPEN, all outputs off		——	1.1	——	mA
		DM114 REXT = 200Ω, OUT0~7 = off			10.7		
		DM115 REXT = OPEN, all outputs off		——	1.1	——	
		DM115 REXT = 300Ω, OUT0~7 = off		——	7.2	——	
Supply Current "ON"	$I_{dd (on)}$ VDD=3.3V	DM114 REXT = 200Ω, OUT0~7 = on		——	10.7	——	
		DM115 REXT = 300Ω, OUT0~7 = on		——	7.2	——	

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Switching Characteristics (Ta = 25 °C unless otherwise noted)

DM114

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time ("L" to "H")	ENABLE-OUTn	tp_{LH}	VDD=5.0V VIH=VDD VIL=GND	—	40	80	ns
	CLK-SOUT			—	16	20	
Propagation Delay Time ("H" to "L")	ENABLE-OUTn	tp_{HL}	REXT=210Ω VL=5.0V RL=47Ω CL=15pF	—	70	140	ns
	CLK-SOUT			—	16	20	
Output Current Rise Time		t_{or}		—	250	400	ns
Output Current Fall Time		t_{of}		—	30	50	ns

DM115

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time ("L" to "H")	ENABLE-OUTn	tp_{LH}	VDD=5.0V VIH=VDD VIL=GND	—	40	80	ns
	CLK-SOUT			—	16	20	
Propagation Delay Time ("H" to "L")	ENABLE-OUTn	tp_{HL}	REXT=630Ω VL=5.0V RL=150Ω CL=15pF	—	70	140	ns
	CLK-SOUT			—	16	20	
Output Current Rise Time		t_{or}		—	10	15	ns
Output Current Fall Time		t_{of}		—	30	50	ns

Note: (Delay between outputs)

The DM114、DM115 also incorporated the delay unit between outputs. The delay time is 4 ns(typ.), out7 has no delay, out5 has 4 ns delay, out 3 has 8 ns delay, and then out 1, out 0, out 2, out 4, out6. The delay is to prevent large current impulse.
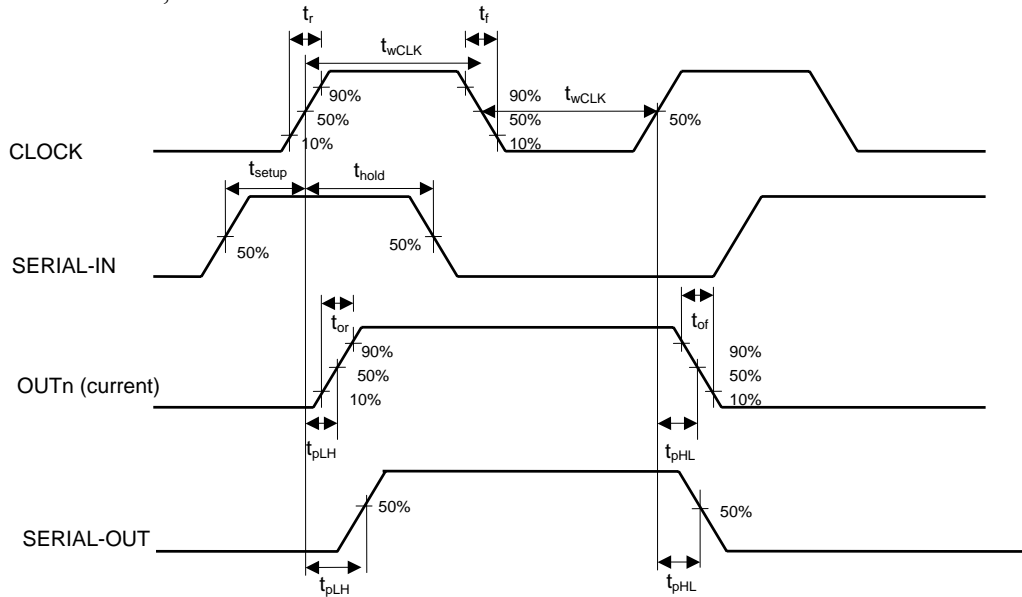
Test Circuit
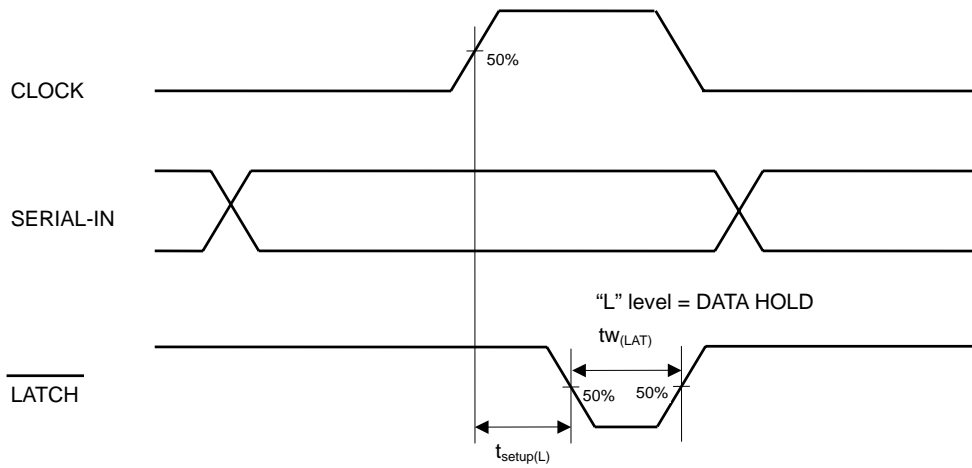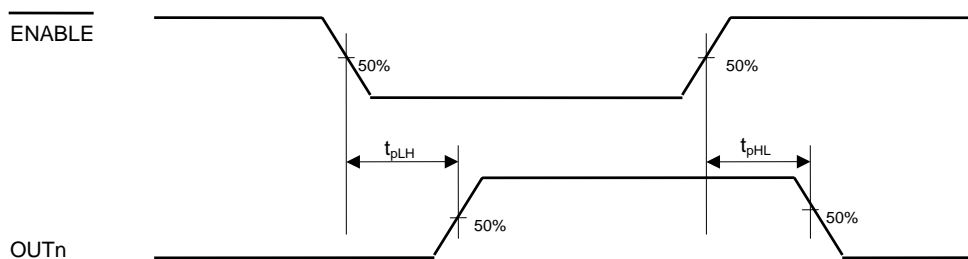
DC characteristic
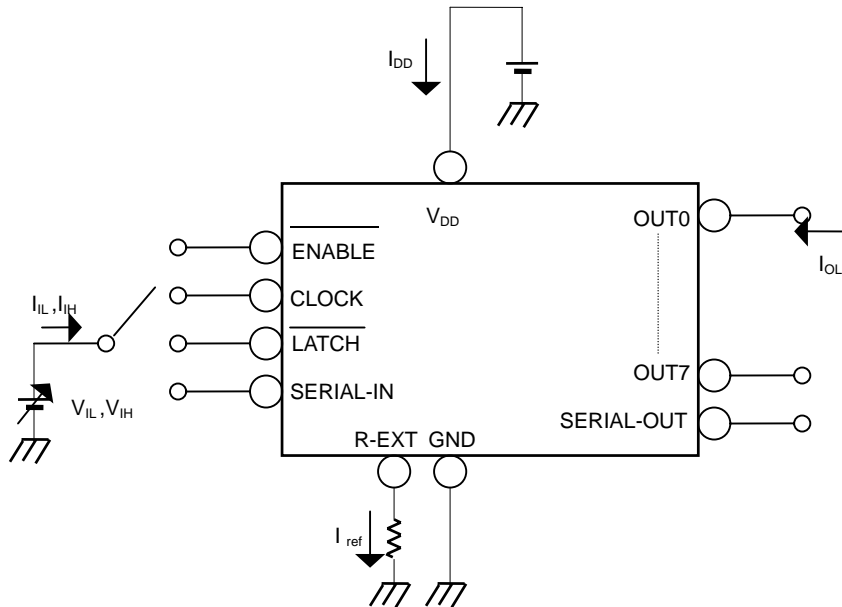
AC characteristic

Preliminary
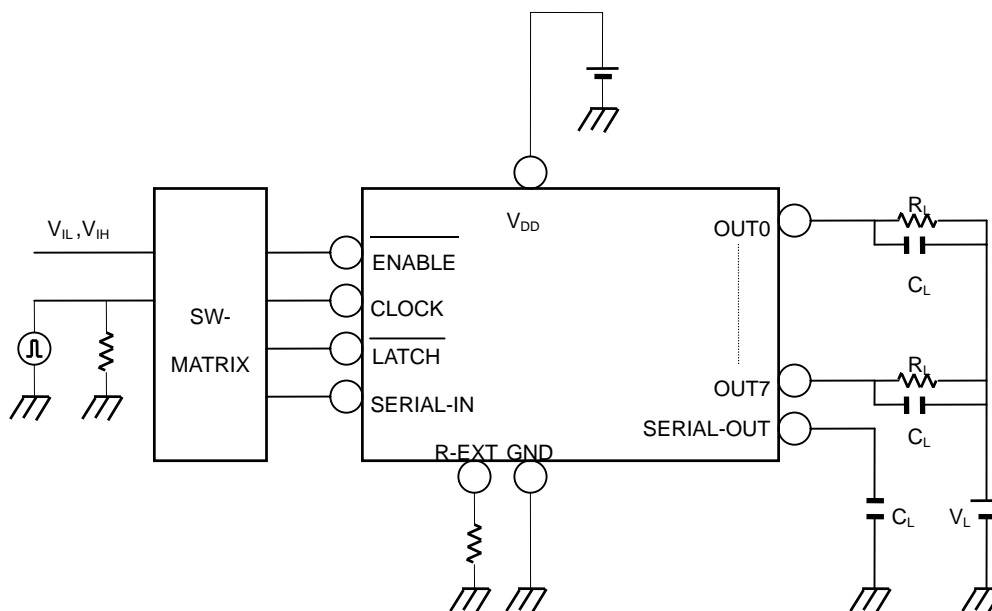
Timing Diagram

1. CLOCK-SERIAL OUT, OUTn

2. CLOCK-$\overline{\text{LATCH}}$

3. $\overline{\text{ENABLE}}$-OUTn (Current)

Output Current vs. External Resistor

DM114   **DM115**
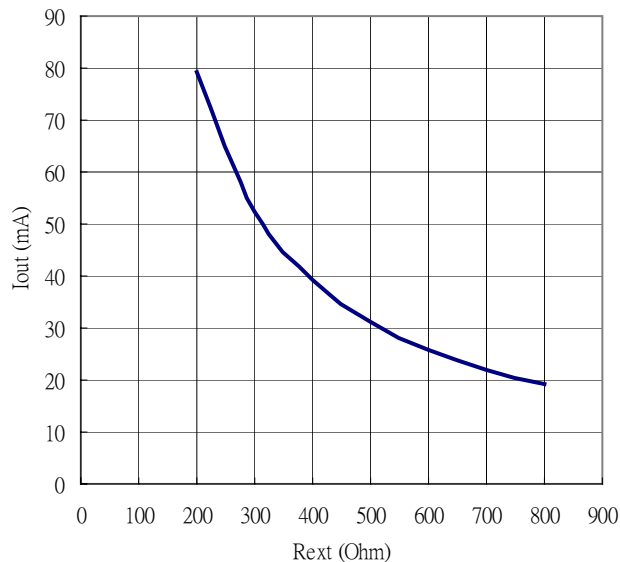
DM114:   Iout ≈ 1.3V / Rext * 12   DM115:   Iout ≈ 1.3V / Rext * 12.5
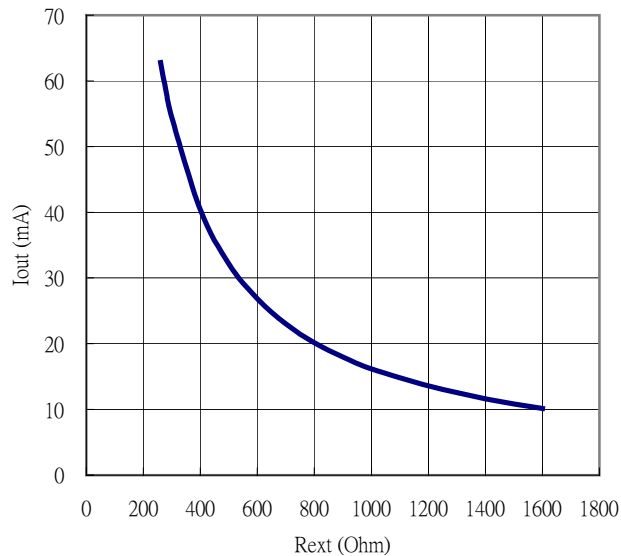
Output Current Performance vs. Output Voltage
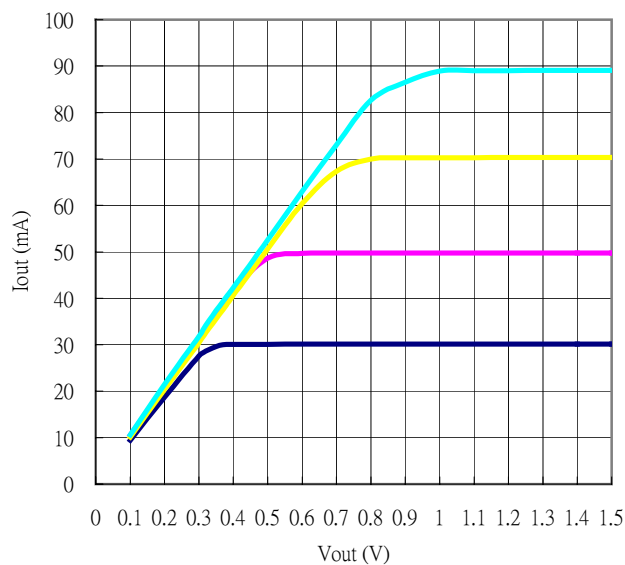
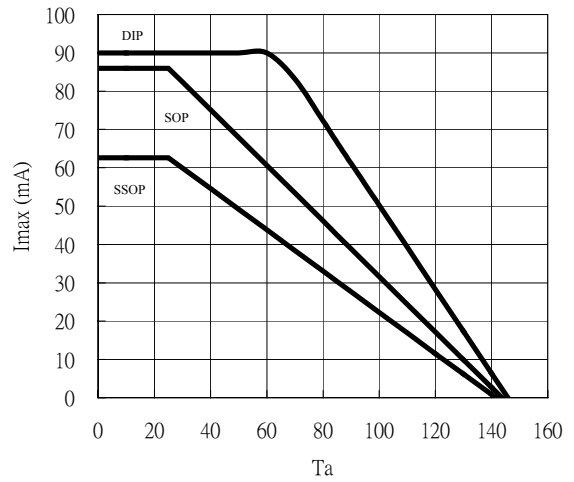**DM114**   **DM115**
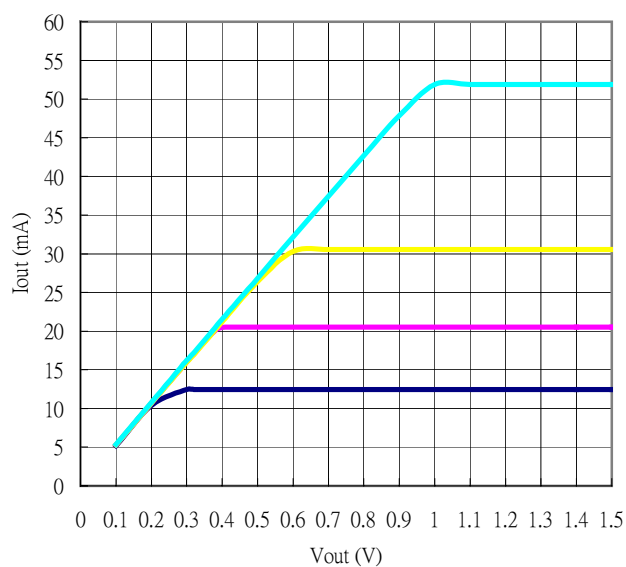
Note: In order to obtain a good constant current output, a suitable output voltage is necessary. Users can get related information about the minimum output voltage from the above graph.
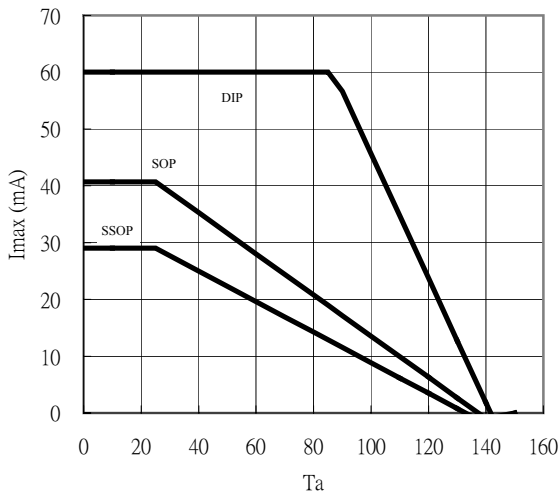
Pd - Ta
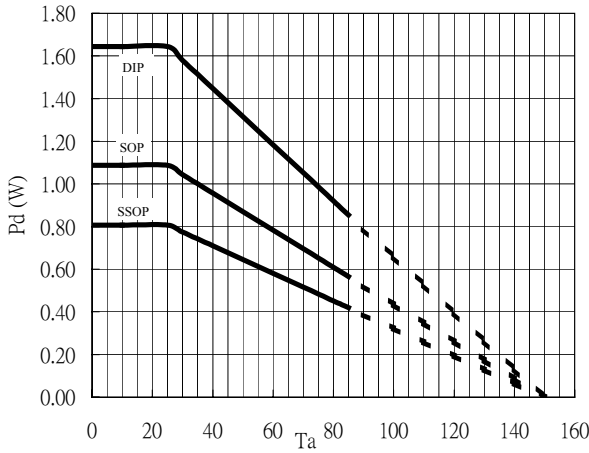
Imax - Ta (DM114)

Imax - Ta (DM115)

Note

   As the power dissipation of a semiconductor chip is limited its package and ambient temperature, this device requires a maximum output current be calculated for a given operating condition.   The maximum allowable power consumption (Pd (max)) of this device is calculated as follows:

$$Pd(\max)(Watt) = \frac{(Tj\,(junction\ temperature)\,(max) - Ta\,(ambient\ temperature)\,)(°C)}{Rth\,(°C/Watt)}$$

Based on the Pd (max), the maximum allowable current can be calculated as follows:

$$Iout = (\ Pd - V_{DD} \cdot I_{DD}) / (\ \#\ outputs \cdot Vo \cdot Duty\ )$$

System Configuration Example

[1] Output current (I_{OUT})

Sink current is set by the external resistor as shown in figure (Iout vs. Rext).

[2] LED supply voltage (V_{LED}) setup

$$V_{LED} = V_{CE} (T_r V_{sat}) + V_f (\text{LED forward voltage}) + V_O (\text{IC supply voltage})$$

To prevent too much power dissipated by the device due to higher V_{LED}, an additional R can be used to reduce the Vout when the outputs consume current:
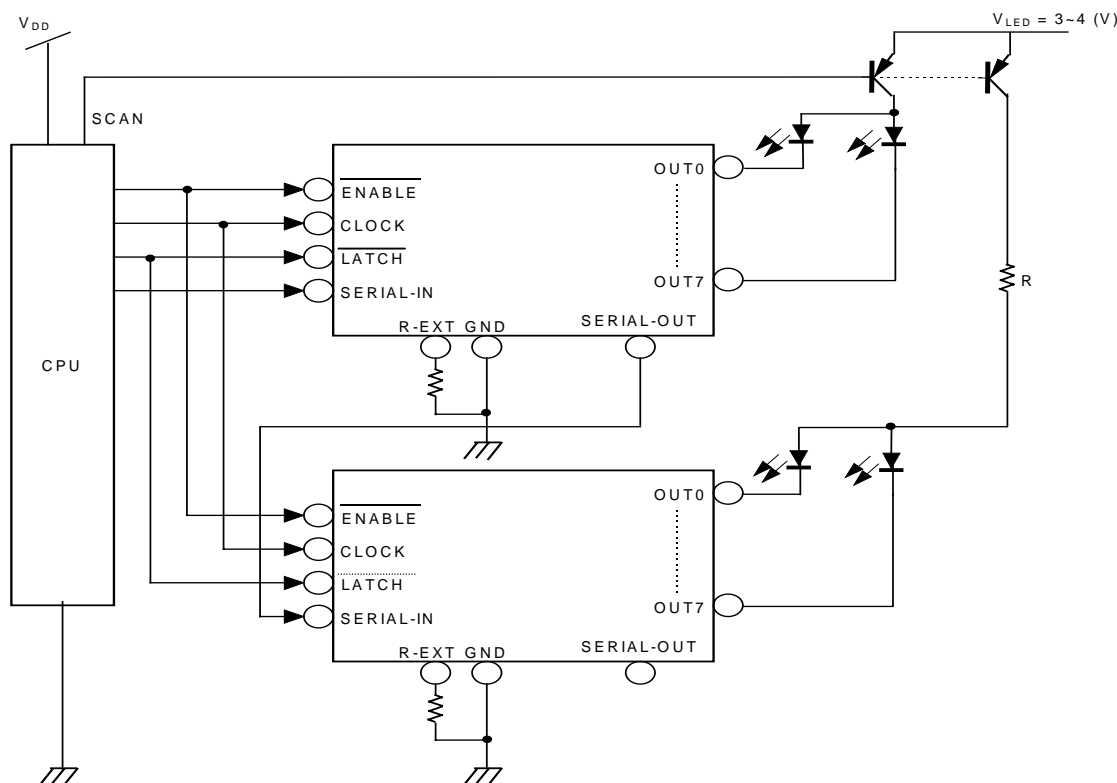
$$R = \frac{V_{LED} - V_f - V_O(\min)}{I_O(\max) \bullet Bit(\max)}$$
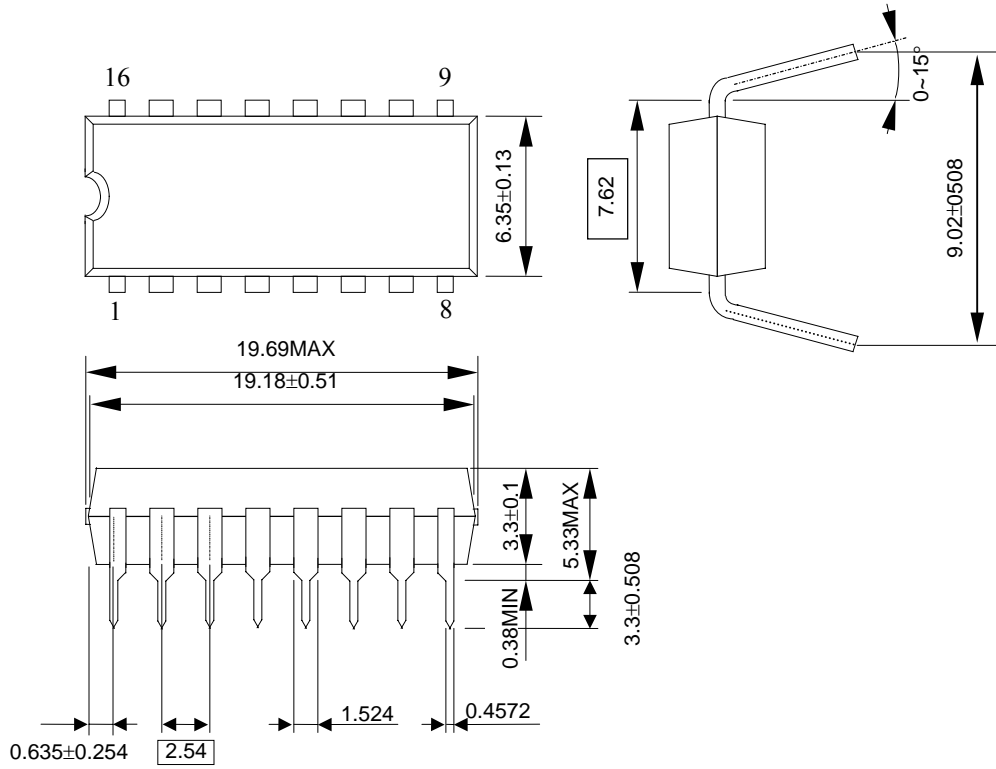
Note

This device has only one ground pin shared by signal, output sink current, and power ground.

It is advisable to pattern the ground layout with minimized inductance such that the switching noise induced by the input signals and the output sink current would not cause chip malfunction. To prevent the drivers' outputs from damage by overshoot stress, it is also advisable not to turn off the drivers and scan transistors simultaneously.
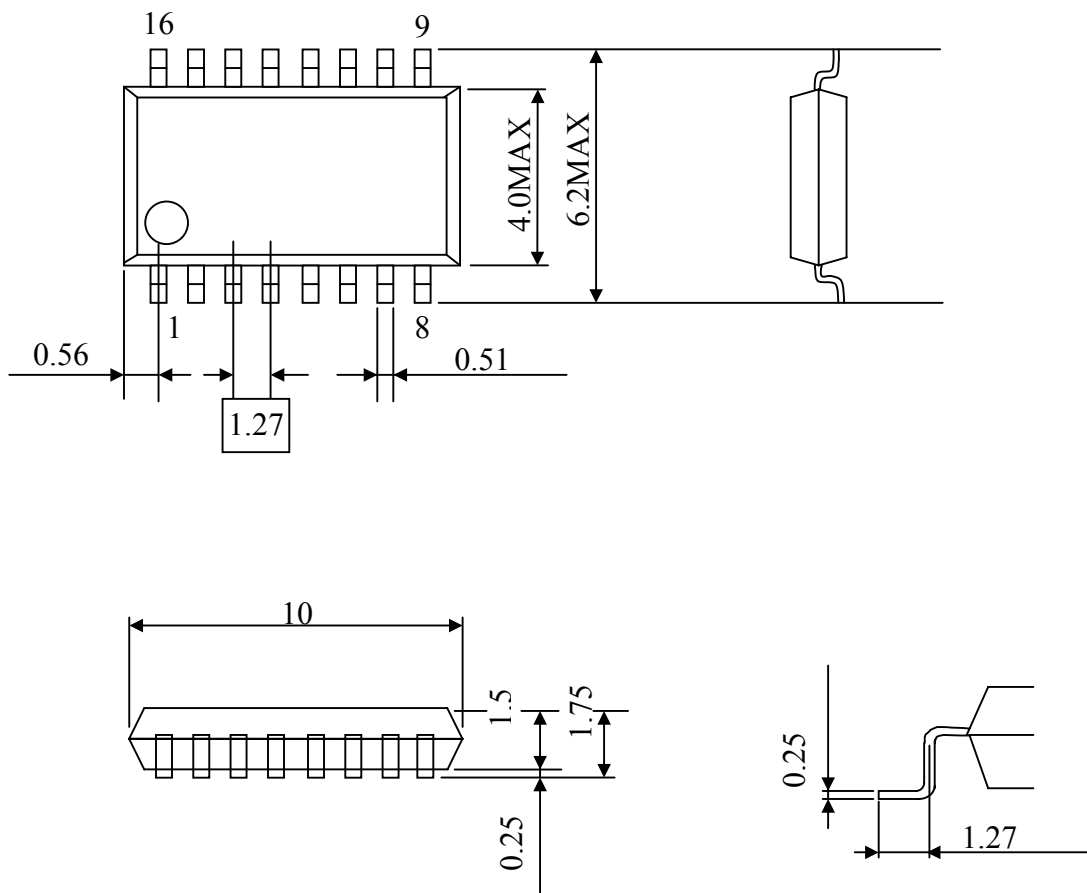
Package Outline

PDIP16

Unit: mm

16   9

6.35±0.13

7.62

0~15°

9.02±0508

1   8

19.69MAX

19.18±0.51

3.3±0.1

5.33MAX

0.38MIN

3.3±0.508

1.524

0.4572

0.635±0.254   2.54

Weight : 1.11g(Typ.)

Package Outline

SOP16

Unit: mm

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Package Outline

SSOP16

Unit: mm

16   9

3.91

5.99

1

0.229

0.635

8

0.3Max

4.9

1.5

1.63MAX

0.15

0.254

0.635
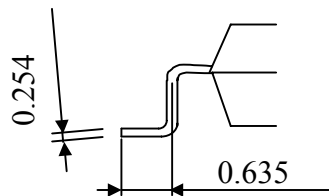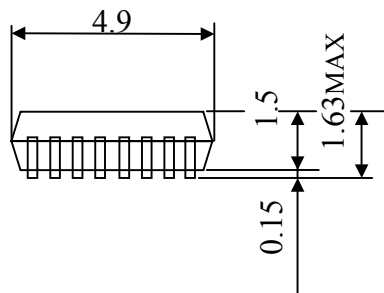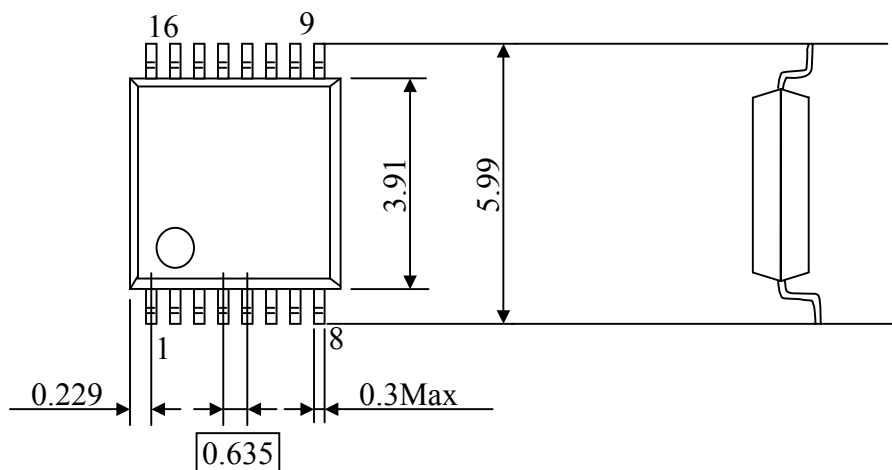
The products listed herein are designed for ordinary electronic applications, such as electrical appliances, audio-visual equipment, communications devices and so on. Hence, it is advisable that the devices should not be used in medical instruments, surgical implants, aerospace machinery, nuclear power control systems, disaster/crime-prevention equipment and the like. Misusing those products may directly or indirectly endanger human life, or cause injury and property loss.
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