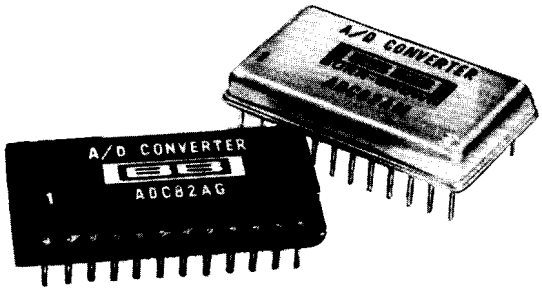
BURR-BROWN®



ADC82

IC ANALOG-TO-DIGITAL CONVERTERS

FEATURES

- **ABSOLUTE ACCURACY - No external gain or offset adjustments are required for 0 to +10V or ±10V signal ranges**
- **PRECISION - ±1/2LSB maximum nonlinearity error**
- **COMPACT DESIGN - 24-pin ceramic or metal dual-in-line package**
- **LOW COST - Ceramic packaged ADC82AG**
- **FAST CONVERSION SPEED - 2.8μsec, max Throughput sampling rates of over 300kHz Faster conversion speeds obtainable with optional external clock**
- **COMPLETELY SELF-CONTAINED - Internal clock, comparator, and reference**

DESCRIPTION

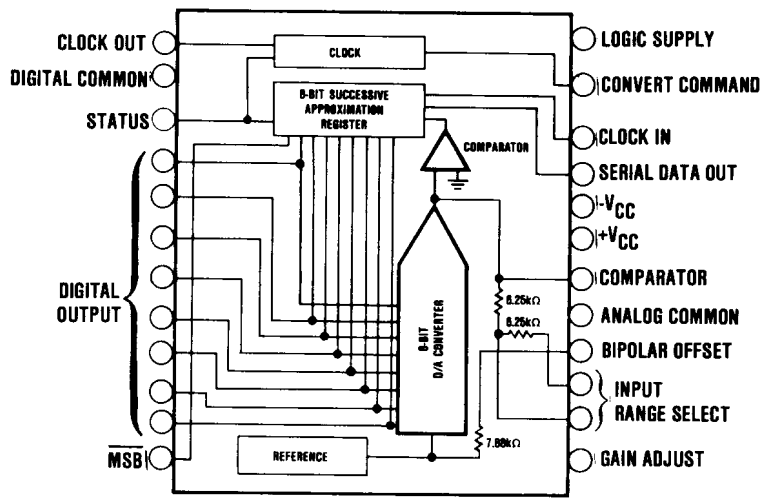
The model ADC82AG and ADC82AG are high-speed, 8-bit successive-approximation A/D converters designed for applications requiring system throughput sampling rates of over 300kHz. They utilize state-of-the-art IC and laser-trimmed thin-film components and are packaged in a 24-pin ceramic (ADC82AG) or metal (ADC82AM) package.

Thin-film internal scaling resistors are provided for the selection of analog input signal ranges of ±2.25V, ±5V, ±10V, 0 to +5, 0 to +10V, or 0 to +20V.

No external adjustments are required to obtain initial absolute accuracies of better than ±1LSB for the 0 to +10V or ±10V signal ranges. Gain and offset errors may be externally trimmed to zero to obtain even greater accuracy.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are DTL/TTL-compatible. Power supply voltages are ±15VDC and +5VDC.

FUNCTIONAL DIAGRAM



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DISCUSSION OF PERFORMANCE

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent Quantization Error of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors, including Gain, Offset, Linearity, Differential Linearity and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits Off) and Offset drift shifts the line left or right over the operating temperature range. Linearity error is unadjustable and is the most meaningful indicator of A/D converter accuracy. Linearity error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A Differential Linearity error of ±1/2LSB means that the width of each bit step over the range of the A/D converter is 1LSB ±1/2LSB.

The ADC82 is also Monotonic, assuring that the output digital code either increases or remains the same for increasing analog input signals. A monotonic converter can have missing codes; therefore, Burr-Brown specifies no missing codes over a temperature range.

TIMING CONSIDERATIONS

The timing diagram of the ADC82 (see Figure 2) assumes an analog input such that the positive true digital word 10011000 exists. The output will be complementary as shown in Figure 2 (01100111 is the digital output).

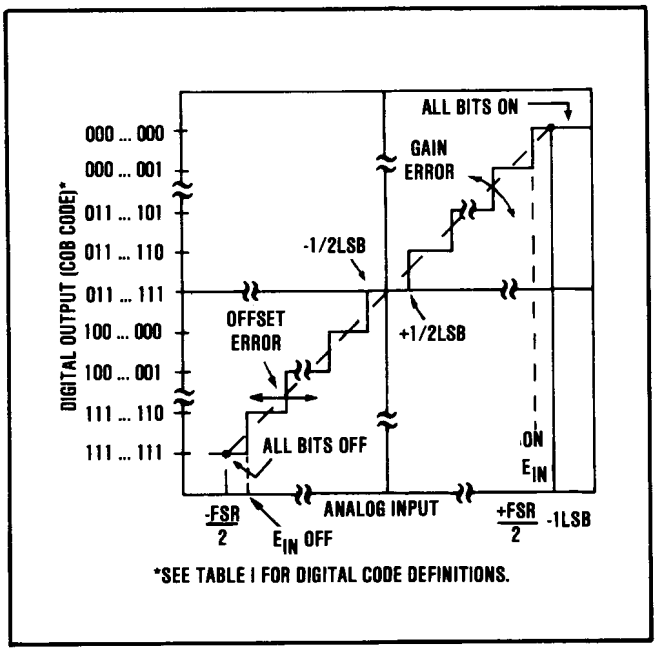


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

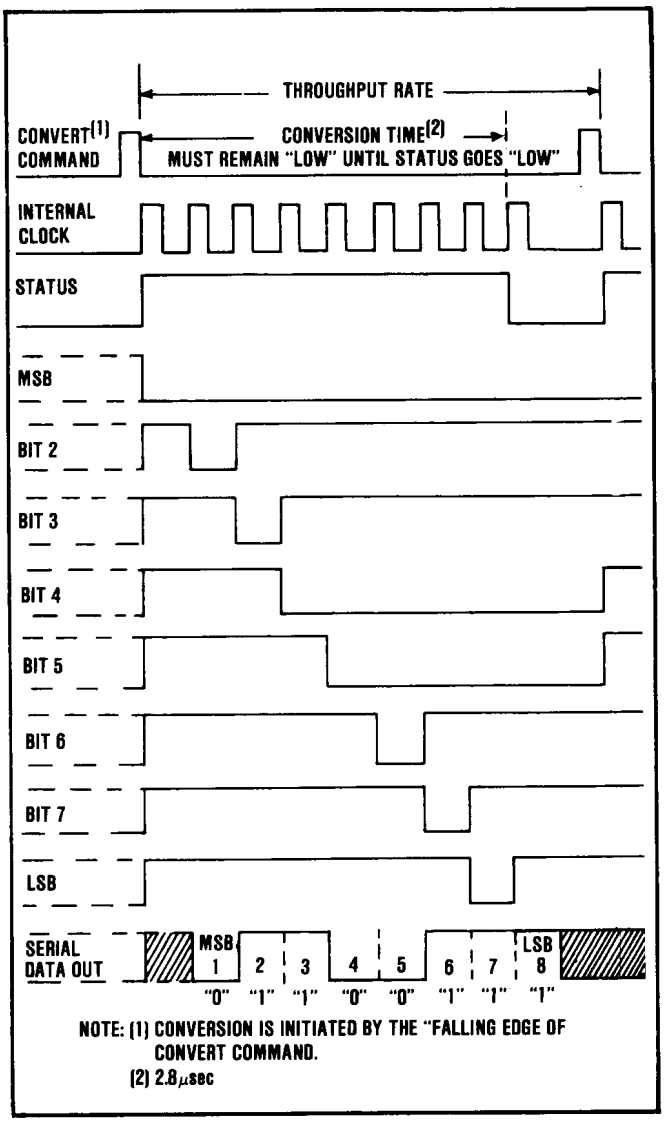


FIGURE 2. ADC82 Timing Diagram.

SPECIFICATIONS

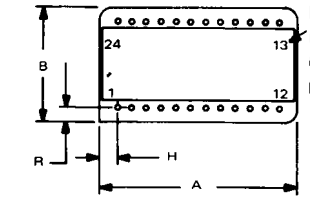
ELECTRICAL

Typical at +25°C and rated power supplies unless otherwise noted.

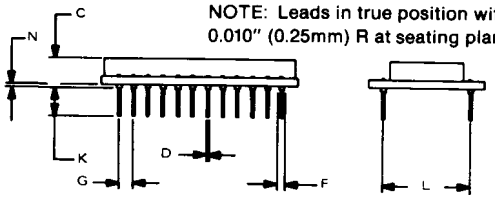
MODEL	ADC82AG ADC82AM	UNITS
RESOLUTION	8	Bits
INPUT		
ANALOG INPUTS		
Voltage Ranges		
Bipolar	±2.5, ±5, ±10	V
Unipolar	0 to +5, 0 to +10, 0 to +20	V
Impedance (Direct Inputs)		
0 to +5V, ±2.5V	3.125	kΩ
0 to +10V, ±5V	6.25	kΩ
0 to +20V, ±10V	12.50	kΩ
DIGITAL INPUTS(1)		
Convert Command	Positive pulse 50nsec wide (min) trailing edge ("1" to "0") initiates conversion	
Logic Loading	1	TTL Load
External Clock	1	TTL Load
TRANSFER CHARACTERISTICS		
ERROR		
Total Accuracy Error, max	±1	LSB
Gain Error(2)	±0.1	%
Offser Error(2)		
Unipolar	±0.05	% of FSR(3)
Bipolar	±0.05	% of FSR
Linearity Error, max(4)	±0.2	% of FSR
Inherent Quantization Error	±1/2	LSB
Differential Linearity Error	±1/2	LSB
No Missing Codes Temp. Range	0 to 70	°C
Power Supply Sensitivity		
+15V	±0.02	% of FSR/%Vs
+5V and -15V	±0.006	% of FSR/%Vs
DRIFT		
Specification Temp. Range	-25 to +85	°C
Gain, max	±40	ppm/°C
Offset		
Unipolar	±20	ppm of FSR°C
Bipolar, max	±35	ppm of FSR°C
Linearity, max	±20	ppm of FSR/°C
Monotonicity	Guaranteed	
CONVERSION SPEED, max(5)	2.8	µsec
OUTPUT		
DIGITAL DATA (All codes complementary)		
Parallel		
Output Codes(6)		
Unipolar	CSB	
Bipolar	COB, CTC	
Output Drive	5	TTL Loads
Serial Data Codes (NRZ)	CSB, COB	
Output Drive	5	TTL Loads
Status	Logic "1" during conversion	
Status Output Drive	5	TTL Loads
Internal Clock		
Clock Output Drive	4	TTL Loads
Frequency(7)	2.85	MHz
POWER REQUIREMENTS		
Rated Voltages	±15, +5	VDC
Range for Rated Accuracy(8)	+4.75 to +5.25, ±14.5 to ±15.5	VDC
Supply Drain, +15VDC	+20	mA
-15VDC	-20	mA
+5VDC	+80	mA
TEMPERATURE RANGE		
Specification	-25 to +85	°C
Storage	-55 to +125	°C

MECHANICAL

ADC82AG



Pin numbers shown for reference only. Numbers may not be marked on package.

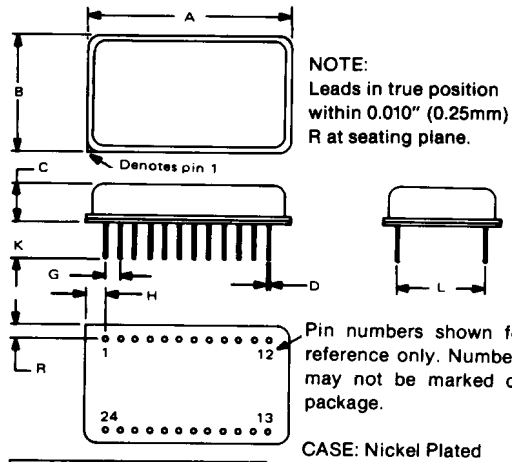


NOTE: Leads in true position within 0.010" (0.25mm) R at seating plane.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.310	1.360	33.27	34.54
B	.770	.810	19.56	20.57
C	.150	.210	3.81	5.33
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.600 BASIC		15.24 BASIC	
N	.002	.010	0.05	0.25
R	.085	.105	2.16	2.67

CASE: Ceramic
MATING CONNECTOR: 245MC
PIN: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).
WEIGHT: 7 grams, (0.25 oz).

ADC82AM



NOTE:
Leads in true position within 0.010" (0.25mm) R at seating plane.

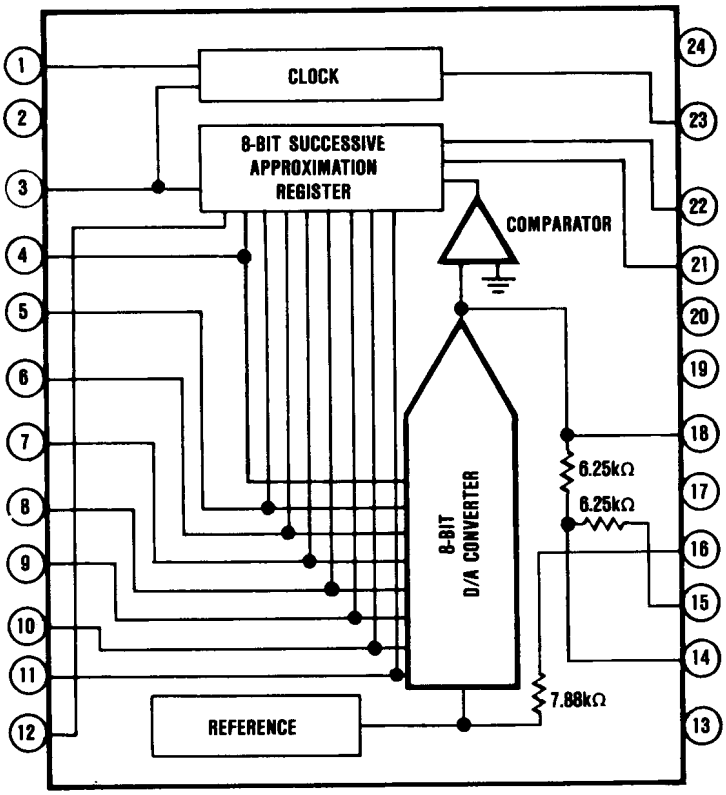
Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.365	1.385	34.67	35.18
B	.790	.810	20.07	20.57
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.125	.150	3.18	3.81
K	.150	.300	3.81	7.62
L	.600 BASIC		15.24 BASIC	
R	.080	.110	2.03	2.79

CASE: Nickel Plated
MATING CONNECTOR: 245MC
PIN: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).
WEIGHT: 7 grams, (0.25 oz).

NOTES:
1. DTL/TTL compatible i.e., Logic "0" = 0.8V max, Logic "1" = 2.0V min.
2. FSR means Full Scale Range - for example, unit connected for ±10V range has 20V FSR.
3. Adjustable to zero with external trimpots.
4. Error shown is the same as ±1/2LSB max for resolution of A/D converter.
5. Conversion time with internal clock.
6. See Table I. CSB - Complementary Binary.
   COB - Complementary Offset Binary.
   CTC - Complementary Two's Complement.
7. For conversion speeds specified.
8. ±14.0V to ±16.0V for ±1-1/4LSB total accuracy error.

CONNECTION DIAGRAM

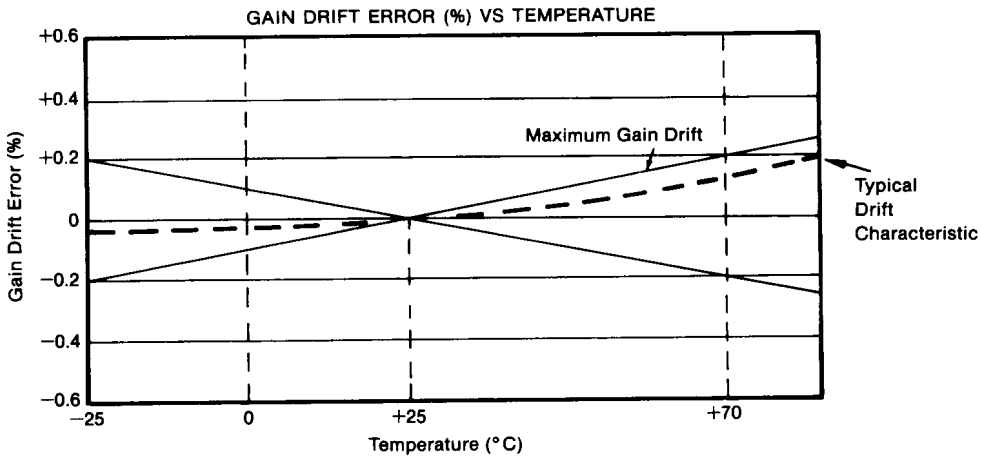


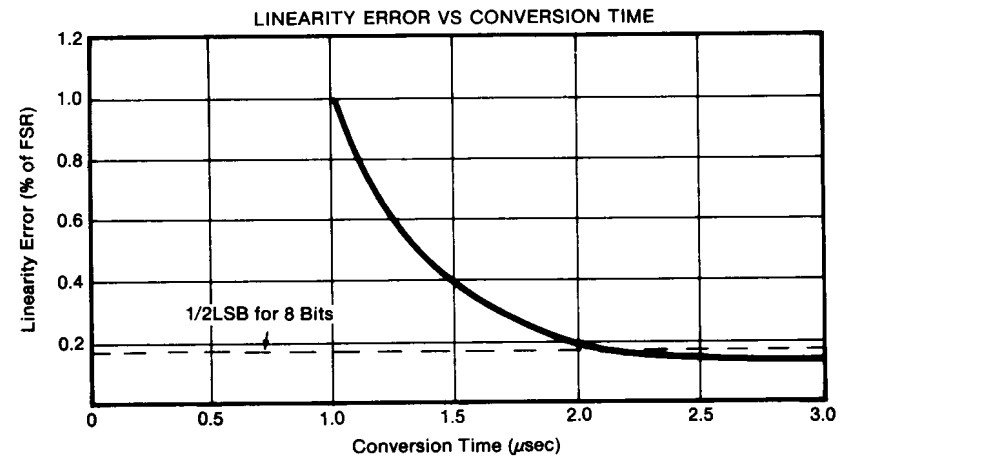
PIN ASSIGNMENTS

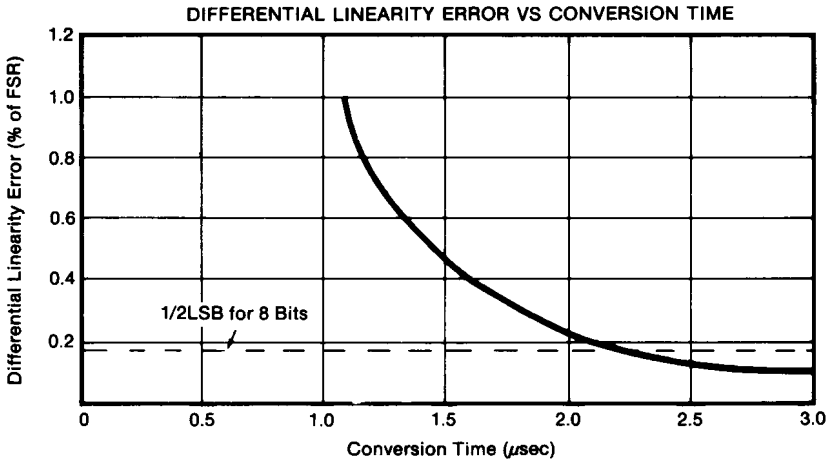
1. Clock Out
2. Digital Common*
3. Status
4. Bit 8 (LSB)
5. Bit 7
6. Bit 6
7. Bit 5
8. Bit 4
9. Bit 3
10. Bit 2
11. Bit 1 (MSB)
12. $\overline{\text{Bit 1 (MSB)}}$
13. Gain Adjust
14. R_1 (10V Range)
15. R_2 (20V Range)
16. Bipolar Offset
17. Analog Common
18. Comparator Input
19. +15
20. -15V
21. Serial Out
22. Clock In
23. Convert Command
24. +5V

*Internally connected to case on ADC82AM.

TYPICAL PERFORMANCE CURVES







DEFINITION OF DIGITAL CODES

PARALLEL DATA

Three binary codes are available on the ADC82 parallel output; they are complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges and complementary two's complement (CTC) and complementary offset binary (COB) for bipolar input signal ranges.

Table I describes the LSB, transition values and code definitions for each possible ADC82 analog input signal range.

SERIAL DATA

Two straight binary (complementary) codes are available on the serial output line of the ADC82; they are CSB and COB. The serial data is available only during conversion and appears with the most significant bit (MSB) occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values shown in Table I also apply to the serial data output except for the CTD code.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES						
Analog Input Voltage Ranges	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V	0 to +20V
Code Designation		COB or CTC*	COB or CTC*	COB or CTC*	CSB**	CSB**	CSB**
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$ n = 8	$\frac{20V}{2^n}$ 78.13mV	$\frac{10V}{2^n}$ 39.06mV	$\frac{5V}{2^n}$ 19.53mV	$\frac{10V}{2^n}$ 39.06mV	$\frac{5V}{2^n}$ 19.53mV	$\frac{20V}{2^n}$ 78.13mV
Transition Values							
MSB LSB							
000 ... 00Ø***	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5 -3/2LSB	+10V -3/2LSB	+5V -3/2LSB	+20V -3/2LSB
011 ... 111	Mid Scale	0	0	0	+5V	+2.5V	+10V
111 ... 11Ø	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2.5V +1/2LSB	0 + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB

* COB = Complementary Offset Binary
**CSB = Complementary Straight Binary
*CTC = Complementary Two's complement - obtained by using the complement of the most-significant bit ($\overline{MSB}$). $\overline{MSB}$ is avaliable on pin-12.
***Ø is the Transition Bit. Voltages given are the nominal value for transition to the code specified.

DISCUSSION OF SPECIFICATIONS

The ADC82 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors, and conversion speed effects on accuracy. The ADC82 is factory trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial gain and offset errors are factory trimmed to ±0.05% of FSR at +25°C for both the 0 to +10 and ±10V ranges. No external adjustment is required to obtain initial absolute accuracies of ±1LSB. When using one of the other input signal ranges or when even greater initial accuracy is desired these errors may be trimmed to zero by connecting external potentiometers as shown in Figures 9 and 10.

ACCURACY DRIFT VS TEMPERATURE

Three major drift parameters degrade A/D converter accuracy over temperature; they are gain, offset and linearity drift. The worst-case accuracy drift is the summation of all three drift errors over temperature. Statistically, these errors do not add algebraically, but are random variables which behave as root-sum squared (RSS) or 1σ errors as follows:

$$RSS = \sqrt{\epsilon_g^2 + \epsilon_o^2 + \epsilon_e^2}$$

Where ϵ_g = gain drift error (ppm/°C)
ϵ_o = offset drift error (ppm of FSR/°C)
ϵ_e = Linearity error (ppm of FSR/°C)

For unipolar operation, the total RSS drift is ±49.0ppm/°C and for bipolar operation, the total RSS drift is ±56.8 ppm/°C.

ACCURACY VS SPEED

In successive approximation A/D converters, the conversion speed affects linearity and differential linearity errors. Conversion speed and its effect on linearity and differential linearity errors for the ADC82 are shown in Typical Performance Curves.

The ADC82 conversion speeds are specified for a maximum linearity error of ±1/2LSB and a differential linearity error of ±1/2LSB with the internal clock. Faster conversion speeds are possible with an external clock (see Figures 6 and 7.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect the accuracy of the ADC82. The ADC82 power supply sensitivity is specified for ±0.006% of FSR/%Vs for -15V and +5V supplies and ±0.02% of FSR/%Vs for +15V supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with the ADC82. See layout precautions and power supply decoupling below.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital commons are not connected internally in the ADC82 but should be connected together as close to the unit as possible, preferably to a large ground plane under the ADC82. If these grounds must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum or electrolytic type capacitors as shown in Figure 3 to obtain noise free operation. These capacitors should be located close to the ADC82. 1μF electrolytic type capacitors should by bypassed with 0.01μF ceramic capacitors for improved high frequency performance.

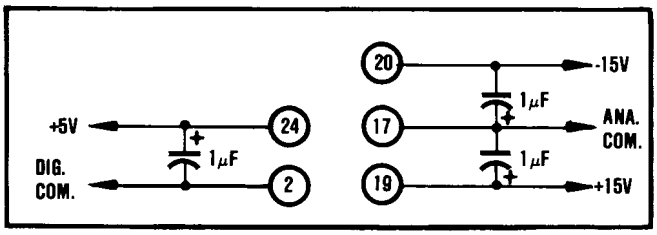


FIGURE 3. Recommended Power Supply Decoupling.

INPUT SCALING

The ADC82 input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 4 for circuit details.

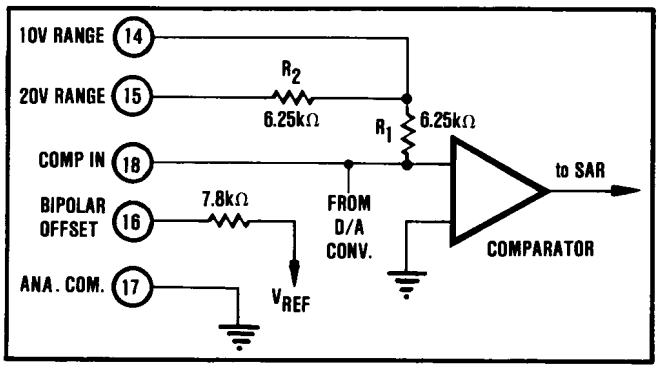


FIGURE 4. ADC82 Input Scaling Circuit.

TABLE II. ADC82 Input Scaling Connection.

Input Signal Range	Output Code	Connect Pin 16 To Pin	Connect Pin 15 To	Connect Input Signal To
±10V	COB or CTC	18	Input Signal	15
±5V	COB or CTC	18	Open	14
±2.5V	COB or CTC	18	Pin 18	14
0 to +5V	CSB	17	Pin 18	14
0 to +10V	CSB	17	Open	14
0 to +20V	CSB	17	Input Signal	15

CLOCK OPTIONS

The ADC82 is extremely versatile in that it can be operated in several different modes with either internal or external clock. Most of these options can be implemented with nothing more than an inexpensive quad 2-input NAND gate (7400) as shown in Figures 5 through 8.

CONVERTER INITIALIZATION

On power-up, the state of the ADC internal circuitry is indeterminate. One conversion cycle is required to initialize the converter after power is applied.

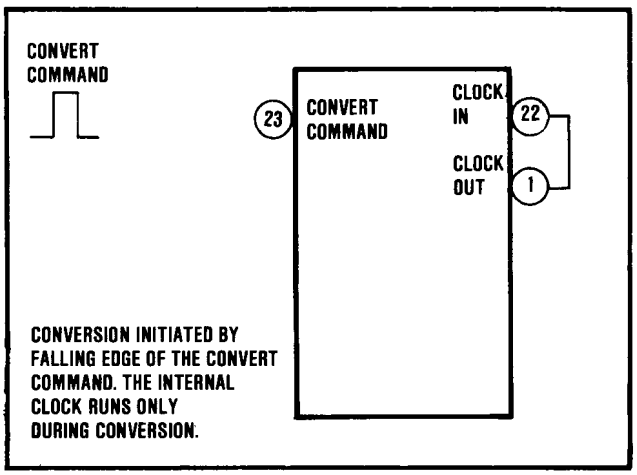


FIGURE 5. Internal Clock-Normal Operating Mode.

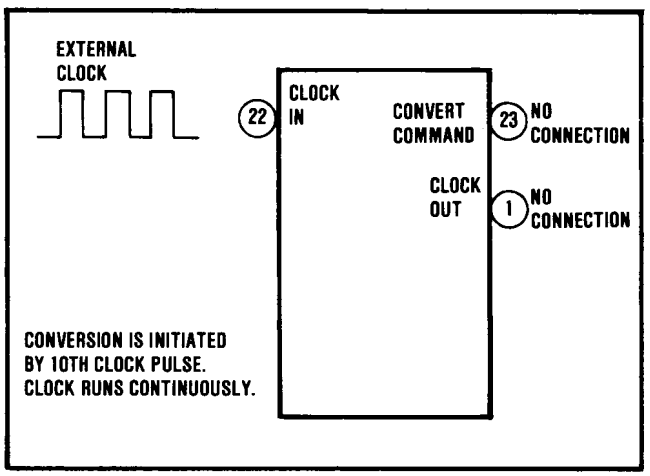


FIGURE 6. Continuous Conversion with External Clock.

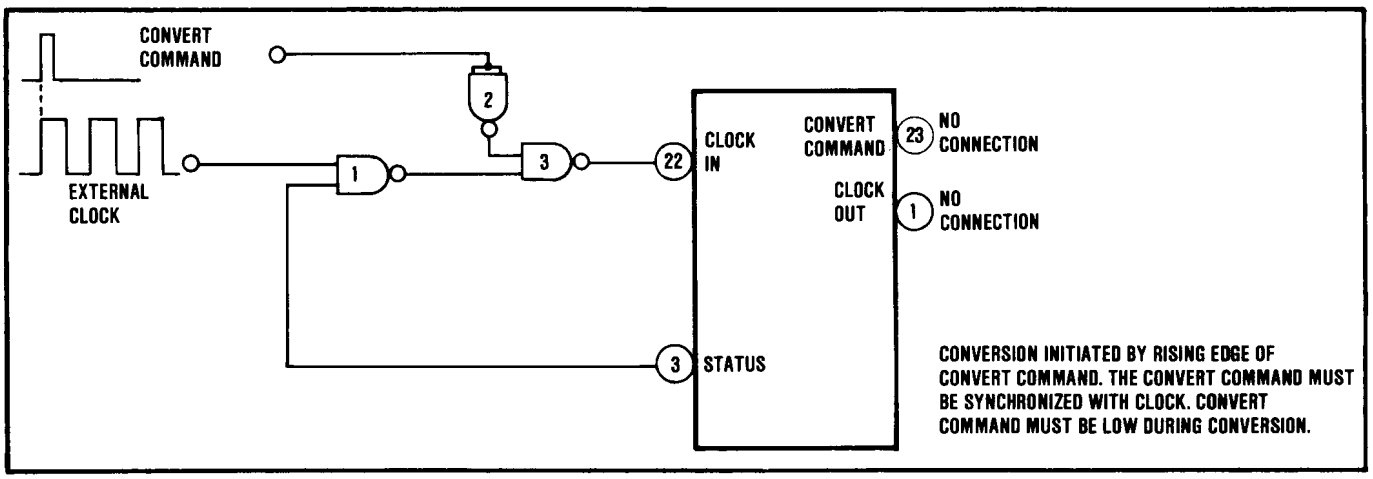


FIGURE 7. Continuous External Clock.

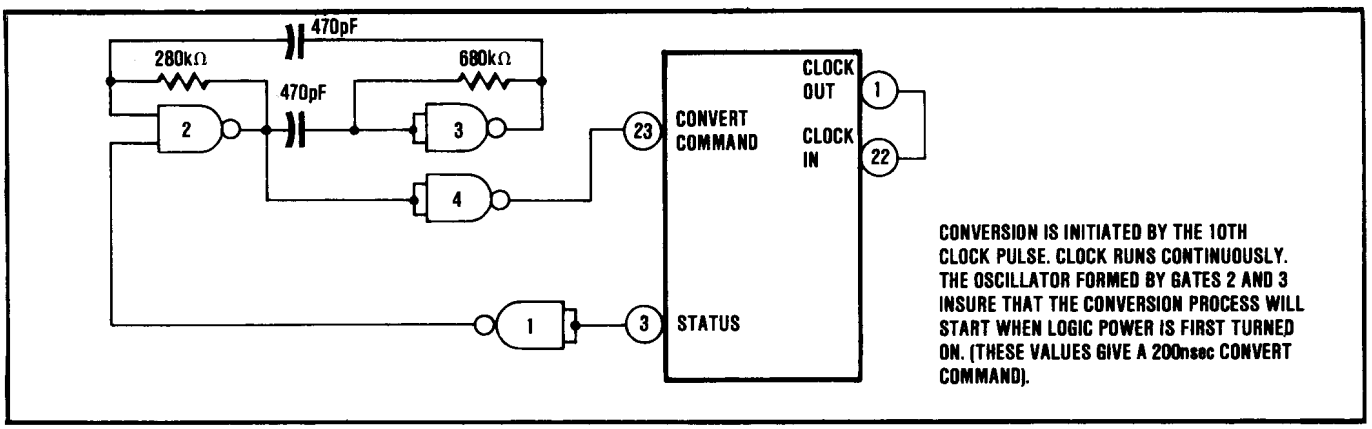


FIGURE 8. Continuous Conversion with Internal Clock.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC82 as shown in Figures 9 and 10. Multiturn potentiometers with 100ppm/°C or better TCR's are recommended for minimum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 13 (Gain Adjust) may be left open if no external adjustment is required.

ADJUSTMENT PROCEDURE

Offset - Connect the Offset potentiometer as shown in Figure 9. Sweep the input through the end point transition voltage that should cause an output transition to all bits off (E_{IN}^{OFF}).

Adjust the Offset potentiometer until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

Gain - Connect the Gain adjust potentiometer as shown in Figure 10. Sweep the input through the end point transition voltage that should cause output transitions to all bits on (E_{IN}^{ON}). Adjust the Gain potentiometer until the actual end point transition voltage occurs at E_{IN}^{ON}.

Table I details the transition voltage levels required.

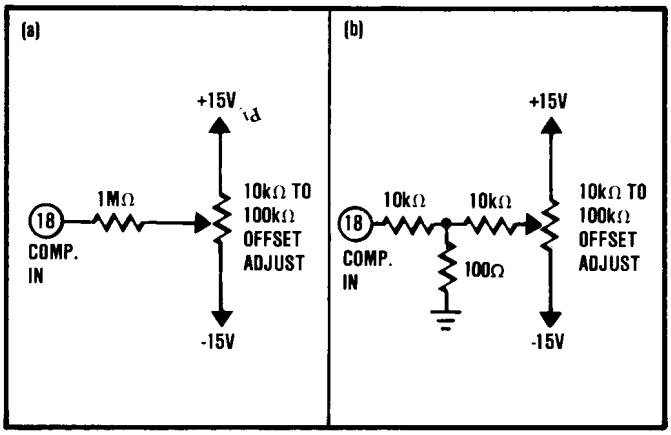


FIGURE 9. Two methods of Connecting Optional Offset Adjust with a ±1.0% of FSR Range of Adjustment.

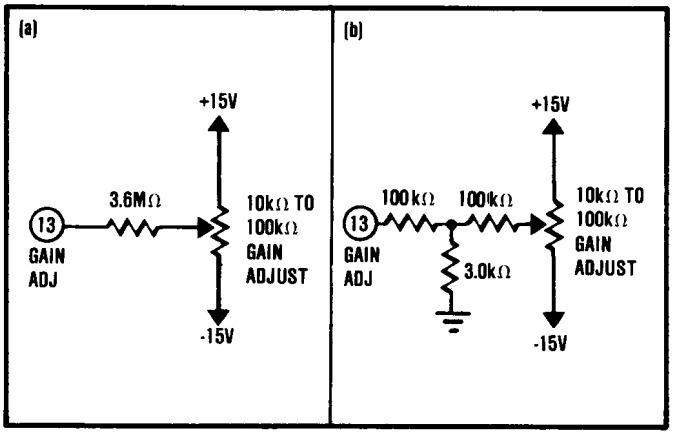


FIGURE 10. Two Methods of Connecting Optional Gain Adjust with a ±1.0% Range of Adjustment.

ORDERING INFORMATION